ELECTRONIC MECHANIC

NSQF LEVEL - 5

1st Year (Volume II of II)

TRADE THEORY

SECTOR: Electronics & Hardware

Directorate General of Training

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MINISTRY OF SKILL DEVELOPMENT & ENTREPRENEURSHIP
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NATIONAL INSTRUCTIONAL MEDIA INSTITUTE, CHENNAI

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FOREWORD

The Government of India has set an ambitious target of imparting skills to 30 crores people, one out of every four Indians, by 2020 to help them secure jobs as part of the National Skills Development Policy. Industrial Training Institutes (ITIs) play a vital role in this process especially in terms of providing skilled manpower. Keeping this in mind, and for providing the current industry relevant skill training to Trainees, ITI syllabus has been recently updated with the help of Media development committe members of various stakeholders viz. Industries, Entrepreneurs, Academicians and representatives from ITIs.

The National Instructional Media Institute (NIMI), Chennai, has now come up with instructional material to suit the revised curriculum for **Electronic Mechanic 1st Year (Volume II of II) Trade Theory NSQF Level - 5 in Electronic & Hardware Sector under Semester Pattern.** The NSQF Level - 5 Trade Theory will help the trainees to get an international equivalency standard where their skill proficiency and competency will be duly recognized across the globe and this will also increase the scope of recognition of prior learning. NSQF Level - 5 trainees will also get the opportunities to promote life long learning and skill development. I have no doubt that with NSQF Level - 5 the trainers and trainees of ITIs, and all stakeholders will derive maximum benefits from these Instructional Media Packages IMPs and that NIMI's effort will go a long way in improving the quality of Vocational training in the country.

The Executive Director & Staff of NIMI and members of Media Development Committee deserve appreciation for their contribution in bringing out this publication.

Jai Hind

RAJESH AGGARWAL
Director General/ Addl.Secretary
Ministry of Skill Development & Entrepreneurship,
Government of India.

New Delhi - 110 001

PREFACE

The National Instructional Media Institute (NIMI) was established in 1986 at Chennai by then Directorate General of Employment and Training (D.G.E & T), Ministry of Labour and Employment, (now under Directorate General of Training, Ministry of Skill Development and Entrepreneurship) Government of India, with technical assistance from the Govt. of the Federal Republic of Germany. The prime objective of this institute is to develop and provide instructional materials for various trades as per the prescribed syllabi under the Craftsman and Apprenticeship Training Schemes.

The instructional materials are created keeping in mind, the main objective of Vocational Training under NCVT/NAC in India, which is to help an individual to master skills to do a job. The instructional materials are generated in the form of Instructional Media Packages (IMPs). An IMP consists of Theory book, Practical book, Test and Assignment book, Instructor Guide, Audio Visual Aid (Wall charts and Transparencies) and other support materials.

The trade practical book consists of series of exercises to be completed by the trainees in the workshop. These exercises are designed to ensure that all the skills in the prescribed syllabus are covered. The trade theory book provides related theoretical knowledge required to enable the trainee to do a job. The test and assignments will enable the instructor to give assignments for the evaluation of the performance of a trainee. The wall charts and transparencies are unique, as they not only help the instructor to effectively present a topic but also help him to assess the trainee's understanding. The instructor guide enables the instructor to plan his schedule of instruction, plan the raw material requirements, day to day lessons and demonstrations.

In order to perform the skills in a productive manner instructional videos are embedded in QR code of the exercise in this instructional material so as to integrate the skill learning with the procedural practical steps given in the exercise. The instructional videos will improve the quality of standard on practical training and will motivate the trainees to focus and perform the skill seamlessly.

IMPs also deals with the complex skills required to be developed for effective team work. Necessary care has also been taken to include important skill areas of allied trades as prescribed in the syllabus.

The availability of a complete Instructional Media Package in an institute helps both the trainer and management to impart effective training.

The IMPs are the outcome of collective efforts of the staff members of NIMI and the members of the Media Development Committees specially drawn from Public and Private sector industries, various training institutes under the Directorate General of Training (DGT), Government and Private ITIs.

NIMI would like to take this opportunity to convey sincere thanks to the Directors of Employment & Training of various State Governments, Training Departments of Industries both in the Public and Private sectors, Officers of DGT and DGT field institutes, proof readers, individual media developers and coordinators, but for whose active support NIMI would not have been able to bring out this materials.

R. P. DHINGRA
EXECUTIVE DIRECTOR

Chennai - 600 032

INTRODUCTION

TRADE THEORY

The manual of trade theory consists of theoretical information for the Second Semester course of the Electronic Machanic Trade NSQF Level - 5. The contents are sequenced according to the practical exercise contained in the manual on trade practical. Attempt has been made to relate the theortical aspects with the skill covered in each exercise to the extent possible. This co-relation is maintained to help the trainees to develop the perceptional capabilities for performing the skills.

The Trade theory has to be taught and learnt along with the corresponding exercise contained in the manual of trade practical. The indicating about the corresponding practical exercise are given sheet of this manual.

It will be preferable to teach/learn the trade theory connected to each exercise at least one class before performing the related skills in the shop floor. The trade theory is to be treated as an integrated part of each exercise.

The material is not the purpose of self - learning and should be considered as supplementary to class room instruction.

TRADE PRACTICAL

The trade practical manual is intended to be used in practical workshop . It consists of a series of practical exercises to be completed by the trainees during the second semester course of Electronic Machanic Trade supplemented and supported by instructions/ informations to assist in performing the exercises. These exercises . These exercises are designed to ensure that all the skills in compliance with NSQF Level 5 .

The manual is divided into Ten modules. The distribution of time for the practical in the Ten modules are given below.

Module 1	Transistor Amplifier	75Hrs
Module 2	Oscillators	25 Hrs
Module 3	Wave Shaping Circuits	25Hrs
Module 4	Power Electronic Components	50Hrs
Module 5	MOSFET & IGBT	25Hrs
Module 6	Opto - Electronics	25Hrs
Module 7	Basic Gates, Combinational Circuits , Flip Flops	75Hrs
Module 8	Electronic Circuit Simulator	50Hrs
Module 9	Counter & Shift Registers	75Hrs
Module 10	Op - Amp & Timer 555 Applications	100Hrs
	Project work / Industrial visit	50 Hrs
	Total	575 Hrs

The skill training in the shop floor is planned through a series of practical exercises centred around some practical object. However, there are few instances where the individual exercise does not form a part of project.

While developing the practical manual a sincere effort a sincere effort wasa made to prepare each exercise wgich will be easy to understand and carry out even by below average trainee. However the devlopment team accept that there is a scope for further improvement. NIMI, looks forward to the suggestions from the experienced training faculty for improving the manual.

ACKNOWLEDGEMENT

National Instructional Media Institute (NIMI) sincerely acknowledges with thanks for the co-operation and contribution extended by the following Media Developers and their sponsoring organisations to bring out this Instructional Material **(Trade Theory)** for the trade of **Electronic Machanic NSQF Level -5** under the **Electronic & Hardware** Sector for ITIs.

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Shri S.Gopalakrishnan	–	Assistant Manager, NIMI, Chennai - 32

NIMI records its appreciation for the Data Entry, CAD, DTP Operators for their excellent and devoted services in the process of development of this Instructional Material.

NIMI also acknowledges with thanks, the invaluable efforts rendered by all other staff who have contributed for the development of this instructional material.

NIMI is grateful to all others who have directly or indirectly helped in developing this IMP.

CONTENTS

LEARNING / ASSESSABLE OUTCOME

On completion of this book you shall be able to

- **Construct, test and verify the input/output characteristics of various analog circuits.**
- **Plan and construct different power electronic circuits and analyze the circuit functioning.**
- **Select the appropriate optoelectronic components and verify the characteristics in different circuits.**
- **Assemble, test and troubleshoot various digital circuits.**
- **Simulate and analyze the analog and digital circuits using Electronic simulator software.**
- **Identify, place, solder, desolder and test different SMD discrete components and ICs package with due care and following safety norms using proper tools/ setup.**
- **Construct and test different circuits using ICs 741 Operational Amplifiers & ICs 555 Timer, Linear integrated circuits and Execute the result.**

1st Year (Volume II of II)

Week No.	Learning outcome Reference	Professional Skills (Trade Practical) With indicative hours	Professional Knowledge (Trade Theory) with respect to different
27	• Construct, test and verify the input output characteristics of various analog circuits.	Transistor 102. Identify different transistors with respect to different package type, B-E-C pins, power, switching transistor, heat sinks etc. (5 hrs) 103. Test the condition of a given transistor using ohm-meter. (5 hrs) 104. Measure and plot input and output characteristics of a CE amplifier. (7 hrs) 105. Construct and test a transistor based switching circuit to control a relay (use Relays of different coil voltages and Transistors of different β) (8 hrs)	Construction, working of a PNP and NPN Transistors, purpose of E, B & C Terminals. Significance of α, β and relationship of a Transistor. Need for Biasing of Transistor. V_{BE}, V_{CB}, V_{CE}, I_C, I_B, Junction Temperature, junction capacitance, frequency of operation. Transistor applications as switch and amplifier. Transistor input and output characteristics. Transistor power ratings & packaging styles and use of different heat sinks.
28-29	• Construct, test and verify the input/ output characteristicsof various analog circuits.	Amplifier 106. Construct and test fixed-bias, emitter-bias and voltage devider-bias transistor amplifier. (12 hrs) 107. Construct and Test a common emitter amplifier with and without bypass capacitors (5 hrs) 108. Construct and Test common base amplifier. (5 hrs) 109. Construct and Test common collector/emitter follower amplifier. (5 hrs) 110. Construct and Test Darlington amplifier. (5 hrs) 111. Construct and test a two stage RC Coupled amplifier. (5 hrs) 112. Construct and test a Class B complementary push pull amplifier. (8 hrs) 113. Construct and test class C Tuned amplifier. (5 hrs)	Different types of biasing, various configurations of transistor (C-B, C-E & C-C), their characteristics and applications. Transistor biasing circuits and stabilization Techniques. Classification of amplifiers according to frequency, mode of operation and methods of coupling. Voltage amplifiers - voltage gain, loading effect. Single stage CE amplifier and CC amplifier. Emitter follower circuit and its advantages. RC coupled amplifier, Distinguish between voltage and power amplifier, Push pull amplifier and class C tuned amplifier. Alpha, beta, voltage gain, Concept of dB dBm. Feedback and its types.
30	• Construct, test and verify the input/ output characteristics of various analog circuits.	Oscillators 114. Demonstrate Colpitts oscillator, Hartley oscillator circuits and compare the output frequency of the oscillator by CRO. (7 hrs) 115. Construct and test a RC phase shift oscillator circuits. (5 hrs) 116. Construct and test a crystal oscillator circuits. (5 hrs)	Introduction to positive feedback and requisites of an oscillator. Study of Colpitts, Hartley, Crystal and RC oscillators. Types of multi vibrators and study of circuit diagrams.

		117. Demonstrate Astable, monostable, bistable circuits using transistors. (8 hrs)	
31	• Construct, test and verify the input/ output characteristics of various analog circuits	Wave shaping circuits 118. Construct and test shunt clipper. (6 hrs) 119. Construct and test series and dual clipper circuit using diodes. (7 hrs) 120. Construct and test clamper circuit using diodes. (5 hrs) 121. Construct and test Zener diode as a peak clipper. (7 hrs)	Diode shunt clipper circuits, Clamping / limiting circuits and Zener diode as peak clipper,uses their applications.
32-33	• Plan and construct different power electronic circuits and analyse the circuit functioning.	Power Electronic Components 122. Identify different power electronic components, their specification and terminals. (6 hrs) 123. Construct and test a FET Amplifier. (6 hrs) 124. Construct a test circuit of SCR using UJT triggering. (7 hrs) 125. Identify different heat sinks used in SCRs. (3 hrs) 126. Construct a snubber circuit for protecting SCR use freewheeling diode to reduce back emf. (7 hrs) 127. Construct a jig circuit to test DIAC. (7 hrs) 128. Construct a simple dimmer circuit using TRIAC. (7 hrs) 129. Construct UJT based free running oscillator and change its frequency. (7 hrs)	Construction of FET & JFET, difference with BJT. Purpose of Gate, Drain and source terminals and voltage / current relations between them and Impedances between various terminals. Heat Sink- Uses & purpose. Suitability of FET amplifiers in measuring device applications. Working of different power electronic components such as SCR, TRIAC, DIAC and UJT.
34	• Plan and construct different power electronic circuits and analyse the circuit functioning	MOSFET & IGBT 130. Identify various Power MOSFET by its number and test by using multimeter. (5 hrs) 131. Identify different heat sinks used with various power MOSFET devices. (5 hrs) 132. Construct MOSFET test circuit with a small load. (5 hrs) 133. Identify IGBTs by their numbers and test by using multimeter. (5 hrs) 134. Construct IGBT test circuit with a small load. (5 hrs)	MOSFET, Power MOSFET and IGBT, their types, characteristics, switching speed, power ratings and protection. Differentiate FET with MOSFET. Differentiate Transistor with IGBT.
35	• Select the appropriate opto electronics components and verify the characteristics in different circuit.	Opto Electronics 135. Test LEDs with DC supply and measure voltage drop and current using multimeter. (5 hrs) 136. Construct a circuit to test photo voltaic cell. (5 hrs) 137. Construct a circuit to switch a lamp load using photo diode. (5	Working and application of LED, IR LEDs, Photo diode, photo transistor, their characteristics and applications.

		hrs) 138. Construct a circuit to switch a lamp load using photo transistor. (5 hrs) 139. Identify opto coupler input and output terminals and measure the quantum of isolation between input/output terminals and operate a relay by connecting a switch. (5 hrs)	Optical sensor, opto-couplers, circuits with opto isolators. Characteristics of LASER diodes.
36	• Assemble, test and troubleshoot various digital circuits.	Basic Gates 140. Identify different Logic Gates (AND, OR, NAND, NOR, EXOR, EX-NOR, NOT ICs) by the number printed on them. (6 hrs) 141. Verify the truth tables of all Logic Gate ICs by connecting switches and LEDs. (8 hrs) 142. Construct and verify the truth table of all the gates using NAND and NOR gates. (6 hrs) 143. Use digital IC tester to test the various digital ICs (TTL and CMOS). (5 hrs)	Introduction to Digital Electronics. Difference between analog and digital signals. Logic families and their comparison, logic levels of TTL and CMOS. Number systems (Decimal, binary, octal, Hexadecimal). BCD code, ASCII code and code conversions. Various Logic Gates and their truth tables.
37	• Assemble, test and troubleshoot various digital circuits.	Combinational Circuits 144. Construct Half Adder circuit using ICs and verify the truth table. (3 hrs) 145. Construct Full adder with two Half adder circuit using ICs and verify the truth table. (5 hrs) 146. Construct the adder cum subtractor circuit and verify the result. (5 hrs) 147. Construct and Test a 2 to 4 Decoder. (3 hrs) 148. Construct and Test a 4 to 2 Encoder. (3 hrs) 149. Construct and Test a 4 to 1 Multiplexer. (3 hrs) 150. Construct and Test a 1 to 4 De Multiplexer. (3 hrs)	Combinational logic circuits such as Half Adder, Full adder, Parallel Binary adders, 2-bit and four bit full adders. Magnitude comparators. Half adder, full adder ICs and their applications for implementing arithmetic operations. Concept of encoder and decoder. Basic Binary Decoder and four bit binary decoders. Need for multiplexing of data. 1:4 line Multiplexer / Demultiplexer.
38	• Assemble, test and troubleshoot various digital circuits..	Flip Flops 151. Identify different Flip-Flop (ICs) by the number printed on them. (5 hrs) 152. Construct and test four bit latch using 7475. (5 hrs) 153. Construct and test R-S flipflop using IC7400 with clock and without clock pulse. (5 hrs) 154. Verify the truth tables of FlipFlop ICs (RS, D, T, JK, MSJK) by connecting switches and LEDs. (10 hrs)	Introduction to Flip-Flop. S-R Latch, Gated S-R Latch, D- Latch. Flip-Flop: Basic RS Flip Flop, edge triggered D Flip Flop, JK Flip Flop, T Flip Flop. Master-Slave flip flops and Timing diagrams. Basic flip flop applications like data storage, data transfer and frequency division.

39-40		Electronic circuit simulator 155. Prepare simple digital and electronic circuits using the software (10 hrs) 156. Simulate and test the prepared digital and analog circuits (16 hrs) 157. Convert the prepared circuit into a layout diagram. (10 hrs) 158. Prepare simple, power electronic and domestic electronic circuit using simulation software. (14 hrs)	Study the library components available in the circuit simulation software. Various resources of the software.
41-43		Counter & shift Registers 159. Construct and test a four bit asynchronous binary counter using 7493 (4 hrs) 160. Construct and test 7493 as a modulus-12 counter. (4 hrs) 161. Construct and test a four bit Synchronous binary counter using 74163. (5 hrs) 162. Construct and test synchronous Decade counter. (4 hrs) 163. Construct and test an up/down synchronous decade counter using 74190 and monitor the output on LEDs. (5 hrs) 164. Identify and test common anode and common cathode seven segment LED display using multi meter. (3 hrs) 165. Display the two digit count value on seven segment display using decoder/driver ICs. (4 hrs) 166. Construct a shift register using RS/ D/JK flip flop and verify the result. (5 hrs) 167. Construct and test four bit SIPO register. (5 hrs) 168. Construct and test four bit PIPO register. (5 hrs) 169. Construct and test bidirectional shift registers. (5 hrs)	Basics of Counters, types, two bit and three bit Asynchronous binary counters and decade counters with the timing diagrams. 3-bit Synchronous counters and synchronous decade counters. Types of seven segment display. BCD display and BCD to decimal decoder. BCD to 7 segment display circuits. Basics of Register, types and application of Registers.
44-47		Op – Amp & Timer 555 Applications 170. Use analog IC tester to test the various analog ICs. (5 hrs) 171. Construct and test various Op-Amp circuits Inverting, Non-inverting and Summing Amplifiers. (15 hrs) 172. Construct and test Differentiator and Integrator (10 hrs) 173. Construct and test a zero crossing detector. (5 hrs) 174. Construct and test Instrumentation amplifier (10 hrs) 175. Construct and test a Binary weighted and R-2R Ladder type	Block diagram and Working of Op-Amp, importance, Ideal characteristics, advantages and applications. Schematic diagram of 741, symbol. Non-inverting voltage amplifier, inverting voltage amplifier, summing amplifier, Comparator, zero cross detector, differentiator, integrator and instrumentation amplifier, other popular Op-Amps. Block diagram of 555, functional

		Digital-to-Analog Converters (15hrs.) 176. Construct and test Astable timer circuit using IC 555 (10 hrs) 177. Construct and test mono stable timer circuit using IC 555. (10 hrs) 178. Construct and test VCO (V to F Converter) using IC 555. (10 hrs) 179. Construct and test 555 timers as pulse width modulator (10 hrs)	description w.r.t. different configurations of 555 such as monostable, astable and VCO operations for various application.
48-49	Project work / Industrial visit Broad Areas: 1. Delayed automatic power on circuit. 2. Neon flasher circuit using IC 741 3. UJT act as a relaxation oscillator 4. Up/down synchronous decade counter 5. Portable continuity cum capacitor tester		
50-51	Revision		
52	Examination		

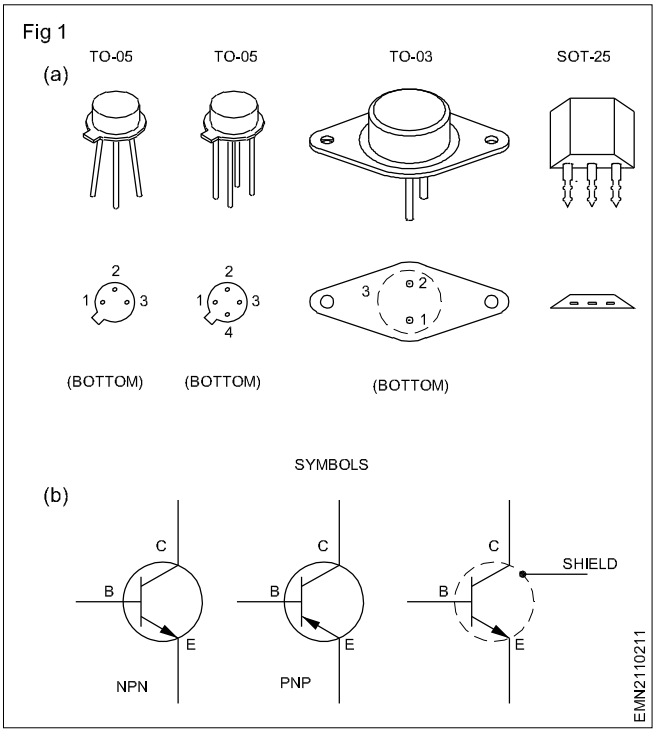
Transistors and Classification

Objectives: At the end of this lesson you shall be able to

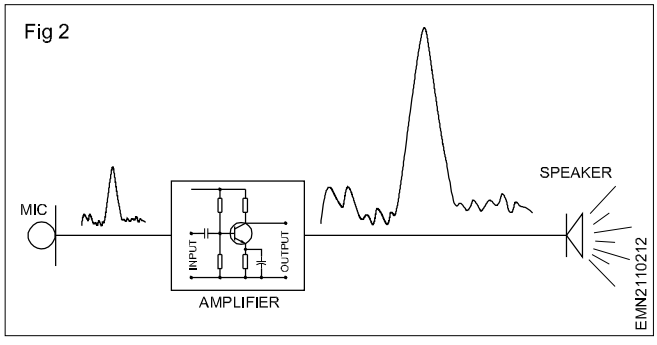
- **introduction of transistors**
- **list the advantages of transistors over vacuum tubes**
- **list the important classifications of transistors**
- **state the name and functions of terminals of a transistor**
- **name of the types of transistor packages**
- **describe the two tests to be conducted on a transistor before using it**
- **working principle of transistor.**

INTRODUCTION

Transistors are the semiconductor devices having three or four leads/terminals. Fig 1a shows some typical transistors. Fig 1b shows the symbols used for different types of transistors.

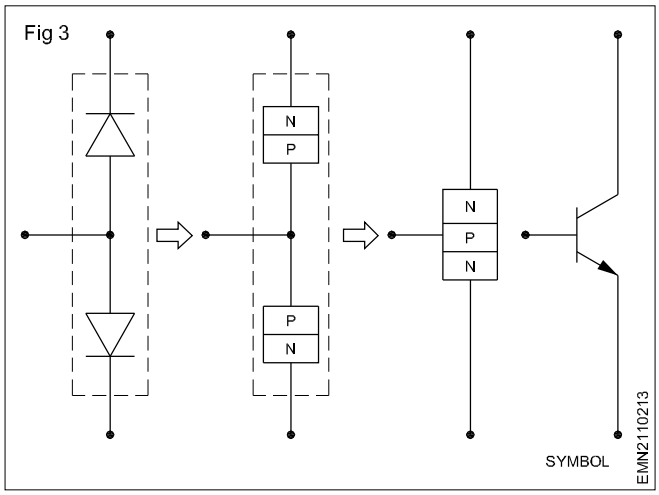


Transistors are mainly used for enlarging or amplifying small electric/electronic signals as shown in Fig 2. The circuit which uses transistors for amplifying is known as a transistor amplifier.

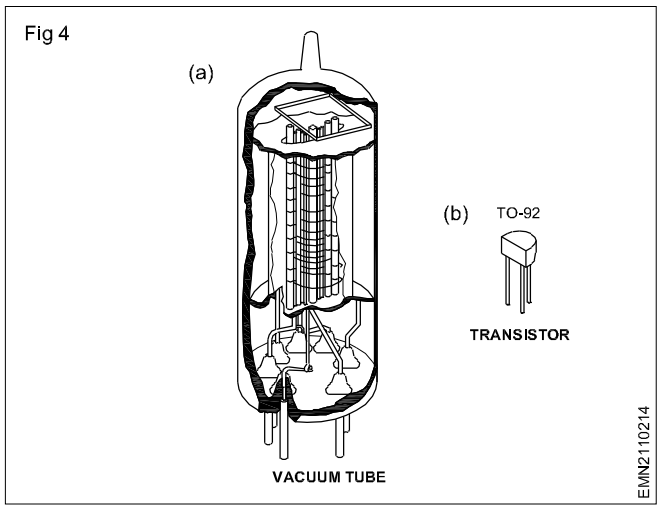


One other important application of transistors is its use as a solid state switch. A solid state switch is nothing but a switch which does not involve any physical ON/OFF contacts for switching.

Transistors can be thought of as two PN junction diodes connected back to back as shown in Fig 3.



Before the transistors were invented (1947), there was what were known as vacuum tubes which were used in amplifiers. A typical vacuum tube is shown in Fig 4a.



Compared with the present day transistors the vacuum tubes were big in size , consumed more power, generated lot of unwanted heat and were fragile. Hence vacuum tubes became absolute as soon as transistors came to market.

Transistors were invented by Walter H. Brazil and John Barlow of Bell Telephone Laboratories on 23rd Dec. 1947. Compared to vacuum tubes (also known as valves), transistors have several advantages. Some important advantages are listed below;

– Very small in size (see Fig 4b)

– Light in weight

– Minimum or no power loss in the form of heat

– Low operating voltage

– Rugged in construction.

To satisfy the requirements of different applications, several types of transistors in different types of packaging are available. As in diodes, depending upon the characteristics, transistors are given a type number such as BC 107, 2N 6004 etc., The characteristics data corresponding to these type numbers are given in *Transistor data books*.

CLASSIFICATION OF TRANSISTORS

1 Based on the semiconductor used.

– Germanium transistors

– Silicon transistors

Like in diodes, transistors can be made, using any one of the above two important semiconductors. However, most of the transistors are made using silicon. This is because, silicon transistors work better over a wide temperature range (higher thermal stability) compared to germanium transistors.

Transistor data books give information about the semiconductor used in any particular transistor.

2 Based on the way the P and N junctions are organized as shown in Fig 5.

– NPN transistors

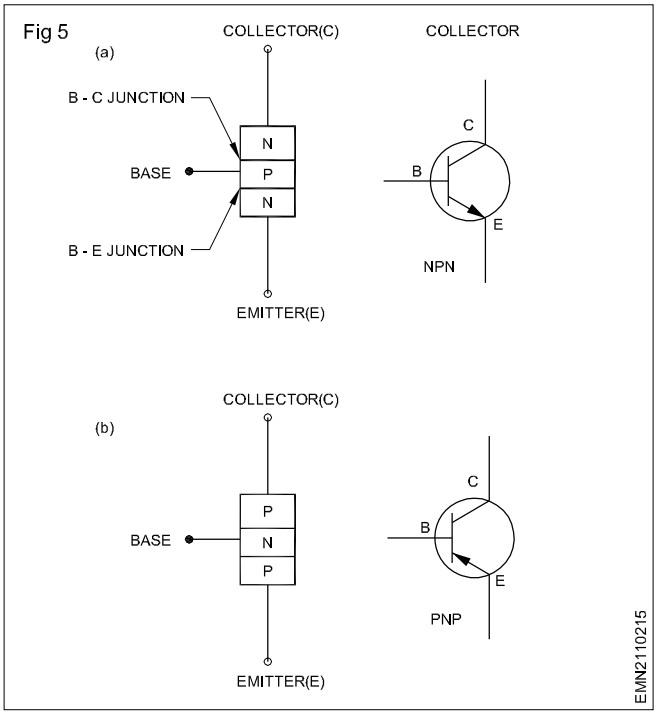
– PNP transistors

Both NPN and PNP transistors are equally useful in electronic circuits. However, NPN transistors are preferred for the reason that NPN has higher *switching speed* compared to PNP.

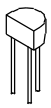
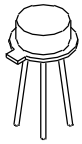
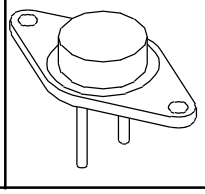
Details of switching speed is discussed in further lessons.

Whether a transistor is PNP or NPN can be found with the help of transistor data book.

Fig 5



3 Based on the power handling capacity of transistors as shown in Table below (Fig 6).

Low power transistors (less than 2 watts)	**Medium power transistors** (2 to 10 watts)	**High power transistors** (more than 10 watts)
Fig 6 TO-92 	TO-05 	TO-03 

Low power transistors, also known as small signal amplifiers, are generally used at the first stage of amplification in which the strength of the signal to be amplified is low. For example, to amplify signals from a microphone, tape head, transducers etc.,

Medium power and high power transistors, also known as large signal amplifiers are used for achieving medium to high power amplification. For example, signals to be given to loudspeakers etc. High power transistors are usually mounted on metal chassis or on a physically large piece of metal known as heat sink. The function of heat sink is to, take away the heat from the transistor and pass it to air.

Transistor data books give information about the power handling capacity of different transistor.

4 Based on the frequency of application

- Low freq. transistors (Audio frequency or A/F transistors)
- High freq. transistor (Radio frequency or R/F transistors)

Amplification required for signals of low or audio range of frequencies in Tape recorders, PA systems etc., make use of A/F transistors. Amplifications required for signals of high and very high frequencies as, in radio receivers, television receivers etc., use R/F transistors.

5 Based on the manufacturing method

- Grown junction
- Alloy junction
- Planar type
- Point contact
- Epitoxial
- Mesa

The aim of each manufacturing process is to yield transistors most suitable for a particular type of application.

Transistor data books generally do not give information about the adopted manufacturing process of transistor. However, the relevant details can be obtained from the transistor manufacturer.

6 Based on the type of final packaging

- Metal
- Plastic
- Ceramic

Metal packaged transistors are generally used in medium and high power amplifications. Plastic packaging is generally used for low power amplification. Some plastic packages come with a metal heat sink. Such transistors are used for medium power amplification. Ceramic packaging is used for special purpose very high frequency applications, for higher temperature stability etc.,

Some examples of packaging type codes used with transistors are, TO-3, TO-92, SOT-25 and so on.

Transistor data books give information about the type of packaging and its case outline.

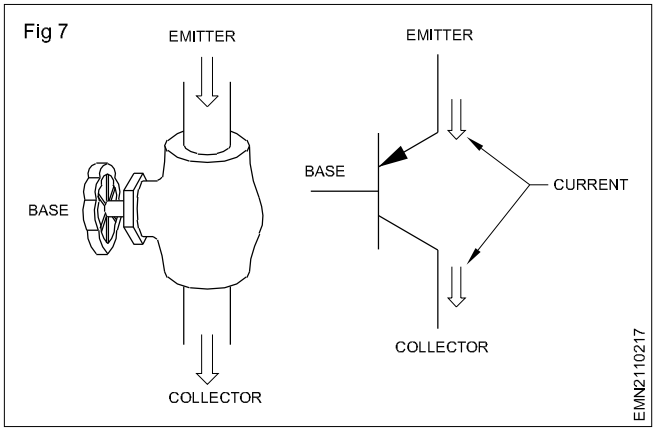
Inside a transistor

Inside a transistor there are two PN junctions connected to each other as shown in Fig 3 and Fig 5. Outside a transistor, one can see only three leads. These leads are known as **base, emitter** and **collector** as shown in Fig 5. As shown in Fig 5, the three leads/pins/pigtails called **base, emitter** and **collector** are taken from each of doped semiconductor material.

In simple terms, as shown in Fig 7, the function of the **base, emitter** and **collector** regions of a transistor are,

Emitter - emits current carriers(electrons/holes)

Fig 7



Collector - collects current carriers

Base - controls flow of current carriers from emitter to collector.

While connecting a transistor to a circuit, it is necessary to identify the base, the emitter and the collector pins. A Transistor data book gives information on pin identification of transistors. However, it is convenient to put sleeve wires over the transistor pins for the following reasons;

- for easy identification while wiring
- sleeves act as spacers while mounting and solder ing
- they ensure the required minimum lead distance from the solder joint to the transistor body.

Following colour scheme is suggested for putting sleeves to transistor pins although, any convenient colour scheme may be adopted.

Base pin - Blue colour sleeve

Emitter pin - Red colour sleeve

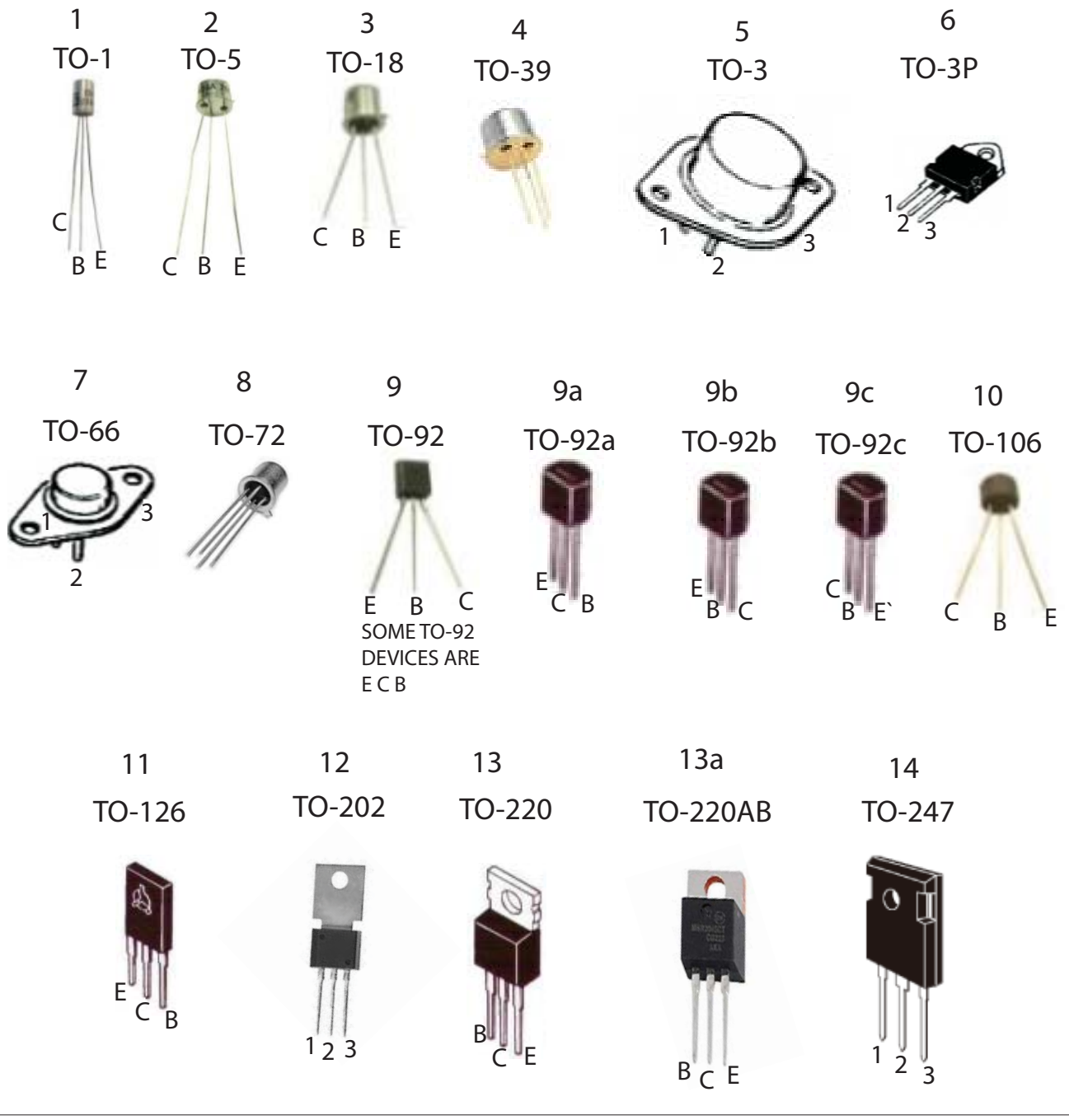
Collector pin - Yellow colour sleeve

Shield pin - Black colour sleeve

TRANSISTOR TYPE PACKAGES:

The popular transistors with different ratings used for general purpose to special applications are manufactured in a variety of package styles.some of the commonly used transistors with their package numbers and lead indentifications are shown in Fig 8.

Fig 8



Heatsink

In any electrical/electronic cirouits the high power rectifiers, SCRs, transistors, MOSFETS, even LEDs used in high bright lights consumes power generates considerable amount of heat while the cicuit is functioning.Typically power handling semiconductor devices/components are inadegquate to dissipate heat as their dissipation capability is significantly low.

Due to this reason, heating up of components leads to malfunctioning problems and may cause failure of the entire circuit or performance of the system. Therefore, to solve these problems, heatsinks are the solution that must be provided to these semiconductor devices for cooling purpose.

Heatsink is a device made of aluminium metal attached to the electronic device, that dissipates heat into surrounding air meduim and cools them for improving their performance reliability and also avoids the damage to the components. Heat sink transfers the heat or thermal energy from a high temperature component to a low temperature medium like air.

Heatsinks are classified into different categories as extruded heatsinks as they can be made as extrusions based on the heat dissipating rating shape and size etc as shown in Fig 9.

To select a particular heatsink various parameters are to be taken into consideration such as heat dissipation rate in heat dissipation ratio of the semiconductor device used

Fig 9

in watts, maximum junction temperature of device in degree celsius, air flow condition etc.

The method of mounting a transistor in To - 220 package is shown in Fig 10. A thin mica film is introduced between the transistor body and the aluminium heatsink surface. An insulating washer inserted to avoid short circuit by the screw and nut used for tightly fastening to the heatsink that radiates the heat generated of the transistor.

Testing transistors using ohmmeter

1 Junction test

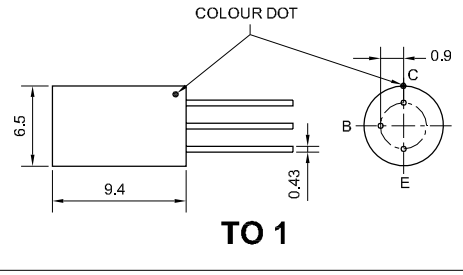
Since a transistor can be regarded as two diodes connected back-to-back, a transistor's general working condition (quick-test) can be assessed by checking these two diodes as shown in Fig 11a and 11b.

Fig 8a shows a NPN transistor and Fig 8b shows a PNP transistor. The imaginary diodes 1 and 2 can be tested as testing any diode. When a diode is tested, if the ohmmeter shows high resistance in one direction and low resistance

CHART - 1

Types of transistor packages and pin identification chart

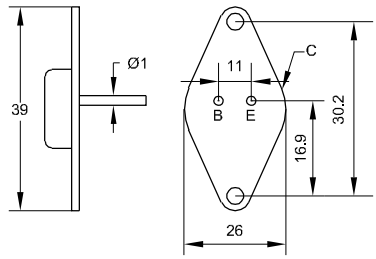
Fig 1



TO 1

EM2201C1

Fig 2

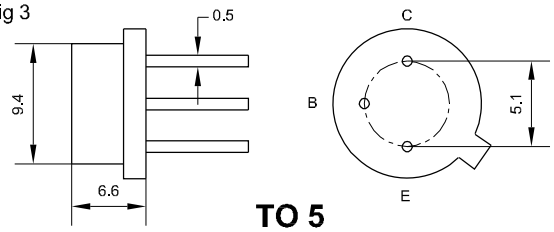


NOTE: BODY OF TRANSISTOR IS THE COLLECTOR

TO 3

EM2201C2

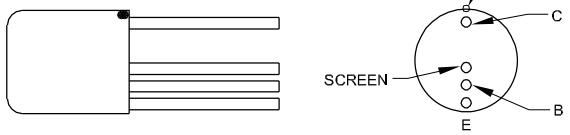
Fig 3



TO 5

EM2201C3

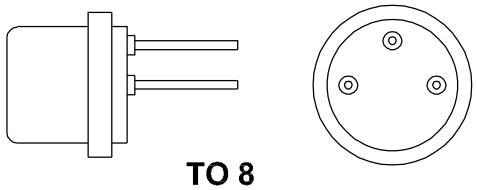
Fig 4



TO 7

EM2201C4

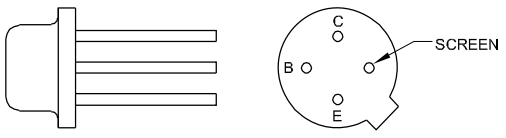
Fig 5



TO 8

EM2201C5

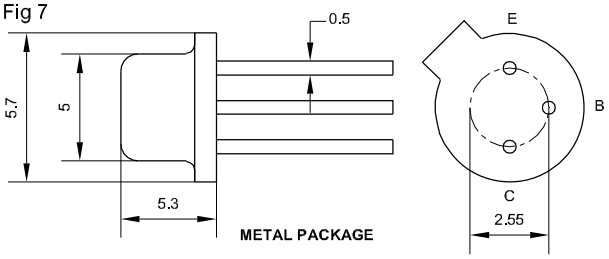
Fig 6

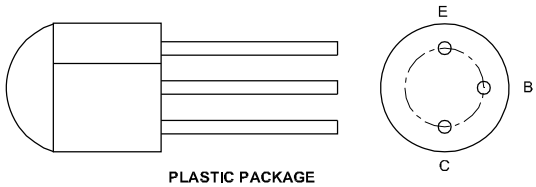


TO 12

EM2201C6

Fig 7



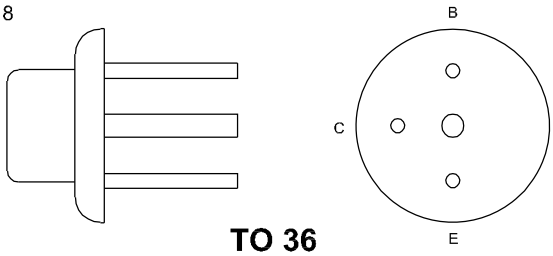


PLASTIC PACKAGE

TO 18

EM2201C7

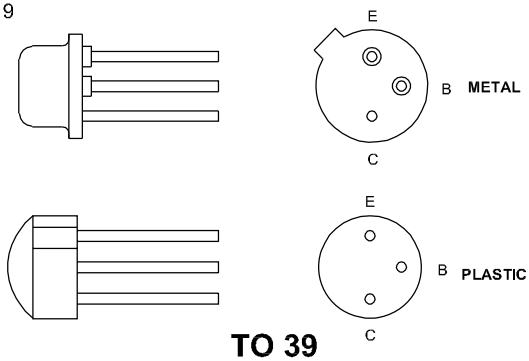
Fig 8



TO 36

EM2201C8

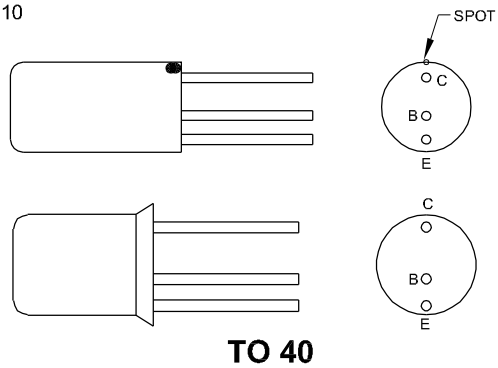
Fig 9



TO 39

EM2201C9

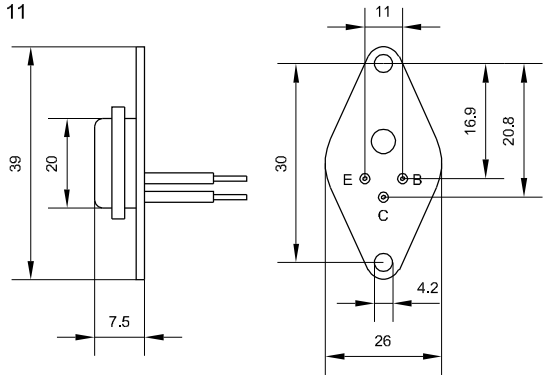
Fig 10



TO 40

EM2201CA

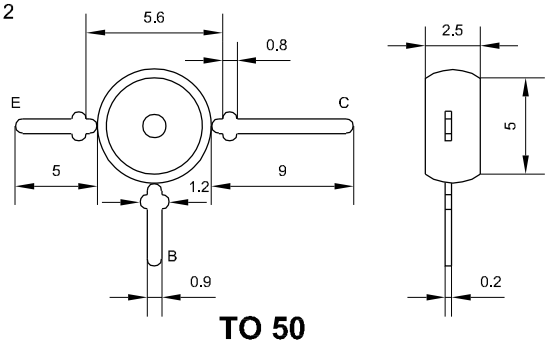
Fig 11



TO 41

EM2201CB

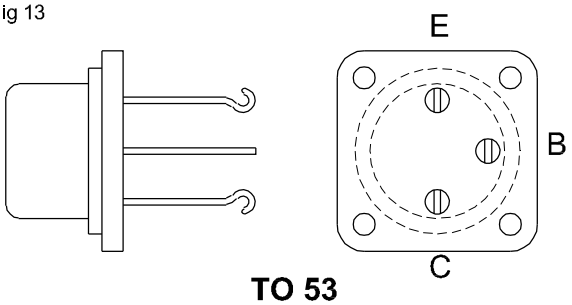
Fig 12



TO 50

EM2201CC

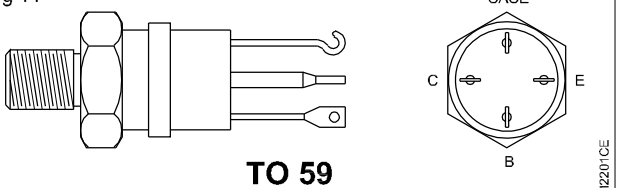
Fig 13



TO 53

EM2201CD

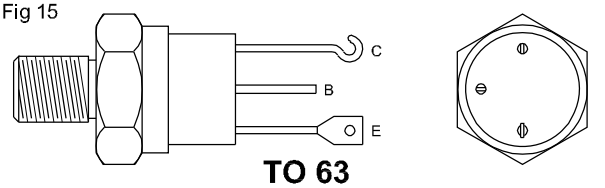
Fig 14



TO 59

EM2201CE

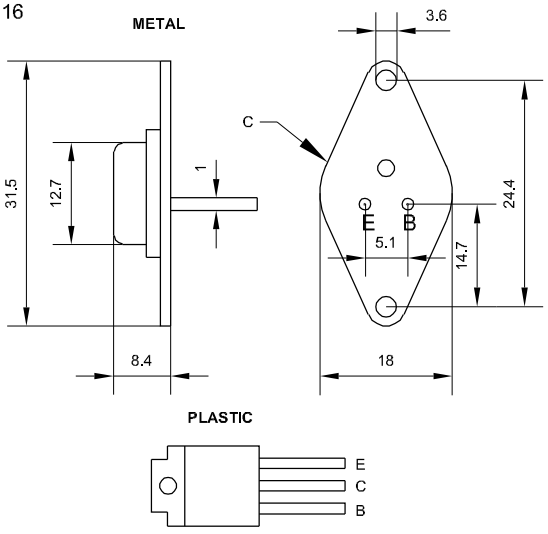
Fig 15



TO 63

EM2201CF

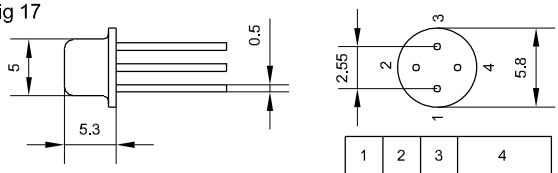
Fig 16



TO 66

EM2201CG

Fig 17

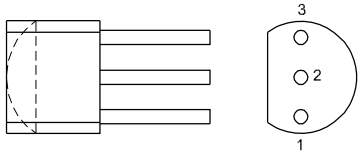


	1	2	3	4
A	E	B	C	CASE
B	B	E	C	CASE
C	D	S	G	CASE
D	S	D	G	CASE
E	S	G	D	CASE

TO 72

EM2201CH

Fig 18

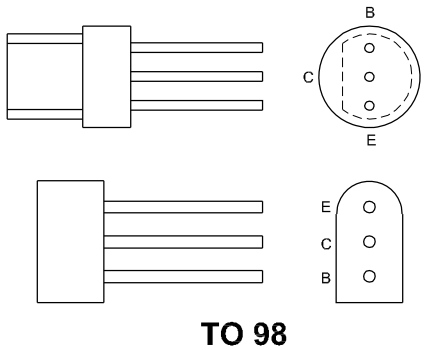


	1	2	3
A	E	C	B
B	E	B	C
C	C	B	E
D	C	E	B
E	S	G	D
F	D	S	G
G	B_2	E	B_1
H	E	B_2	B_1

TO 92

EM2201CI

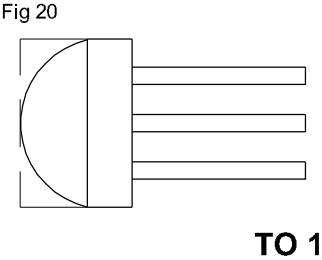
Fig 19



TO 98

EM2201CJ

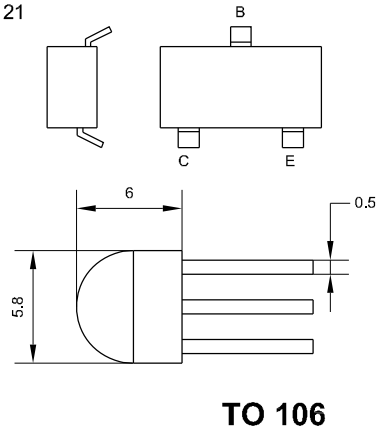
Fig 20



TO 105

EM2201CK

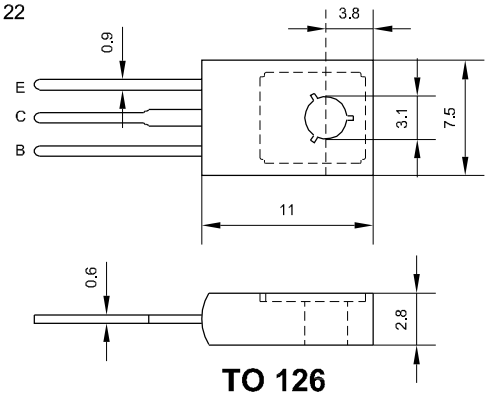
Fig 21



TO 106

EM2201CL

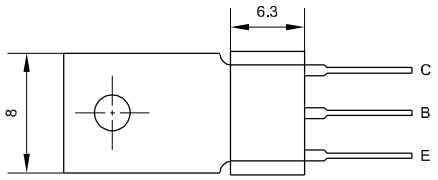
Fig 22



TO 126

EM2201CM

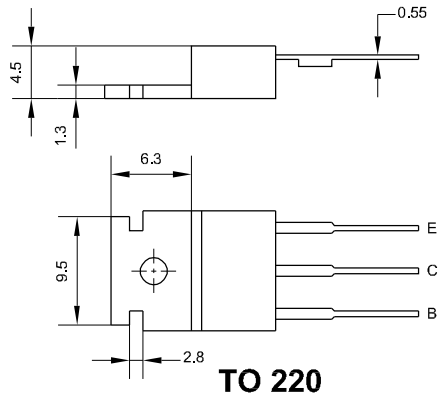
Fig 23



TO 202

EM2201CN

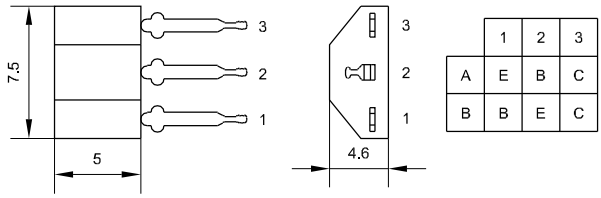
Fig 24



TO 220

IT1A01XO

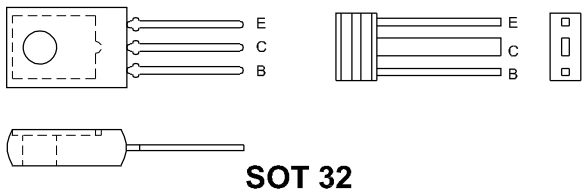
Fig 25



SOT 25

EM2201CP

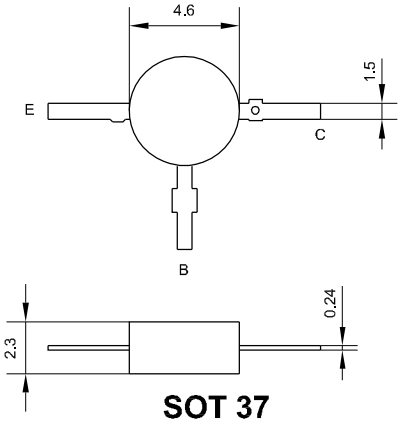
Fig 26



SOT 32

EM2201CQ

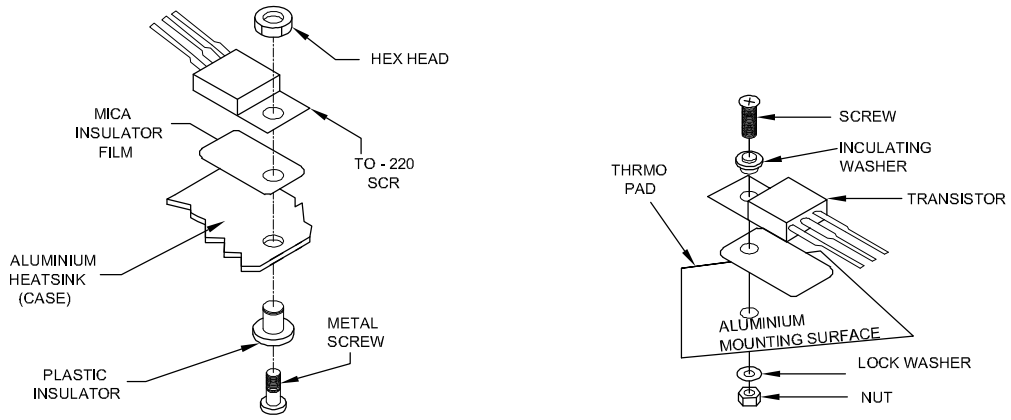
Fig 27



SOT 37

EM2201CR

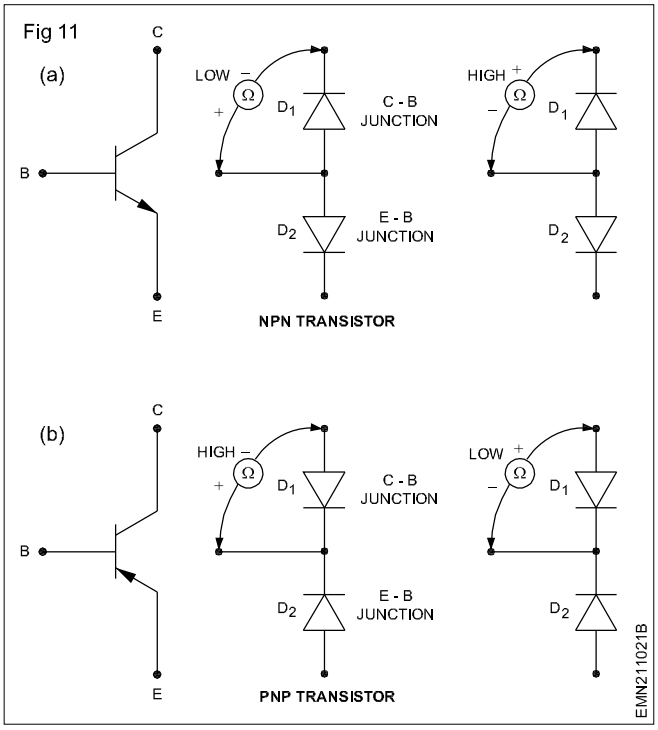
Fig 10



MOUNTING METHOD OF TRANSISTOR ON HEATSINK

in another direction, then the diode corresponding to that diode junction can be regarded as GOOD. One important point to note in a transistor is that, both the diodes of the transistor should be GOOD to declare the transistor as GOOD.

Fig 11



While connecting a transistor to a circuit, it is necessary to identify the base, the emitter and the collector pins. A Transistor data book gives information on pin identification of transistors. However, it is convenient to put sleeve wires over the transistor pins for the following reasons;

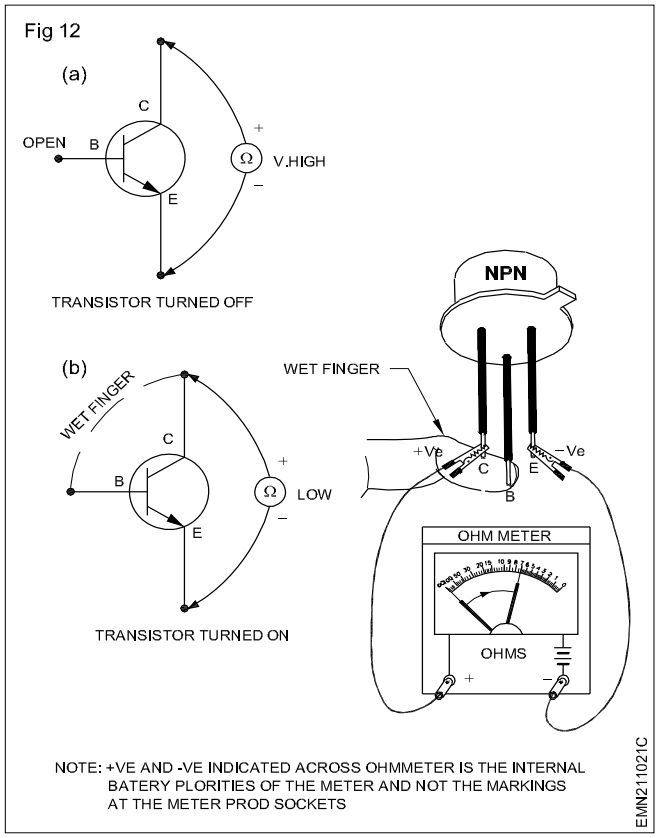
2 Quick TURN-ON test

Recall that the base lead of the transistor controls the flow of current carriers from emitter to collector. So, if the base is open, then there can be no current flow through emitter-collector. This means, the resistance between emitter and collector will be high when the base is open as shown in Fig 12a. This can be checked using an ohmmeter with the base lead open.

In Fig 12, the +ve and –ve indicated across ohmmeter is the internal battery polarities of the meter and not the markings at the meter prod sockets.

When the collector and base leads of a transistor is touched with a wet finger as the base of the transistor turns ON the transistor and makes current to flow through emitter-collector. Because of the current flow, the resistance across emitter-collector will be low. From this test it is possible to make a quick test of the transistors

Fig 12



basic operation. This test is most suitable for low power and medium power transistors.

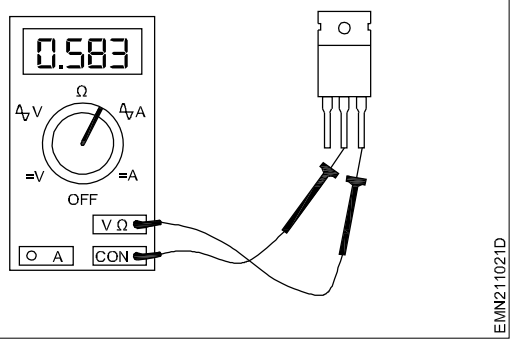
The above two tests on a given transistor, using a simple ohmmeter revels the condition of the transistor. These tests are essential before using a transistor in a circuit.

Testing transistor using DMM

Electronics repair technicians often uses a digital multmeter (DMM) to test whether a transistor is working in fig 14. properly or not (serviceable or unservicecable). The DMM is shown simple test with DMM function/ range switch set at the diode symbol (Diode tesst mode) is used for this purpose.

There are three set of testing across the base to Emitteer, base to collector and Emitter to collector terminals both in forward and reverse directions as shown in Fig 14. are to be carried out to determine the condition of any transistor.

Fig 13



As the transistor is considered to be junction of two - back - to - back diodes, in this test, the DMM measures the voltage drop across the base to Emitter and base to collector in both directions. The readings of common type of small signal type normal working (Serviceble) silicon NPN transistor is given in the table below as a reference.

Direction	Base to Emitter	Base to collector	Emitter to collector	Remarks
Forward	0.45v to 0.9v	0.45 to 0.9v	'OL'	serviceable
Reverse	'OL'	'OL'	'OL'	

Incase the bipolar transister measures contrary to these readings it is considered to be defective. Also, with the voltage drop readings it is possible to determine the emitter lead of an unknown/unmarked transistor, as the emitter - base junction typically has a shightly higher voltage drop than the collector- base junction.

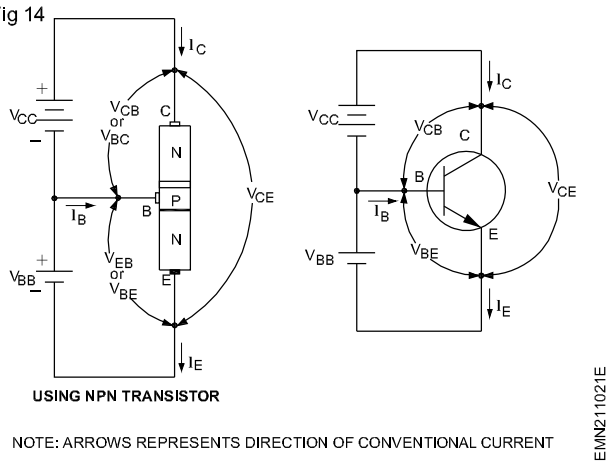
Thus, this test is used only to verify whether the transistor is serviceasle or rot, but it doesnot guarantee that the transistor is operating within its designated parameters.

Transistor data from transistor data book

Introduction

Voltage across the junctions and current through the base, collector and emitter in a transistor are symbolically represented as shown in Fig 1. The direction of current arrows shown in Fig 1 corresponds to the direction of conventional current.

Fig 14



Similar to diodes, at the contact region of each P-N junction, there are depletion regions. The depletion is at the region forward biased base-emitter junction and wide at the reverse biased base-collector junction.

1 Maximum permissible emitter-base voltage, $V_{EB(max)}$ or $V_{BE(max)}$

Recall from the lesson of P-N junction diodes, that the forward bias voltage required to set a PN junction into conduction is 0.7volts for silicon and 0.3 volts for germanium. Any further increase in forward bias voltage across the PN junction increases only the current through the junction. If an excessively large forward voltage is applied across a P-N junction, the junction ruptures resulting in short circuit of the junction. Then, the P-N junction no more behaves as a PN junction. Hence, while applying forward voltage across a P-N junction, the maximum permissible voltage limit should not be crossed.

In a transistor, the forward voltage across the base-emitter PN junction is referred to as V_{EB} or V_{BE}. The maximum value of V_{EB} that can be applied across this junction is indicated as $V_{EB(Max)}$. If the applied voltage across E-B junction, exceeds $V_{EB(Max)}$, the junction will rupture and the transistor will become defective.

The value of $V_{EB(Max)}$ is different for different transistors. This specification for any particular transistor can be obtained from transistor data books. As an example $V_{EB(max)}$ of a few transistors are given below;

Transistor type number	BC147	BC148	BC180	BF200
$V_{EB(max)}$	6V	5V	3V	3V

The terms $V_{EB(max)}$ and $V_{BE(max)}$ are the same

2 Maximum permissible collector-base voltage, $V_{CB(max)}$ or $V_{BC(max)}$

When a P-N junction is reverse biased, the junction does

not conduct. If the applied reverse voltage is increased beyond a limit, the junction ruptures and the junction starts conducting like any conductor losing is original property. This maximum permissible reverse voltage that can be applied across the collector-base is indicated by $V_{CB(max)}$ or $V_{BC(max)}$. This value is different for different transistors. This value for any particular transistor can be obtained from transistor data book. As an example $V_{CB(max)}$ for a few transistors are given below;

Transistor type number	BC147	BC148	BF170	BF200
$V_{CB(max)}$	50V	30V	160V	30V

3 Maximum permissible Collector-Emitter Voltage, $V_{CE(max)}$

This is the maximum voltage that can be applied across the collector-emitter junction of a transistor. Beyond this voltage both the base-emitter and the base-collector junction will get damaged. $V_{CE(max)}$ is also different for different transistors. $V_{CE(max)}$ for any particular transistor can be obtained from transistor data book. As an example $V_{CE(max)}$ for a few transistors are given below;

Transistor type number	BC147	BC148	BF170	BF200
$V_{CE(max)}$	45V	20V	160V	20V

4 Maximum permissible collector current, $I_{C(max)}$

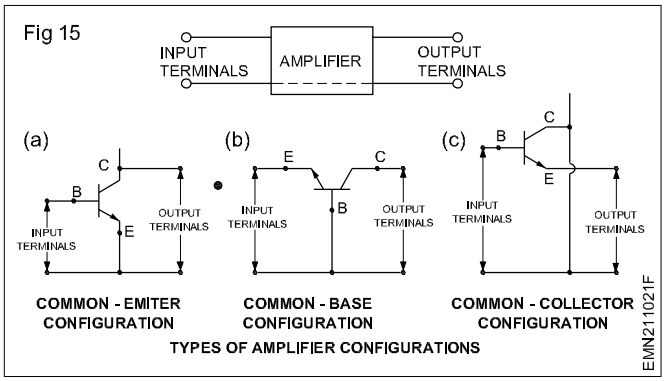
This is the maximum current that can be forced to flow through the collector region of a transistor. If current higher than this limit is forced the collector, the transistor will get heated up excessively and eventually burn out. This specification $I_{C(max)}$ of a transistor indicates whether the transistor is low, medium or a high power transistor. $I_{C(max)}$ of any particular transistor can be obtained from transistor data book. $I_{C(max)}$ for a few transistors are given below;

Transistor type number	BC547	BC548	BF170	BF200
$I_{C(max)}$	200mA	200mA	50mA	20mA

5 Minimum DC current gain, b_{dc} or H_{FE}

The current gain of a transistor is a ratio of the output current to the input current. A transistor can be connected in three different ways as shown in Fig15.

Fig 15a is referred to as **common-emitter configuration** or common-emitter amplifier. This is because, the emitter lead of the transistor is used as a common terminal between the input and output. Common emitter amplifiers are the most commonly used amplifier configuration in electronic circuits. This is because, in this configuration, you get the best out of a transistor. Details of common emitter configuration are discussed in further lessons. The **current gain** in common-emitter configuration is indicated by the symbol β (spell it as Beta). All data books



give the current gain of transistors in β. This is because, once β of a transistor is known, the current gain of the transistor when connected in other configurations as shown in Fig 15b and Fig 15c can be easily computed.

The value of b given in data books is generally the current gain calculated as a ratio of, a small change in DC base current (DI_B) to a corresponding change in the DC collector current (DI_C).

Hence, a suffix DC is attached to the term b and given as β_{dc} in data books. β_{dc} of transistors is also referred to as H_{FE} in some data books.

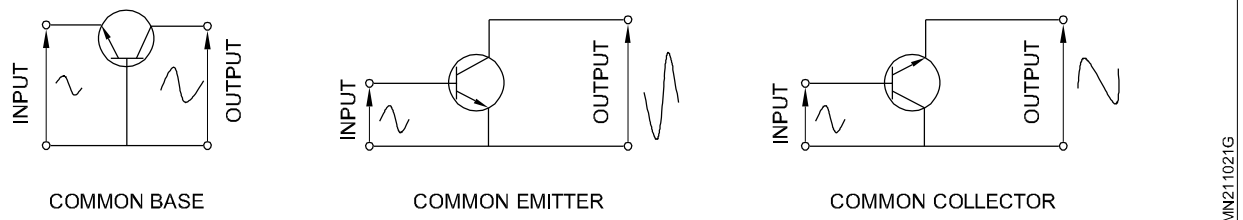
Fig 15b shows a **common-base amplifier**, where the base lead of the transistor is common to both the input and output terminals. The current gain in common-base configuration is indicated by the symbol α (spell it as alpha). The current gain α, of a common-base amplifier will always be less than 1. Although the current gain of this amplifier is very low, this configuration is preferred over the common emitter configuration in some special amplifiers. Details of common-base amplifiers are discussed in further lessons.

Fig 15c shows a **common-collector amplifier**, where the collector lead is common to both the input and output terminals. This common-collector configuration is also known as **emitter-follower** because, voltage at the emitter lead follows the voltage given at the base of the transistor. The current gain in a common-collector amplifier is not very much different from that of the common-emitter amplifier. Hence, no separate symbol is used to indicate the current gain of a common-collector amplifier. This configuration is as important and as popular as the common-emitter configuration because, it is used to interconnect circuits having different impedances. Details of this circuit are discussed in further lessons.

It is very important to note that the β of a transistor is given in data books as β Minimum(MN) or β Typical(TP). This is because the value of β varies due to variations in the level of the base current. Details of variation in β is discussed in detail in further lessons. While designing a circuit, it is suggested to use the typical value of β of the transistor. If the data book gives only the minimum value of β, the typical value can be taken as twice the minimum value.

Characteristics	Common base	Common emmiter	Common collector
Input resistance	Very low (less than 100ohm)	Low (less than 2K)	High (above 100k ohm)
Output resistance	Very high (more than 100k ohm)	High (less than 50k ohm)	Low (less than 100 ohm)
Current gain	Less than one	High (about 100)	Very high (above 100)
Voltage gain	Medium	High	Medium
Phase relation between I/P and O/P	In phase	180 phase shift (invert or phase)	In phase
Applications	High frequency applications for more	Audio frequency application	Impudence matching

Fig 16



6 Typical application of a particular type of transistor

Transistor applications are almost infinite. However, these applications can be broadly classified as given below;

– Industrial circuit applications

– Consumer circuit applications

– Special purpose circuit applications

Under each of the above classification, there may be one or more further classifications. Transistor data books give these details as appendix to the data book. Data books generally adopt some form of symbolic coding scheme under the column *use/appln* to indicate the application of a particular transistor. Meanings of the codes will be given in the appendix of the data book.

For example, in Towers International Transistor Selector Data Book, for the transistor 2N 6004, under the column USE the codes mentioned is AMG. This means 2N6004 is,

A - Audio frequency transistor

M - Medium current rating

G - General purpose applications

From this code, we can conclude that the transistor 2N6004 is used for general purpose amplifier circuits in the audio frequency range for medium current/power application.

Important specifications that go along with any transistor, can be summarised as follows;

– maximum permissible emitter-base voltage, $V_{EB(max)}$ or $V_{BE(max)}$

– maximum permissible collector-base voltage, $V_{CB(max)}$ or $V_{BC(max)}$

– maximum permissible collector-emitter voltage, $V_{CE(max)}$

– maximum permissible collector current, $I_{C(max)}$

– minimum or typical dc current gain, b_{dc} or H_{FE}

– typical application of the transistor.

In addition to the above listed specifications, there are a few more specifications for transistors. These specifications will be introduced at the appropriate place in further lessons.

Transistor type numbering scheme

The transistor type numbering scheme follows the same PRO-ELECTRON(European), JEDEC(American), JIS(Japan) and House codes (particular to the manufacturer) standards as used for diodes.

Transistors in Pro-electron standard are registered with,

– two letter and three numeral codes or

– three letter and two numeral codes.

A few examples of,

– Two letter and three numeral codes are, AC128, BC107, BF200 etc.

– Three letter and two numeral codes are, ACY17, BCX73 etc.

Two letter and three numeral codes

The first letter in the type number of the device indicates,

the type of semiconductor material used in making the device.

Example: Device numbers starting with B are made of Silicon.

The second and third letters indicate the general applications of the component.

Example: In transistor type code BC107, the second letter C indicates that it is a low power audio frequency transistor. Table No.28 of pocket table book gives further details of pro-electron codes for transistors.

The three digit numerals after two or three letters is the registration code number which corresponds to the detailed voltage, current and temperature specification of that transistor. This detailed specification can be obtained referring to data book.

Three letter and two numeral code

If the transistor has a three letter and two numeral code, then the first two letters carry the same meaning as given in the above example. The third letter indicates that the device is manufactured for a specific field of application.

For example: BCY98 indicates that it is a silicon, audio/ low frequency, low power, industrial transistor.

In Jedec(USA) standard transistor type numbering scheme, the first numeral gives the number of PN junctions in the device. For example 1 for diodes as they have only one PN junction and 2 for conventional bipolar transistors as they have two PN junctions. This first numeral is followed by the letter N and a register number. For example a device numbered 2N6004 indicates that, it is a device with two junctions (transistor) which was the 6004th to be registered in the standards. The detailed specification for the registered number can be found referring to transistor data book.

In JIS (Japan) standard transistor type numbering scheme, all transistor numbers start with 2S followed by a letter and several numbers(e.g. 2SB77). The letter after S has the following significance,

A = PNP transistor for high frequency application

B = PNP transistor for low frequency application

C = NPN transistor for high frequency application

D = NPN transistor for low frequency application

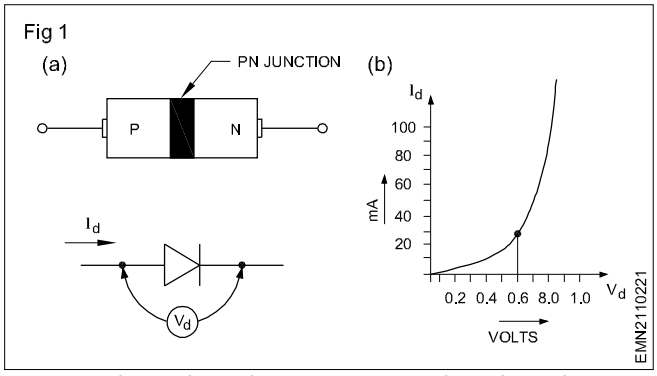
Manufacturers who cannot manufacture transistors which satisfy the full detailed specification of any of the above said standards employ their own coding scheme. Such coding schemes are known as **House codes** and they are particular to individual manufacturers. One such House code maintained by, The **S**emiconductors **L**td., Poona, has house code such as SL100, SG100 etc.

Transistors Input and Output Characteristics of Transistors

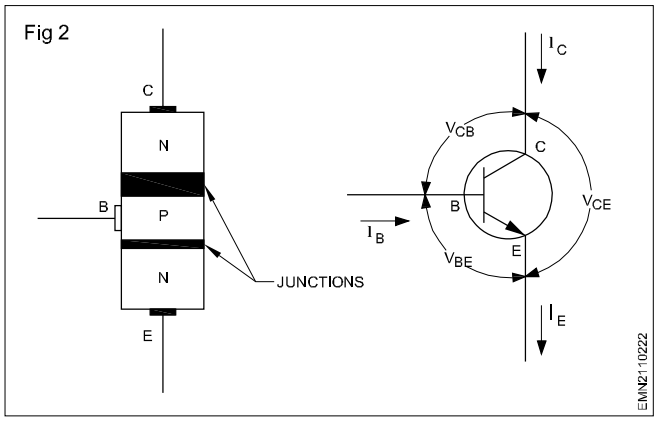
Objectives: At the end of this lesson you shall be able to

- **state the necessity of characteristic curves for transistors**
- **list and explain the two important characteristic curves of transistors**
- **define voltage and break down voltage**
- **state the importance of DC load line curves**
- **state the meaning of Q-point**
- **state the method of fixing Q-point for a given transistor using the transistor data.**

A semiconductor diode, as shown in Fig 1, has only one PN junction. When the voltage across the PN junction is increased or decreased, the current through the diode increases or decreases. There is only one voltage parameter(V_d) and one current parameter(I_d). Therefore, the relationship between these two parameters is easy to understand through the diode characteristic graph of V_d versus I_d as shown in Fig 1b.



In a transistor since there are two PN junctions there are three voltage parameters V_{BE}, V_{BC}, V_{CE} and three current parameters I_B, I_C, I_E, as shown in Fig 2.



Any change in any one parameter causes changes in all the other parameters. Hence it is not very easy to correlate the effect of one parameter with the others. To have a clear understanding of their relationship a minimum of two characteristics graphs should be plotted for any transistor. They are,

– Input characteristics

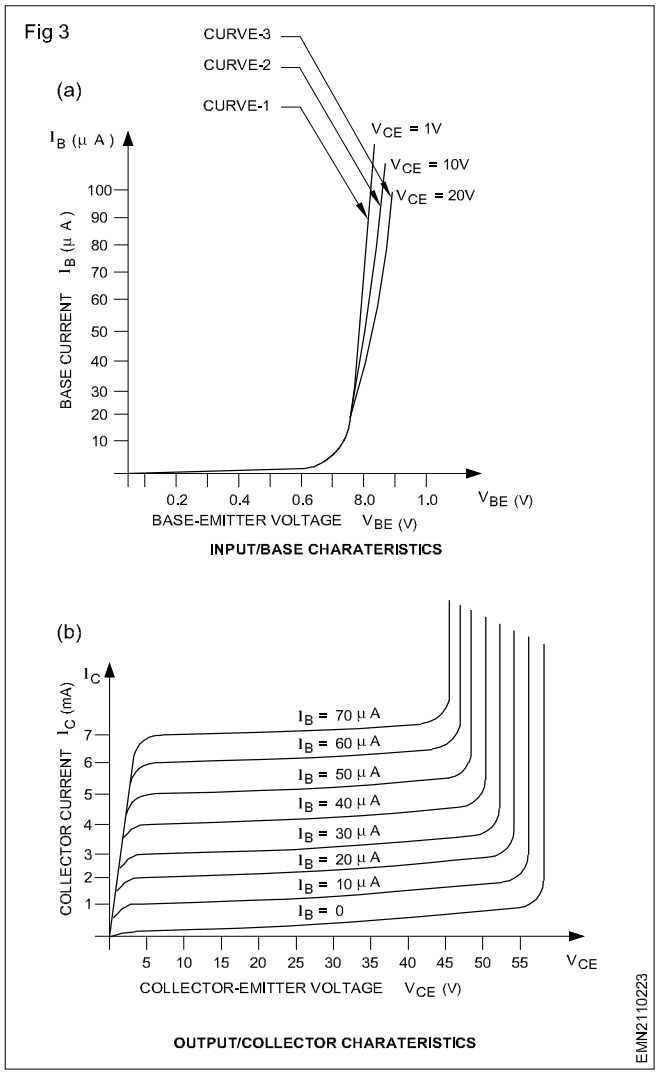
– Output characteristics.

For simplicity in understanding, consider a common-emitter amplifier. The two characteristics graphs are shown in Fig 3.

Input characteristics or Base characteristics

The graph at Fig 3a shows the relationship between the input voltage V_{BE} and input current I_B for different values of V_{CE}.

Since the base-emitter section of a transistor is nothing but a diode, the graph resembles a diode curve as in Fig 1b. But, it is important to note that in Fig 3a, there is a diode curve for each value of the collector-emitter voltage V_{CE}.



While plotting the diode curve 1 of Fig 3a, the value of V_{CE} was maintained constant at 1V. In curves 2 and 3, the value of V_{CE} was increased and hence the path of the curve becomes different.

Why does this happen? The answer is, because of the higher collector voltages, the collector gathers a few more electrons flowing through the base-emitter. This reduces the base current. Hence, the curve with higher V_{CE} has slightly less base current for a given V_{BE}. This phenomenon is known as Early effect.

The gap shown between the curves in Fig 3a is very small. In practice, this gap will be so small, sometimes not even noticeable.

Plotting input/base curves of any given transistor

Necessary data for plotting the input or base characteristics can be obtained by constructing a simple test circuit as shown in Fig 3.

In this test circuit, V_{CE} is set to the required value by adjusting the voltage source V_{CC}. A resistor is introduced in the collector of the transistor to prevent excessive current in the collector which may damage the transistor.

The base-emitter voltage V_{BE} can be set by adjusting the potentiometer. An additional resistor is introduced in series with the DC supply V_{BB} and the POT only to limit the voltage across V_{BE}, and hence, the base current.

Output characteristics or Collector characteristics

The graph at Fig 3b, shows the relationship between the output voltage V_{CE} and output current I_C for different values of I_B.

For simplicity in understanding, consider one of the curves of Fig 3b for a particular value of I_B as shown in Fig 4.

Fig 4 shows the collector characteristics for a constant I_B of 10μA. Behavior of I_C for different values of V_{CE} is explained below;

– When V_{CE} is 0, the collector-base diode is not reverse-biased. Therefore, the collector current is negligibly small.

– For V_{CE} between 0.7V and 1V, the collector diode gets reverse-biased. Once reverse biased, the collector gathers all the electrons that reach its depletion layer. Hence the collector current rises sharply and then becomes almost constant.

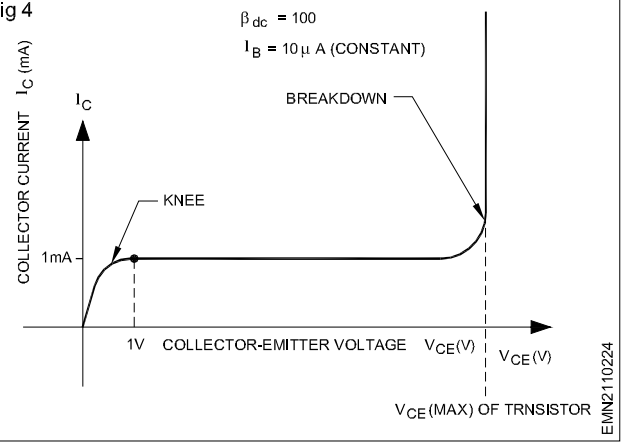
– Above the knee voltage and below the break down voltage, the collector current does not rise steeply or the current is almost constant even if the value of V_{CE} is increased. Thus the transistor works like a controlled constant current source in this region.

– Assuming that the transistor has a β_{dc} of approximately 100, the collector current is approximately 100 times the base current as shown in Fig 4 (1mA is 100 times 10 μA).

– If V_{CE} is further increased, beyond the break down level, $V_{CE(max)}$, the collector-base diode breaks down and normal transistor action is lost. The transistor no longer acts like a current source. As the collector-base gets ruptured, the junction is shorted and hence current increases rapidly above the break-down point as shown in Fig 4.

If several curves for different I_B are drawn on the same graph, the collector curves look like what is shown in Fig 3b.

Fig 4



Since the assumed β_{dc} of the transistor was approximately 100, the collector current is approximately 100 times greater than the base current at any point in the active region. These curves are sometimes called as *static* collector curves because DC currents and voltage are being plotted.

In Fig 3b, notice that at the bottom most curve, eventhough the base current is zero, a small collector current exists. This is because of the leakage current of the collector diode. For silicon transistors this leakage current is so small that it can be almost ignored.

In Fig 3b, also note that the break down voltages become lower at higher currents. This means that the base-emitter voltage from *knee* point till the *break down*, known as the voltage compliance of a transistor, decreases for larger collector currents. Hence, it is necessary to avoid very high collector current such that the transistor operates in a wider active region.

Generally transistor data sheets/books do not show collector curves of transistors. To see the collector curves of a particular transistor, an instrument known as *curve tracer* is used. This instrument looks similar to an oscilloscope. It displays collector curves similar to those shown in Fig 5.

If different transistors are tried on the curve tracer, you will notice changes in knee voltage, β_{dc}, breakdown voltage, etc.

TIP: Two transistors of the same type number (e.g. 2N6004) may have a wide variation in the collector curves.

Fig 5

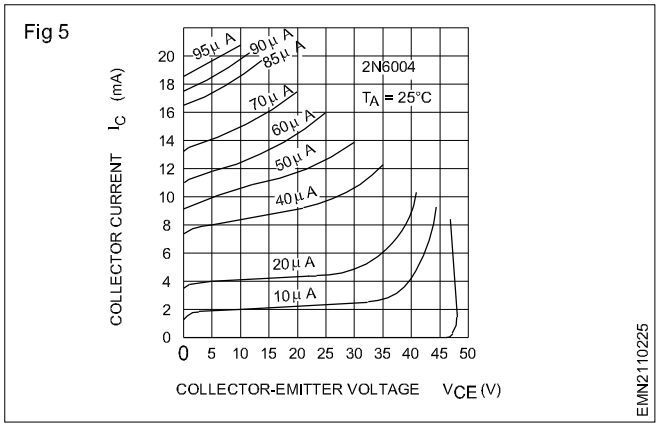
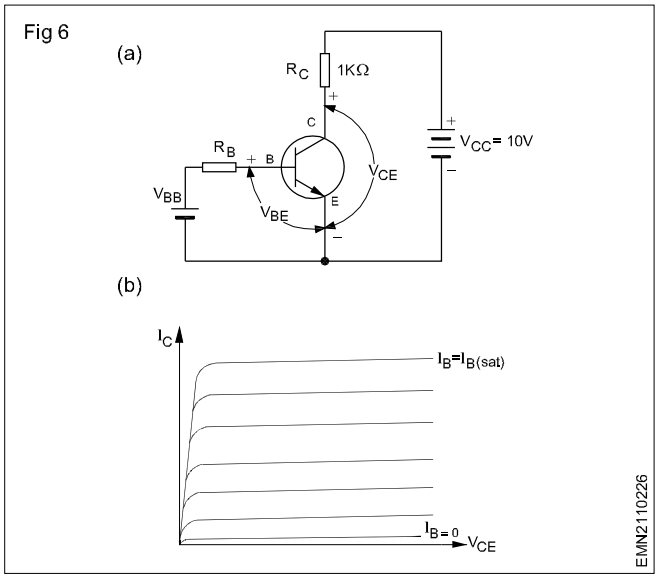


Fig 6



The collector curves are very important because, from these curves the following important information required while designing an amplifier circuit using a particular type of transistor can be obtained;

– DC current gain β of the transistor at different set DC values of I_B and V_{CE}.

– Maximum value of V_{CE} that can be applied for a set value of I_B and I_C.

– Maximum value of I_C that can be made to flow for a set value of I_B.

DC LOAD LINES of transistors

To have a further insight into how a transistor works and in what region of the collector characteristics does it work better can be found using DC load lines.

Consider a forward biased transistor as shown in Fig 6a. Fig 6b shows the collector characteristics of the transistor used.

In the circuit at 6a, consider the following two situations,

– Maximum collector current, $I_{C(max)}$

– Minimum collector current, I_C

For situation (1), assume that V_{CE} is zero or collector-emitter is a short. In that case, the collector current is limited only by the collector resistor R_C. Therefore,

$$I_C = \frac{V_{CC}}{R_C} \text{ at } I_{CE} = 0$$

Under such a condition, for the circuit at Fig 6a, I_C will be equal to 10V/1KΩ = 10mA.

Mark this I_C = 10mA point along V_{CE} = 0 on the collector characteristics of the transistor as shown in Fig 7a.

For situation (2), assume that V_{CE} is maximum or collector-emitter is open. In that case, the collector current is zero.

Therefore,

$V_{CE} = V_{CC}$ In the circuit at 6a, $V_{CE} = V_{CC} = 10V$

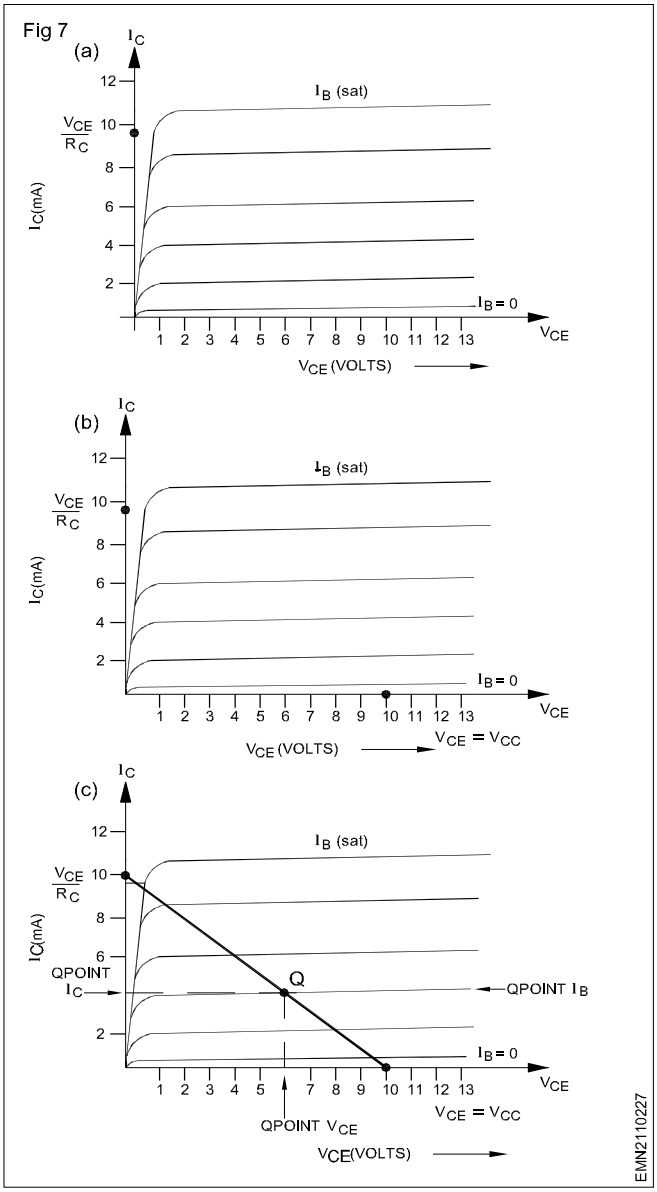
Mark this point of $I_C = 0$ and $V_{CE} = 10V$ on the collector characteristics of the transistor as shown in Fig 7b.

Connect the two marked points through a straight line as shown in Fig 7c. This line is called the load line.

The point at which the load line intersects the $I_B = 0$ is known as the cut off point. At cut off, $I_B = 0$; hence, emitter diode is out of forward bias and the transistor action is lost.

The point at which the load line intersects $I_B = I_{B(sat)}$ is called the saturation point. At this point the base current is maximum and the collector current is also maximum. At saturation, the collector diode comes out of the reverse bias, and hence, the normal transistor action is lost.

For a transistor to work in a normal way, i.e. as a controlled current source, it must not be made to work either in the cut off or in saturation. Therefore the ideal point would be somewhere in the middle of these extreme points on the load line. This middle point is known as *Quiescent point or* Q-point as shown in Fig 7c.



Knowing the Q point, you can fix-up the value of resistors R_C and R_B of the circuit.

The DC load line shows at a glance the active V_{CE} voltage range of the transistor. In other words, it indicates that the transistor acts like a current source anywhere along the DC load line, excluding the saturation or cut off, where the current-source action of the transistor is lost.

Fixing Q point from the data available in data sheets

The Q point can be fairly accurately fixed from the data of a transistor given in transistor data books. This reduces the time consuming work of plotting the collector characteristics and the load line. To do so, the following points are very important to remember;

1 The chosen V_{CC} must be less than $V_{CE(max)}$ given in the data book

TIP : Preferably restrict value of V_{CC} to 3/4 of $V_{CE(max)}$

2 Fix the Q point I_C at 1/2 of $I_{C(max)}$ given in the data book.

3 At the Q point assume 1/2 of V_{CC} will be across V_{CE}.

4 From points (2)&(3) calculate the value of R_C.

5 From the H_{FE} value given in data book, fix the approximate value of the base current at the Q point as given below.

I_B at Q point =

$$\frac{\text{Chosen value of } I_C \text{ at the Q} - \text{point(tipno.2)}}{\text{Typical value of } H_{FE} \text{ from data book}}$$

6 From the value of I_B at the Q point and allowing a 0.7 volts drop across the base-emitter, calculate the value of R_B.

Application of a Transistor as Switch

Objectives : At the end of this lesson you shall be able to
- **explain the function of the transistor**
- **explain the operation of a transistor as a switch**
- **describes the operation of a transistor switching circuit**
- **state the application of transistor switch.**

The function of a transistor at cut-off condition: the transistor is operation at cut-off condition when the emitter and collector junction are both reverse biased

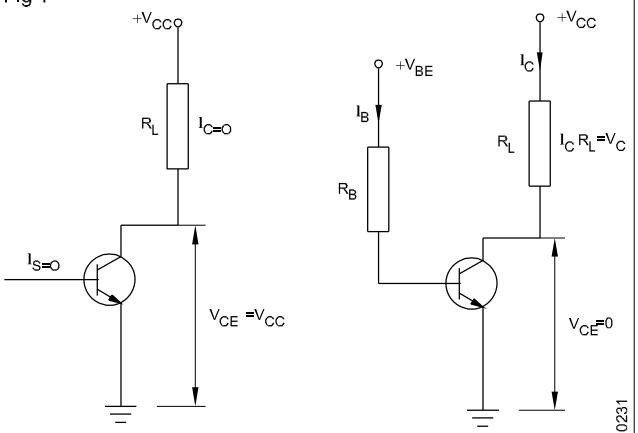
Consider the circuit in Fig 1

$V_{ce}=V_{cc}-(I_c*R_l)$……..(1)

Since $I_b=0$ and $I_c=0 V_{ce}=V_{cc}$

The transistor is said to be cut off for the simple reason that it does not conduct any current as in fig 1a.this corresponds to a switch in an open state, therefore a transistor at cut off is said to be open state.

Fig 1



The function of a transistor at a saturation condition: The transistor is operated at a saturated condition when both the emitter and collector are in forward bias.

In fig 1b if the value of R_b and R_l are such that V_{ce} tends to zero, then the transistor is said to be saturates. Putting $V_{ce}=0$ in the eqn (1) we get

$V_{ce}=0=V_{cc}-I_cR_l$ or $I_c=V_{cc}-R_l$

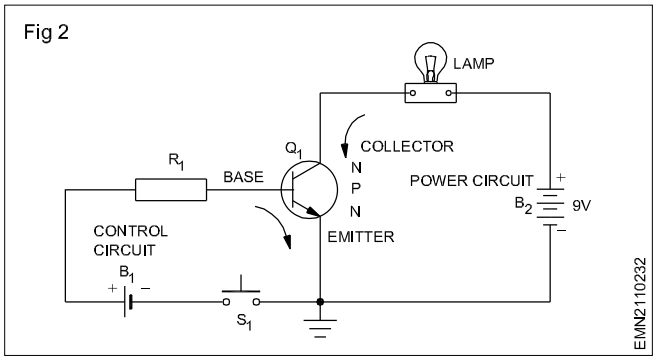
The operation of a transistor as a switch: The switch action for Q_1 in fig. 2 illustrated how the output current can be conducted at the input .note the following importance operating characteristics.

- transistor is normally off without output current unless forward voltage is applied in the base emitter circuit
- the forward voltage controlling the base current mines the amount of output current

In fig 2 the control circuit of the input determines the base current determines the amount of output current.

In fig 2 the control circuit of the input determines the base current. For the power circuit the output is the collector current. An NPN transistor is used for Q_1.the emitter is common to both (a) the current circuit at the input and (b) the power output circuit

Fig 2



The base emitter junction of Q in fig 2 can be forwards biased by the battery B_1.Switch S_1 must be closed apply the forward voltage. reverse polarity means that the N collector is more positive than base, with switch S_1 open ,no current flow in base emitter .The reason is that the forward voltage is not applied .therefore the resistance of the emitter to the collector of the transistor is very high. No current flows in the power circuit and the lamp does not glow.

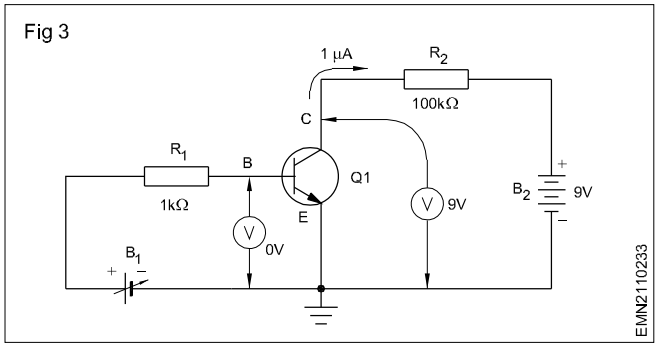
Next assume that switch that S_1 is closed this cause a small change in current flow in the control circuit .R is the current limiting resistor for the base current. Therefore the resistance from the emitter from the collector for the transistor drops. Consequently a large current flow in the power circuit causing the lamp to glow.

Operation of transistor switching circuit: The schematic circuit in the fig 3 shows the measured voltage and collector current Ic in the 'transistor OFF' condition. Note that only a tiny leakage current of 1micro amp flow from the emitter to collector. The resistance from E to C is calculated as

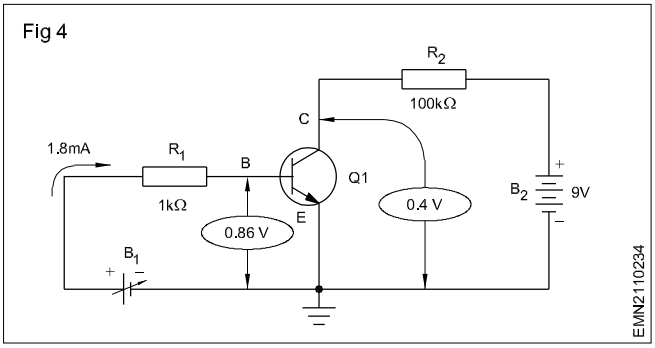
R=V/I=9V/0.000001A=9 M Ω

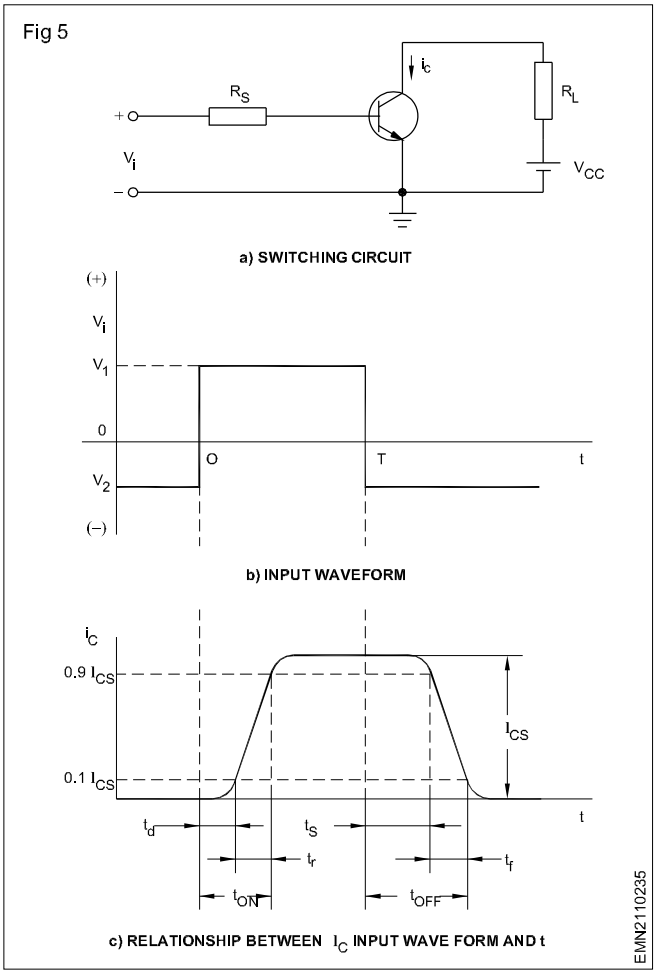
The transistor has a resistance of 9 mega ohms, which is like the open or off condition of a switch

Fig 3



The fig 4 shows the measured voltage and current in the 'transistor ON condition. First, the voltage from the emitter to the base has been increased by adjusting B1,The forward –biased voltage of 0.86V at the emitter-base junction of the transistor cause the resistance of the transistor from E to C drop this resistance from E to C is calculated as





R=V/I=0.4V/0.085A=4.7 ohms

The transistor in fig 4 is said to be at saturation, when it has reached its maximum collector current. when used as switch, the transistor is divided into cut off and saturation by the base current varied by the emitter –base voltage.

Transistor switching time: now let pay attention to the behavior of the transistor as a transistor from one state to the other. consider the transistor circuit shown in fig 5b.this wave form makes transistor between the voltage level V_2 and V_1 at V_2 the transistor is at cut off and at V_1 is applied between the base and the emitter through a resistor R_2 which may be included explicitly in the circuit or may represent the output impedance of the source furnishing the wave form.

In the fig the current does not immediately responds to the input signal. Instead there is a delay and the time escaped during this delay

$t_{off}=t_d+t_r$

When the input signal is at state t=T the current again falls to the responds. Immediately

$t_{off}=t_s+t_f$

The application of transistor as a switch:

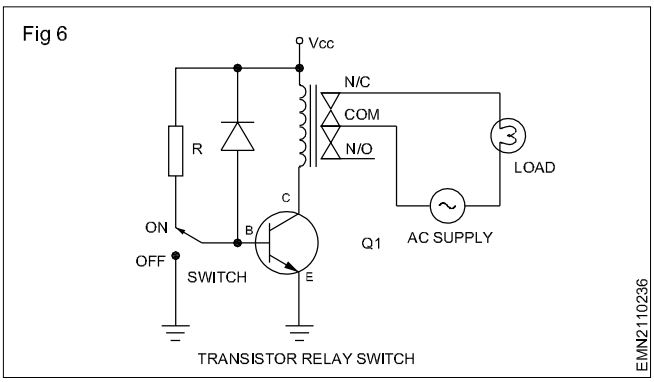
The transistor switch is used as

- as an electronic on off switch
- in the mono stable and bi-stable multi vibrators.
- In counter and pulse generator circuit
- in clipping and clamping circuit
- as a sweep starting switch in the cathode ray oscilloscopic equipments
- as a relay, but unlike the machanical relay the transistor has no moving mechanical parts.

Transistor relay switch: Transistor driven relay electronic switch circuit shown in Fig. 6. This type of circuits are mostly used in electronic circuits to drive high current and voltage circuits by using a small input voltage or current.

Circuit in Fig. 5 is same as transistor switch. In this relay will be the load for transistor. Transistor will ON-OFF relay by operating base current and relay will be operated high by current or voltage load.

When is connected to small current (in Fig6. switch connected to Vcc through current limitting resistor Rs.), transistor will go in saturation, so transistor will act as close switch so, current flows through relay. Due to current flowing in Relay. Relay will be magnetised and N/O contact will close. So, bulb load connected to the AC supply will ON.



When in put switch is OPEN, there is no current flowing to base of transistor. Transistor will goes in cut off, so transistor will act as OPEN switch *** current how through relay. Relay will not be energized and N/O contact remains open. So, bulb load is not getting current, it will not glow.

Biasing of Transistors

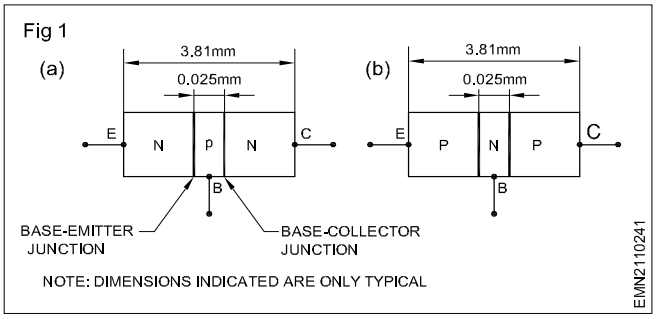
Objectives: At the end of this lesson you shall be able to

- **describe the operation of a NPN transistor & PNP transistor**
- **state the typical percent of base current and collector current in a properly biased transistor**
- **state the relationship between I_E, I_B and I_C**
- **state when a transistor is said to be properly biased**
- **state the meaning of leakage current I_{CO}.**

Biasing of transistors

Biasing a transistor means giving correct polarity and current level of voltages at the terminals of a transistor, such that, it functions as intended. (as an amplifier or as a solid state switch etc.)

Recall, transistors are three-layer semiconductor devices consisting of either a P-type layer sandwiched between two N-type layers as shown in Fig 1a or N-type layer between two P-type layers as shown in Fig 1b.



From Fig 1, the following points are important to note;

– The widths of the outer layers, i.e. emitter and collector layers are much greater than that of the base layer.

– The emitter layer is heavily doped compared to both the base and collector layers.

– The base layer is very thin, of the order of 1/10th the width of the outer layers, and is very lightly doped.

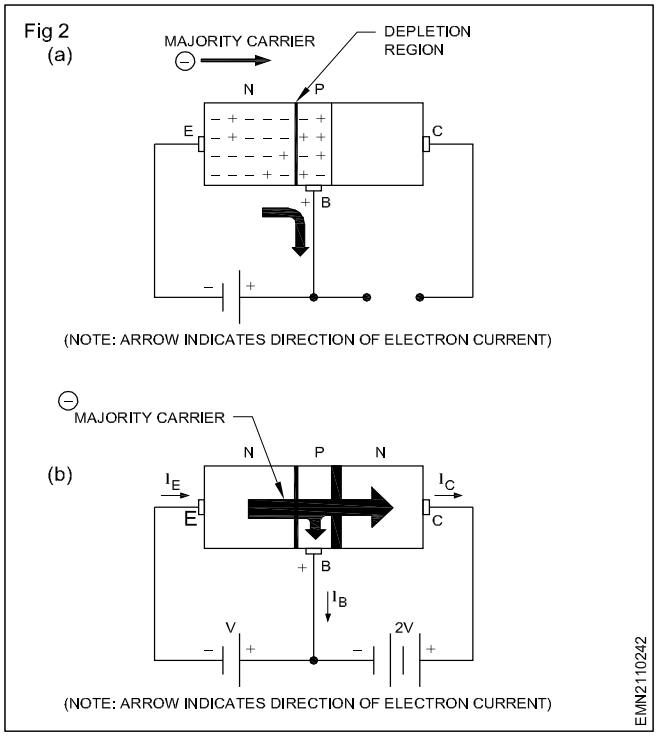
Transistor operation

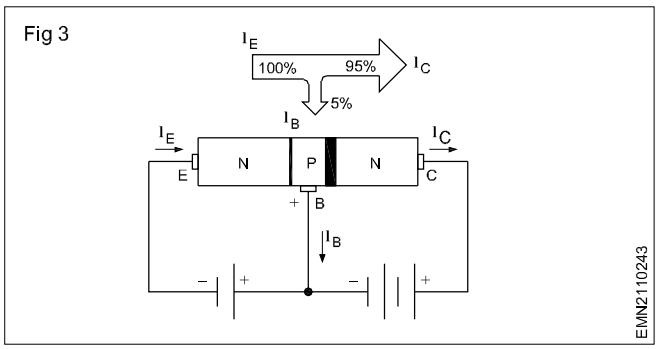
As transistors have three layers, there are two junctions as shown in Fig 1. The **base-emitter** junction behaves as one diode junction. The **base-collector** junction behaves as the other diode junction.

Recall that a diode junction conducts only when +ve supply is connected to the P material and -ve supply to the N material. Fig 2a shows a NPN transistor where the base-emitter junction is forward-biased. Hence, the diode conducts resulting in large flow of majority carriers(electrons) from N-type to P-type material.

Fig 2b shows the base-emitter junction forward biased and the base-collector junction is reverse-biased. Why is the base-collector reverse biased? what effect does this connection have on the transistor operation?

The answer is, in a NPN transistor, majority carriers are electrons, because, the emitter and collector are N-type materials. Free electrons are generated in the N-type emitter because of the forward-biased base-emitter





junction. If the collector voltage is not there , then all the generated electrons flow to the base as shown in Fig 2a.

When the base-collector is reverse-biased, then, a positive voltage appears at the collector. This positive voltage at the collector completely changes the path of the electron current flow. Because of the thin base and the low base-to-emitter voltage (0.7V for silicon), about 95 percent of the electrons pass through the thin base and are attracted to the more positive potential collector as shown in Fig 2b. Only a very small percentage of the electrons from the emitter combine with holes in the base.

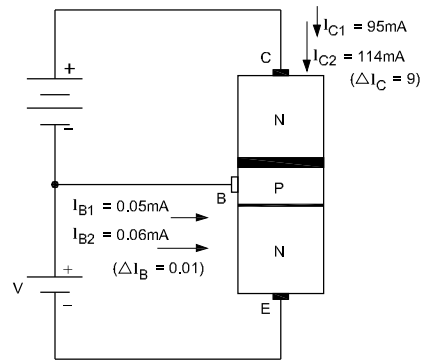
It can be seen from Fig 3, that the,

– current carriers come from the emitter

– base current is small(5% of emitter current)

– and, the collector current is high (95% of emitter current).

Fig 4



Under such conditions, it can be seen that, small changes in the emitter-base current will result in large change in the collector current. For example, an increase of say one electron in base current will result in an increase of 19 electrons in the collector current. This is because the collector current is 95% of the emitter current whereas the base current is only 5% of emitter current. This means that the value of the collector current can be easily controlled by changes in the bias on the emitter-base junction.

Summarizing, small changes in the base current results in large changes in the collector current as shown in Fig 4. This is nothing but amplification which is the intended function of a transistor. This behaviour of a transistor is known as Transistor action.

The ratio of the change in output current to the change in the input current is called the **amplification** or **gain**. In Fig.4, change in output current is ΔI_C due to the change in the input current ΔI_B. Therefore the current gain introduced by the transistor is,

Current gain

$$= \frac{\text{Output current change } \Delta\Delta_C}{\text{Input current change } \Delta\Delta_B} = \frac{9\text{mA}}{0.01\text{mA}} = 900$$

Gain is a dimension-less quantity

This condition as shown in Fig 4, in which the two junctions of the transistor are connected to such polarities of the voltage source, such that the transistor behaves as an amplifier, the transistor is then said to be properly biased or correctly biased.

Some books use the term Forward biased instead of the term properly biased.

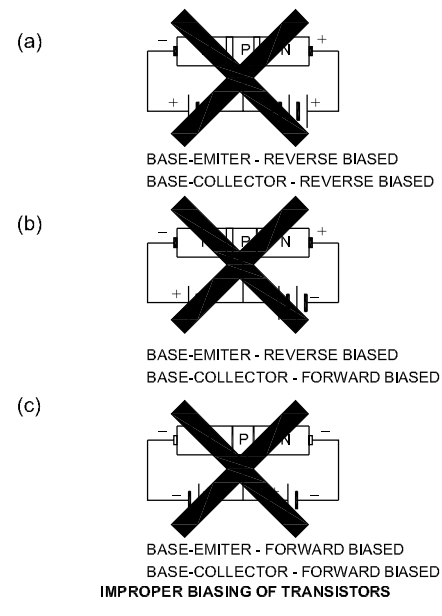
Summarising a transistor is said to be properly biased or correctly biased or forward biased if,

– its base-emitter junction is forward biased

– and, its base-collector junction is reverse biased.

On the other hand, if the polarities of voltages connected to transistor junctions is as shown in Fig 5a and 5b, because the base-emitter junction is reverse biased, no electrons are available for conduction, and, hence, the transistor action does not exist. If the base-emitter is forward biased but the base-collector is not reverse

Fig 5



biased as shown in Fig 5c, then, there is no amplification as both the junctions simply conduct as diodes.

In a properly biased transistor as shown in Fig 3 and Fig 4, the relationship between I_E, I_B and I_C is given by,

$$I_E = I_B + I_C \qquad \text{.....[1]}$$

or $I_C = I_E - I_B$

or $I_B = I_E - I_C$.

Minority current in transistors

In NPN transistor, as shown in Fig 6, if no voltage is applied across the base-emitter junction, but a reverse-bias is applied across the base-collector junction, the following things happen,

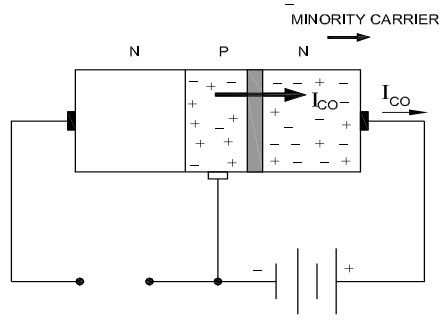
– There is no current in the base-emitter path as no bias voltage exists.

– The base-collector diode is reverse biased; hence, the forward current due to the majority current carriers(electrons) is zero.

– A small quantity current of the order of a few nanoamperes to microamperes flows in the base-collector. This small reverse current is due to minority current carriers, electrons in the **P-type** base material.

– The minority current increases if the voltage applied to the base-collector increases or the junction temperature increases. This is because current increases temperature

Fig 6

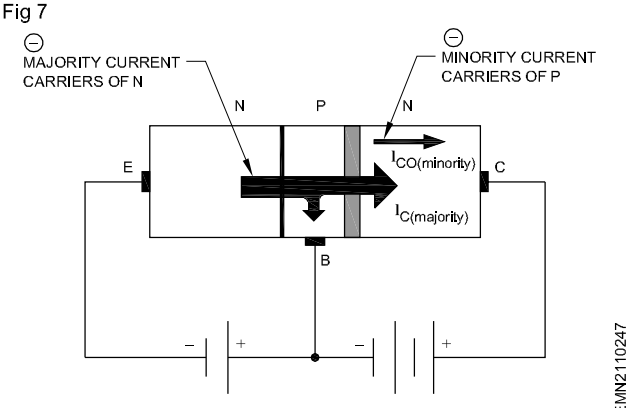


and temperature releases current carriers from the covalent bond structure.

This minority current is called the leakage current and is shown by the symbol I_{CO}. I_{CO} means, collector current I_C with emitter terminal open. The value of this leakage current I_{CO} will be given in the transistor data sheets for all transistors.

As shown in Fig 7, since the forward collector current I_C due to majority carriers and the leakage current I_{CO} due to minority current carriers flow in the same direction, they

Fig 7



are combined. Therefore, the total collector current will be equal to,

$$I_C = I_{C(majority)} + I_{CO(minority)} \quad .....[2]$$

Because of the minority current I_{CO}, the value of collector current I_C will be slightly more than that, given in the equation $I_C = I_E - I_B$. However, this slight increase in I_C value can be neglected because, the value of I_{CO} will be very very small compared to I_C (due to I_E) at normal working temperature.

In any typical general purpose transistor,

– value of I_C and I_E will be in milliamps

– value of I_{CO} will be in nanoamps to microamps

– value of I_B will be in microamps.

Operation of PNP transistors

Working of a PNP transistor is exactly the same as that of NPN transistors discussed earlier, if the role played by the electrons in NPN transistors is interchanged with holes as given below;

In a PNP transistor,

– The majority current carriers are holes instead of electrons

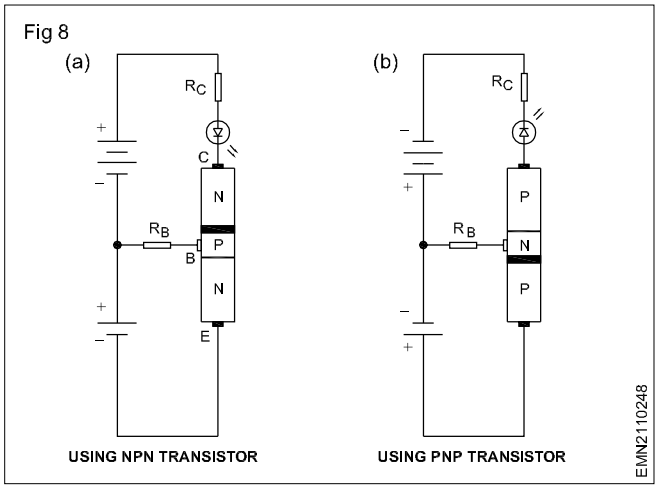
– The minority current I_{CO}, is due to electrons in the N-type base material instead of holes.

Test circuit for testing proper transistor biasing

If a transistor is properly biased (i.e. B-E junction forward biased and C-B junction reverse biased), then, there will be collector current I_C of the order of milliamps. To check this an LED is connected in the collector circuit of the transistors as shown in Figs 8a and 8b. The LED in the collector glows only when the transistor is properly biased otherwise the LED remains OFF.

Resistor R_B and R_C are introduced in the circuit to limit the base and collector currents such that the transistor does not get damaged due to excessive current.

Fig 8



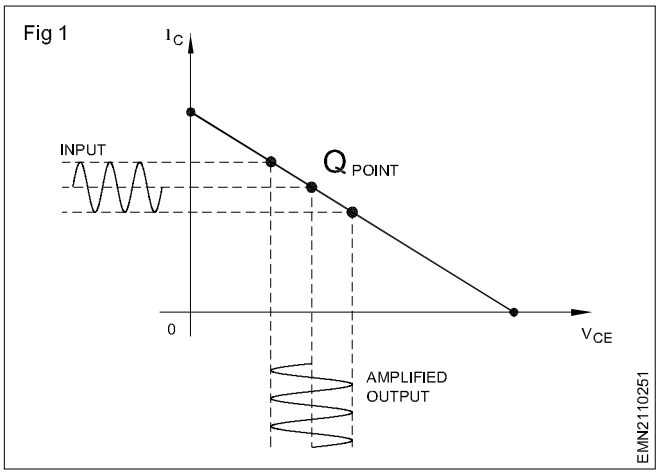
Types of Transistor Biasing

Objectives: At the end of this lesson you shall be able to

- **state the need for biasing of transistors**
- **state the reason for shifting of Q due to temperature and β_{dc} changes**
- **name the three main types of transistor biasing**
- **state the reason why base-bias is not preferred**
- **state the definition of amplifier**
- **list the classification of amplifier**
- **state the meaning of feedback**
- **state the reason why emitter-bias in also known as emitter feedback bias**
- **state why voltage divider bias is the most preferred type of biasing**
- **state the design guidelines for voltage divider type biasing.**

Before any one rides a motor cycle or drives a car, he has to start the engine and keep the engine running. In simple terms biasing transistors is similar to keeping the transistor started before making the real use of it. Once the transistor is started, like the engine of a car, it can be made to amplify, like covering the distance by riding the car.

Before an AC signal is fed to a transistor, it is necessary to set up an operating point or the quiescent(Q) point of operation. Generally this Q point is set at the middle of the DC load line. Once the Q point is set, then the incoming ac signals can produce fluctuations above and below this Q point as shown in Fig 1.



The need for biasing of a transistor can also be explained as follows;

For a transistor to remain operating in the linear region, the emitter diode must remain forward biased and the collector diode must remain reverse biased as long as the amplifier is amplifying. In other words, the amplitude variations in current and voltage of the input signal must not drive the transistor either into saturation or cut off.

Transistor stabilization with proper biasing a required quicent operating point of transistor amblefier in the active resion of transistor charatesties is oltained. It is neccessany that once oberatip boint in slected it should remain stable the maintenace of a boint stable is called stabilisation.

Stable Q point

A set Q point of a transistor amplifier may shift due to increased temperature and transistor b value changes. Therefore, the objective of good biasing is to limit this shifting of the Q point or to achieve a stable Q point.

Recall that, the Q point is nothing but a point in the output characteristic of the transistor. This point corresponds to a particular value of I_B, I_C and V_{CE}. Also recall that, the collector current I_C depends both on I_B and b of the transistor. If I_B changes, I_C changes, and hence, the Q point changes. If b changes, again I_C changes, and hence, the Q point gets shifted.

Shifting of Q due to temperature

Remember that a transistor is a temperature sensitive device. Any increase in the junction temperature results in leakage current. This increased leakage current in turn increases the temperature and the effect is cumulative. This chain reaction is called thermal run away. If this thermal run away is not stopped, it may result in the complete destruction of the transistor due to excessive heat. In transistors, due to this increased leakage current, the base current increases, and hence, the Q point gets shifted. This change in the set Q point affects the performance of the amplifier resulting in distortion.

Shifting of Q due to β_{dc} changes

Recall that two transistors of the same type number may have different values of b. This is due to the manufacturing process of transistors. Hence, when a transistor is replaced or changed, due to different b of the replaced transistor, the Q point again gets shifted.

Therefore, a stable biasing is one which does not shift the Q-point even if temperature varies and/or the b of the transistor changes.

Types of transistor biasing

There are several ways to bias a transistor for linear operation. This means, there are several ways of setting up a Q point near the middle of the dc load line. Important biasing arrangements used with transistors are explained below:

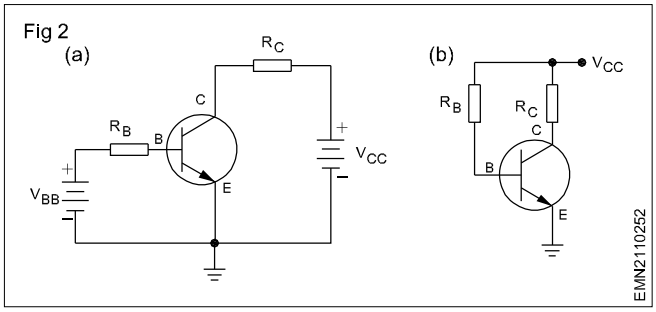


Fig.2 Shows one type of biasing of transistor known as base-bias. As shown in Fig 2b, usually, the collector voltage supply itself is used for the base voltage instead of a separate supply.

The value of the base resistor R_B is fixed such that it allows the necessary Q point base current I_B. The value of R_B ensures that the base-emitter diode is always forward biased by allowing 0.7V(for silicon) across V_{EB}.

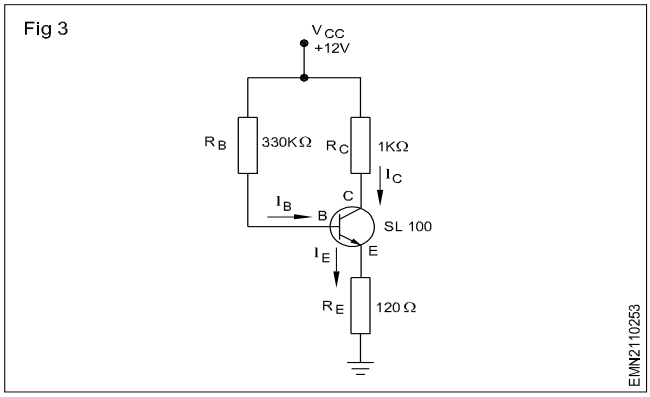
This type of biasing is the simplest of all. However, this is the worst possible way to bias a transistor because the DC Q point changes when,

– temperature increases and

– β of the transistor is changed.

Hence, in a base-biased transistor, it is impossible to set up a stable Q point. Therefore, base biasing of transistors is not generally done in linear amplifier circuits. However, base biasing is commonly used in digital circuits (discussed in further lessons) where transistors are used as a switch and not as a linear amplifier.

2 **EMITTER BIAS or emitter feedback bias**: Fig.3 shows a emitter-biased transistor. This type of biasing compensates for the variations in β_{dc} and keeps the Q point fairly stable.



In Fig 3, if β_{dc} increases, the collector current increases. This inturn increases the voltage at the emitter. This increased emitter voltage decreases the voltage across the base-emitter junction and therefore, the base current reduces. This reduced base current results in less collector current, which partially offsets the increase in I_c due to increased β_{dc}.

Emitter bias is also referred to as emitter feedback bias. This is because an output quantity, i.e., the collector current, produces a change in an input quantity i.e., the base current. The term feedback means a portion of the output is given back to the input. In emitter bias, the emitter resistor is the feedback element because it is common to both the output and input circuits.

In Fig 3, if we add the voltages around the collector loop, we get,

$$I_C R_C + V_{CE} + I_E R_E - V_{CC} = 0 \quad \text{.....\{1\}}$$

Since I_E approximately equals I_C, (asI_B is comparatively very small), equation..(1) can be arranged as,

$$I_C = \frac{V_{CC} - V_{CC}}{R_C + R_E} \text{.....\{2\}} \quad \text{.....\{2\}}$$

If we add voltages around the base loop, we get,

$$I_B R_B + V_{BE} + I_E R_E - V_{CC} = 0. \quad \text{.....\{3\}}$$

Since $I_E \approx I_C$ and $I_B = I_C/b_{dc}$, we can rewrite the equation as,

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B / \beta_{dc}} \text{.....(4)} \quad \text{.....\{4\}}$$

From equation ...(4), the presence of term b indicates that I_C is dependent on b. The intention of emitter-feedback bias to swamp out the effect b_{dc}. This is possible when R_E is made much larger than R_B/b_{dc}. However, in practical circuits R_E cannot be made very large because, large value of R_E takes the transistor out of the linear operating region. Due to this problem, the emitter-feedback bias is almost as sensitive to changes in b_{dc} as is the base-bias. Therefore, emitter-feedback bias is also not a preferred form of transistor bias and should be avoided.

In emitter-bias, the saturation current will be,

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(set)}}{R_E + R_C} \text{....[1]}$$

When the transistor is saturated, the value of V_{CE} will be between 0.2 to 0.3V. Hence can be neglected for all practical purposes.

In Fig 3, the saturation current is,

$$Ic(set) = \frac{12\ V}{1000\ \Omega + 120\ \Omega} = 10.71 mA.$$

Note: $V_{CE(sat)}$ of 0.2 volts is neglected.

When b_{dc} = 100, equation ...(4) gives,

$$I_C = \frac{12\ V - 0.7\ V}{120\ \Omega + 330\ K\Omega / 100} = 3.3\ mA.$$

When b_{dc} = 300, the same equation...(4) gives,

$$I_C = \frac{12\ V - 0.7\ V}{120\Omega + 330\ K\Omega / 300} = 9.262\ mA$$

Fig 4 summarizes the calculations by showing the DC load line and the two Q points. As can be seen, a 3:1 change in b_{dc} produces almost a 3:1 change in the collector current. This change is unacceptable as a stable-biased state.

TIP: For linear operation of the transistor, the base resistor R_B should be greater than bR_C. A base resistance of less than $b_{dc}R_C$ produces saturation in an emitter-feedback-biased circuit.

3 Voltage - Divider bias: Fig 5 shows a typical voltage-divider bias. This type of biasing is also called the universal bias because, this is the most widely used type of biasing in linear circuits.

This type of biasing is known as voltage divider bias because of the voltage divider formed by resistors R_1 and R_2. The voltage drop across R_2 should be such that it forward biases the emitter diode.

Fig 4

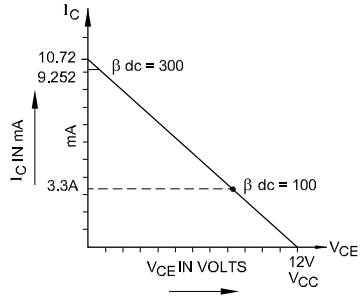
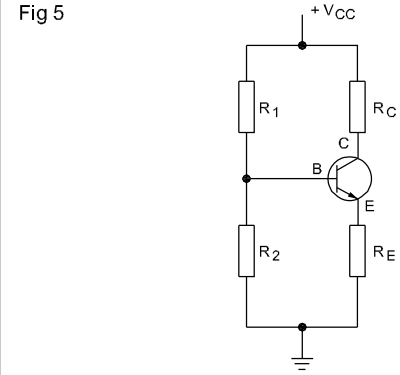


Fig 5



Emitter current in voltage divider bias

Assume that the base lead is open as shown in Fig 6b.

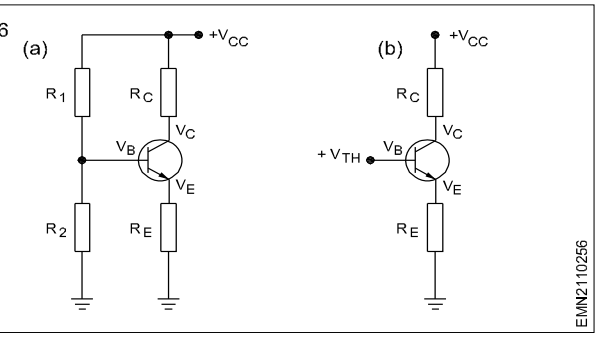
Looking back at the unloaded voltage divider,

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}.$$

V_{TH} is known as the Thevinin's voltage. Refer reference books for Thevinin's theorem.

Now assume that, the base lead is connected back to the voltage divider as in Fig 6a. Then, voltage V_{TH} drives the base of the transistor. In other words, the circuit simplifies to Fig 6a and the transistor acts like the controlled current source.

Fig 6



Because the emitter is boot-strapped to the base,

$$I_E = \frac{V_{TH} - V_{BE}}{R_E}.$$

The collector current I_C will be approximately equal to I_E.

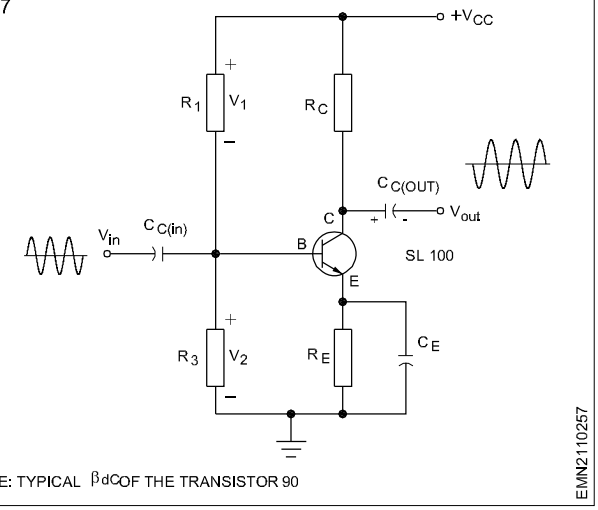
Notice that b_{dc} does not appear in the formula for emitter current. This means that the circuit is not dependent on variations in b_{dc}. This means that the divider-biased transistor has a stable Q point.

Because of the stable Q point, voltage-divider bias is the most preferred form of bias in linear transistor circuits. Hence, divider bias is used almost universally.

Simple voltage divider bias design guidelines

Fig 7 shows an amplifier using voltage-divider bias.

Fig 7



NOTE: TYPICAL β_{dc} OF THE TRANSISTOR 90

The capacitors C_C couple the ac signal into and out of the amplifier. The capacitor C_E is used to by-pass AC signals. A small AC input voltage drives the base, and an amplified AC output voltage appears at the collector.

In Fig 7, as far as the dc voltages and current is concerned, the capacitors appear like open circuits. Hence they can be neglected while designing the circuit for a stable Q point.

Design Step 1

Choose V_E equal to one-tenth of the chosen V_{CC}.

In Fig 7,

$V_E = 0.1V_{CC}$

$= 0.1 \times 12\ V = 1.2\ V.$

This design rule is suitable for most circuits, but remember that this is only a guideline. It is not necessary that everyone uses this rule. So, do not be surprised to find emitter voltages at values different from one-tenth of the supply voltage.

Design Step 2

Fix the required value of I_C almost equal to I_E. Ensure that the worst case chosen I_C is less than $I_{C(max)}$ of the transistor given in the data book.

For Fig 7, fix $I_E \approx I_C = 10$ mA.

$$\text{Therefore, } R_E = \frac{V_E}{I_E} = \frac{1.2\ V}{10mA} = 120\ \Omega$$

Design Step 3

To locate the Q point at approximately the middle of the DC load line, fix $V_{CE} = 0.5\ V_{CC}$.

Therefore, $V_{CE} = 0.5\ V_{CC} = 0.5 \times 12\ V = 6\ V$.

Hence, $V_{RC} = V_{CC} - V_{CE} - V_E = 12 - 6 - 1.2 = 4.8\ V$.

$$\text{Therefor, } R_E = \frac{V_{RC}}{I_C} = \frac{4.8V}{10mA}\ 480\ \Omega$$

Choose the nearest 470W as R_C.

TIP : With the above design rule, without calculation, you can simply choose the value of R_C as,

$R_C = 4 \times R_E = 4 \times 120 = 480W$ which is the same as calculated in step 3.

Design Step 4

To make a stiff voltage divider, apply the 10:1 rule,

i.e., $R_2 \leq 0.1\ \beta_{dc}\ R_E$.

NOTE: Take the typical value of $\boldsymbol{\beta}_{dc}$ from data book.

In Fig 7, with $\beta_{dc} = 90$

$R_2 \leq 0.1 \times 90 \times 120\ W = 1080\ W.$

Therefore, choose $R_2 = 1000\ W = 1\ KW$

Design Step 5

Find the voltage divider voltages V_1 & V_2.

$V_2 = V_{BE} + V_E$

In Fig 7, $V_2 = 0.7\ V + 1.2\ V = 1.9\ V$

Therefore, $V_1 = V_{CC} - V_2$.

In Fig 7, $V_1 = V_{CC} - V_2 = 12\ V - 1.9\ V = 10.1\ V.$

Calculate R_1 using the formula,

$$R_1 = \frac{V_1}{V_2}\ R_2.$$

In Fig 7,

$$R_1 = \frac{10.1V}{1.9V} 1000\Omega = 5.3K\Omega \approx 5.6K\Omega$$

This completes the design of the voltage-divider bias for

the transistor amplifier at Fig 7.

Fig 8a shows the transistor amplifier with the designed values of components.

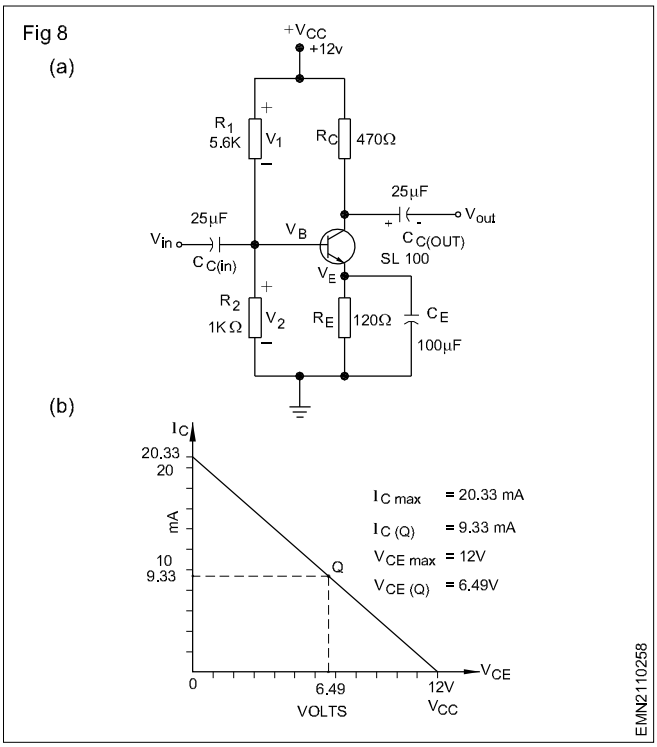
Fig 8b shows the DC load line and the Q point. As can be seen in Fig 8b, the Q point is near the middle of the dc load line. Hence, the designed circuit works in the linear portion of the transistor characteristic curve.

To cross check the above design we can calculate values of voltages and currents using the formulas given below;

$$V_B = \frac{R_2}{R_1 + R_2}.V_{CC}$$

Let us call the parallel combination of R_1 and R_2 as R_{BB}.

Fig 8



$$I_B = \frac{V_B - V_{BE}}{R_{BB} + (\beta + 1) R_E}$$ (See note given below)

$I_C = \beta I_B$

$V_{CE} = V_{CC} - I_C (R_C + R_E)$

NOTE: The formula given for I_B is,

$$I_B = \frac{V_B - V_{BE}}{R_{BB} + (\beta + 1)R_E}$$

This formula is arrived as given below;

$I_E = I_C + I_B$

$I_E = \beta I_B + I_B$

$I_E = (\beta+1) I_B$

In a divider bias, the effective resistance of $R_1 \parallel R_2$, denoted as R_{BB} is given by,

$$R_{BB} = \frac{R_1 . R_2}{R_1 + R_2}$$

The effective bias voltage is represented as VB is given by,

$$V_B = \frac{R_2}{R_1 + R_2}.V_{CC}$$

Writing the Kirchhoff's voltage equation for the base emitter loop at Fig 8,

$V_{CC} - I_B.R_{BB} - V_{BE} - I_E R_E = 0$ .....(1)

Note that R_{BB} is the effective resistance of parallel combination of R_1 and R_2.

Since $I_E = (\beta+1) I_B$

Rewriting equation...(1)

$V_{CC} - V_{BE} - I_B.R_{BB} - (\beta+1) I_B R_E = 0$

Solving the equation, we get, $I_B = \frac{V_{CC} - V_{BE}}{R_{BB} = (\beta + 1)R_E}$

Bias stabilsation transistor to be devolaped

Transistor bias stability: Through proper biasing,a desired quiescent operating point of the transistor amplifier in the active region (linear region) of the characteristics is obtained. It is desired that once selected the operating point should remain stable. The maintenance of operating point stable is called bias stabilisation.

Bias stabilization:

While designing the biasing circuit, care should be taken so that the operating point will not shift into an undesirable region (i.e, into cut - off or saturation region) Factors to be considered while designing the basing circuit:

Temperature dependent factors,

Transistor current gain the flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions.

Since the minority carriers are temperature dependent (gets doubled for energy 10C raise in temperature), they increase with the temperature.

2.5mv./c depends on since = increase in Increase This in turn changes the operation point.

STABLIZATION TECHNIQUE:

This refers to the use of resistive biasing circuits which allow to vary the bias so as to keep Relatively constant with variations.

COMPENSATION TECHIQUE:

This refers to the use of temperature sensitive devices as diodes, transistors, thermistors, etc, which provide compensating voltages adn current to maintain the operating point stable.

STABILITY FACTORS:

The stability factor is a meaure of stability provided by the biasing circuit.

Stability factor indicartes the degree of change in operating

point due to variation in temperature.

Since there are 3 temperature dependent variable, there are 3 stability factors.

Idealy, stability factor should be perfectly zero to keep the operating point stable.

Practically stability factor should have the value as minimum as possible.

The purpose of an amplifier: An amplifier is an electronics device which is used to amplify or increase the e level of week input signal into very high output signal. Transistors are used as amplifier in most of circuit. In addition resistor capacitor and biasing battery are required to form complete amplifier circuit.

Almost all the electronics system works with amplifier. we are able to hear the news or other program on radio. Simply because the amplifier amplifies the weak signal received by the antenna.

Classification of Amplifiers: Various of amplifiers description are based on the following factors.

1. Based on the transistor configuration
    a. Common emitter (CE) amplifier.
    b. Common collector (CC) amplifier
    c. Common base(CB) amplifier
2. Based on the output
    a. Voltage amplifier
    b. Current amplifier
    c. Power amplifier
3. Based on the input
    a. Small signal amplifier
    b. Large signal amplifier
4. Based on coupling
    a. RC coupled amplifier
    b. Transformer coupled amplifier
    c. Impedance coupled amplifier
    d. Direct coupled amplifier
5. Based on frequency response
    a. audio frequency (AF) amplifier
    b. intermediate frequency amplifier
    c. radio frequency (RF) amplifier
    d. VHF and UHF amplifier
6. Based on the feedback
    a. current series feedback amplifier
    b. Current parallel feedback amplifier
    c. Voltage series feedback amplifier
    d. Voltage parallel feedback amplifier
7. Based on biasing condition
    a. class A power amplifier
    b. class B power amplifier
    c. class AB power amplifier
    d. class C power amplifier

Of the above mentioned serial number one and two are explained at this state. Some of the amplifier deals in this book for detailed study can refer to any standard book for the remaining portions depending on their special interest.

Gain and Impedance of Common Emitter Amplifier

Objectives: At the end of this lesson you shall be able to
- **state the meaning and method of finding voltage gain**
- **state the meaning and method of finding input impedance**
- **state the meaning and method of finding output impedance**
- **state the meaning and method of finding power gain**
- **state the phase relationship between input and output in a CE amplifier.**

After a transistor is biased with the Q point near the middle of the DC load line, the transistor can be made to amplify AC and DC signals as shown in Fig 1a. When we use a transistor to amplify a small AC signal, the small AC signal to be amplified is coupled to the base of the transistor using a capacitor. A capacitor is used for AC coupling because as discussed in earlier lessons capacitors behave as short for AC signal and open for DC signal. The varying amplitude and frequency of the coupled AC signal produces greater value variations in the collector current of the same shape and frequency as shown in Fig 1b.

As shown in Fig 1a, if the input is a 1 kHz sine wave, the output will be an enlarged 1 kHz sine wave. The small sine wave given at the base of the transistor produces variations in the base current. Hence, the collector current is an amplified sine wave of the same frequency. The sinusoidal collector current flows through the collector resistor and produces an amplified sine wave output. Such amplifiers which retain the shape of the input signal at the output are called linear amplifiers.

Fig 1b, shows the DC load line, the Q point and AC input and output signals. This is generally referred to as the *AC* load line. As can be seen from Fig 1b, the AC input voltage produces variations in the base current. This results in sinusoidal variations about the Q point. Variations in Q

point are nothing but the variations in the collector current resulting amplified form of the input signal.

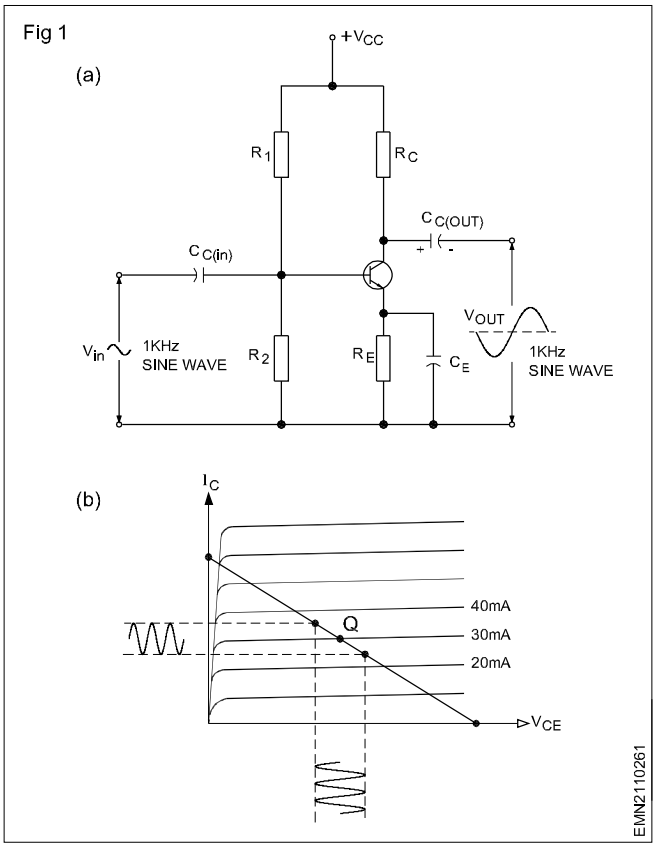
For small input signal levels, generally referred to as small signal operation, the peak to peak swing in the collector current should be less than the ±10% of the collector current at Q point to keep the distortion in the amplified output with in acceptable limits.

For large input signal levels, generally referred to as large-signal operation, the peak to peak swing in the collector current will be larger(more than 10%). If the swing is very large, the transistor may go into saturation and cut off. This swing into saturation and cut off will clip the positive and negative peaks of the output signal. This clipping is nothing but distortion, meaning, the output will not be an exact replicate of the input signal.

AC CURRENT GAIN A_i, of a CE amplifier

The AC current gain of a CE amplifier shown in Fig 1 is the ratio of the AC component of the collector current i_c, to the AC base current i_b.

Fig 1



$$A_i = \frac{i_c}{i_b}$$

Small letter i is used to represent AC current whose value keeps changing with time.

It is to be noted that in most linear CE amplifier circuits the current gain A_i is almost equal to b_{dc} of the transistor. Therefore the following approximation can be used for A_i.

$$A_i \approx \beta$$

In the amplifier at Fig 1, if b_{dc} of the transistor is 100, then the current gain A_i of the amplifier can be taken as 100.

Voltage gain, A or A_v of CE amplifier

The voltage gain of an amplifier is the ratio of AC output voltage to the AC input voltage. This is represented as,

$$\text{Voltage gain, } A_v = \frac{V_{out}}{V_{in}}$$

Small letter v is used for voltage because it is AC voltage whose amplitude keeps changing with time.

For example, in Fig 1, if the input voltage v_{in} is 80 m $V_{(p-p)}$ and the corresponding output voltage v_{out} is 7.2 $V_{(p-p)}$, then the voltage gain A_V is given by,

$$\text{Voltage gain, } A_v = \frac{7.2\ (p-p)}{80\text{m } V_{(p-p)}} = 90$$

A voltage gain of 90 means that, in this amplifier, a base voltage of 1 mV produces an output voltage of 9 mV.

The input and output voltage may be rms, peak, peak-to-peak, as long as the input and output are measured the same way consistently.

Input impedance, Z_{in} of CE amplifier

Recall that the maximum transfer of power takes place when the impedances of the supplying and receiving circuits are matched.

If impedances are to be matched for best circuit operation, both impedances must be known. If a single device such as a microphone, speaker, relay, etc. is to be used, its impedance will be given by the manufacturer. The amplifier to be designed for such a circuit must have an input or output impedance to match the input-output devices.

The AC source driving the amplifier has to supply AC current to the amplifier. The less the current the amplifier draws from the source, the better because the supplying source does not get loaded. The input impedance of the amplifier determines how much of current the amplifier takes from the ac source or the preceding stage of the amplifier.

In the normal frequency range of an amplifier, the coupling and by pass capacitors behave as a short for ac. The AC input impedance Z_{in} sometimes referred to as input resistance R_{in} is defined as the ratio of input signal voltage to input signal current.

$$Z_{in} = \frac{V_{in}}{i_{in}}$$

where, V_{in} and i_{in} are rms or peak or peak-to-peak values.

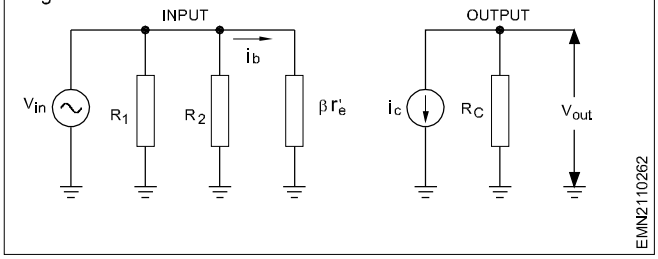
Fig 2 shows the AC equivalent circuit of the CE amplifier shown in Fig 1.

From the AC equivalent circuit the input impedance Z_{in} is given by,

$$Z_{in} \approx R_1 \parallel R_2 \parallel \beta r'_e \qquad \text{.....[1]}$$

where,

Fig 2



R_1 and R_2 are the voltage divider resistors,

b is the DC current gain and r'_e is the ac emitter resistance (V_{BE}/I_E). r'_e is approximately equal to 25W when the Q point is chosen at the mid of the load line.

In the CE amplifier at Fig 1, if R_1 = 18KW, R_2 = 8.2KW and the transistor b is 100, the input impedance Z_{in} will be,

$br'_e = 100(25\ W) = 2.5\ KW$

$Z_{in} = R_1 \parallel R_2 \parallel b\, r'_e$

$= 18\ KW \parallel 8.2\ KW \parallel 2.5\ KW$

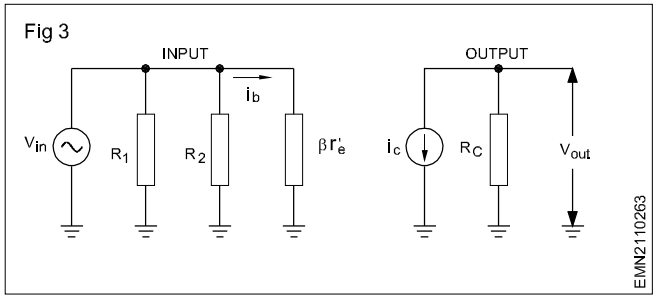
$= 1.73\ KW.$

Practical way of finding Z_{in}

To find Z_{in} of a given CE amplifier circuit, it is merely necessary to measure the AC signal input voltage and current. Then, use these values in the formula, and calculate Z_{in}.

A simpler method to measure i_{in} is to connect a series input resistance of known value in series with the input signal, as in Fig 3.

Fig 3



The voltage drop across the resistor R_s is measured, and Ohm's law is used to determine i_{in}.

$$I_{in} = \frac{V_X - V_Y}{R_S}$$

The value of V_{in} can be measured directly, as shown in Fig.3.

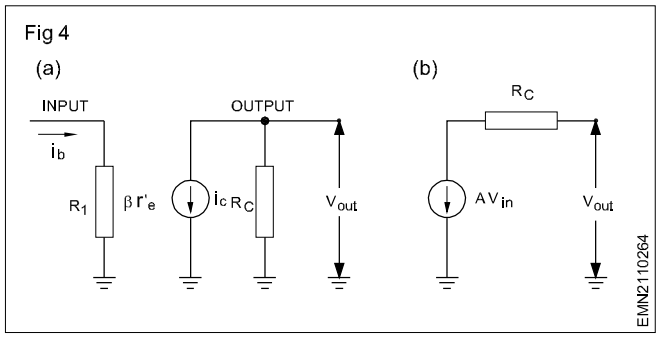
Output impedance, Z_{out}

The output impedance of a CE amplifier is naturally the impedance at the output terminals.

To find the Z_{out} of the CE amplifier shown in Fig 4, consider the AC equivalent of the output as shown in Fig 4a.

Recall that a transistor operating in the linear portion of its characteristics curve is like a current source. Therefore, we can represent it as a current source i_C.

Fig 4



As can be seen from Fig 4a, this collector current source is in parallel with the collector resistor R_C. Assuming that the collector current source is ideal, it has infinite internal impedance. Then, the only impedance in the output is the collector resistor R_C.

The Thevinin's voltage appearing at the output is the voltage gain(A) times the input v_{in}.

Therefore, $V_{out} = A.v_{in}$

Hence, the output AC equivalent circuit of the amplifier can be simplified as shown in Fig 4b. In Fig 4b, an ideal output voltage source AV_{in} with zero internal impedance is in series with the collector resistor R_C. Therefore, the output impedance of the CE amplifier is approximately equal to the collector resistor R_C,

$Z_{out} \approx R_c$

In the CE amplifier circuit at Fig 1, if R_c = 1000W, the output impedance of the amplifier is equal to the value of R_C , that is 1000 W.

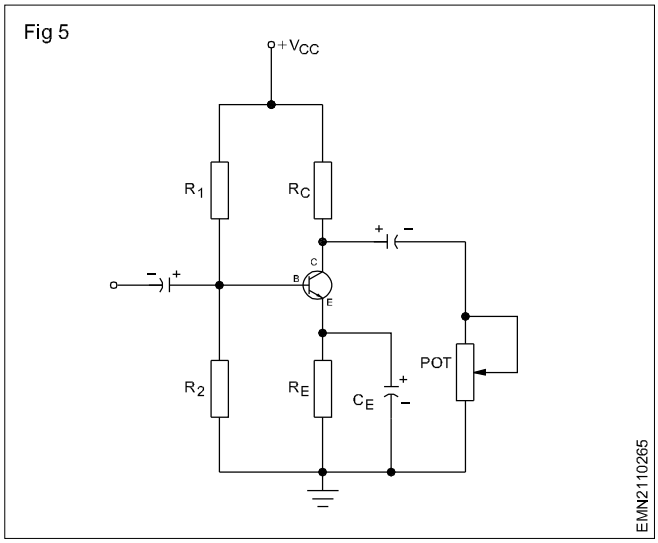
Practical way of finding Z_{out}

The easiest way of measuring the output impedance of a CE amplifier circuit is given below;

(1) Measure the unloaded output voltage V_{out} of the CE amplifier.

(2) Place a variable resistor across the load terminals, as shown in Fig 5.

Fig 5



(3) Adjust the variable resistor until the voltage drop across it is one-half of the unloaded output voltage V_{out}.

(4) Remove the variable resistor and measure its value. This value is equal to Z_{out}.

Z_{out} is not a fixed value; it varies with transistor voltages and the load resistance. Care must always be taken to maintain an undistorted signal when input or output impedances are measured.

Power gain, A_p of a CE amplifier

In the CE amplifier shown in Fig 1, the input power is given by,

$$P_{in} = v_{in}.i_b$$

and the output power is given by,

$$P_{out} = - v_{in}.i_b$$

The negative sign associated with output power. This is because, in a CE amplifier, the output is 180° out of phase with the input signal. Details are discussed in the forthcoming paragraphs.

In the CE amplifier at Fig 1, power gain A_p is the ratio of output signal power to input signal power. The formula is,

$$\text{Power gain} = \frac{P_{out}}{P_{in}}$$

=

Power gain is also given by,

$$A_p = - A_v \, . \, A_i$$

where,

A_v is the voltage gain (v_{out}/v_{in})

A_i is the current gain (i_c/i_b)

For the amplifier at Fig 1, if A_v = 90 and the b of the transistor is 100, then the power gain A_p of the amplifier is given by,

$$A_p = - A_v.A_i = 90 \times 100 = 9000.$$

This means that if an AC input power of 1 µW is given to the amplifier, the output power will be 9mwatts.

Practical way of finding A_p

Since the formula for power is, $P = I^2 \times R = I \times I \times R$

Since,

$$I = \frac{V}{R} \text{ (substituting this in above equation, we get)}$$

$$P = \frac{V^2}{R}$$

Therefore, by Ohm's law, power gain is easy to calculate when signal voltages and impedances are known as given below;

$$P_{out} = \frac{V_{out}^2}{Z_{out}} \quad \text{and} \quad Pin = \frac{V_{in}^2}{Z_{in}}$$

Knowing the values of P_{out} and P_{in} power gain of the circuit can be calculated.

Power gain, A_p in decibels, dB

The power gain of amplifiers is often expressed in decibels (dB). To calculate the power gain of an amplifier in decibels, use the following formula.

$$\text{Power gain dB} = 10 \log \frac{P_{out}}{P_{in}}$$

Input - Output phase relationship

Recall, that while calculating the power gain it was mentioned that the output signal of a CE amplifier is 180° out of phase with its input signal. To find out why this happens in a CE amplifier, assume that the DC base bias current I_B at the set Q point is 30 µA. The corresponding collector current is 1 mA. When the AC signal is applied to the input, the base bias varies from 20 to 40 µA, as shown in Fig 1b. Since the type of transistor used is NPN, as base bias is increased to 40 µA, collector current i_c increases. The resultant effects are,

– the increased transistor conduction causes less voltage drop across the transistor(V_{CE})

– increased i_C causes a larger voltage drop across R_C. Hence, the voltage across the collector to ground gets reduced.

In Fig 1a, as the output signal is taken across the transistor collector and ground, an increasing signal voltage causes a decreasing output signal.

As the input signal level decreases, say to 20 µA, the forward bias is less and transistor conduction decreases . When transistor conduction decreases, its resistance is higher and so the voltage drop across it increases. With increased voltage drop across the transistor, the output voltage V_{out} increases. This increase in V_{out} reduces the voltage drop across the collector load resistance R_C.

From this, it can be concluded that in a CE amplifier, a negative-going input signal causes a higher, or, more positive-going output signal. Therefore, in a CE amplifier the output is 180° out of phase with the input.

Practical way of finding input-output phase relationships

The phase relationship between input-output can be found in two ways as given below.

Method 1: Using a dual trace CRO, connect one of the CRO inputs to the input of the amplifier and the other CRO input to the output of the amplifier. Make the oscilloscope to trigger on the input signal. The waveforms shown on the CRO show the phase relationship between input and output as shown in Fig 6a.

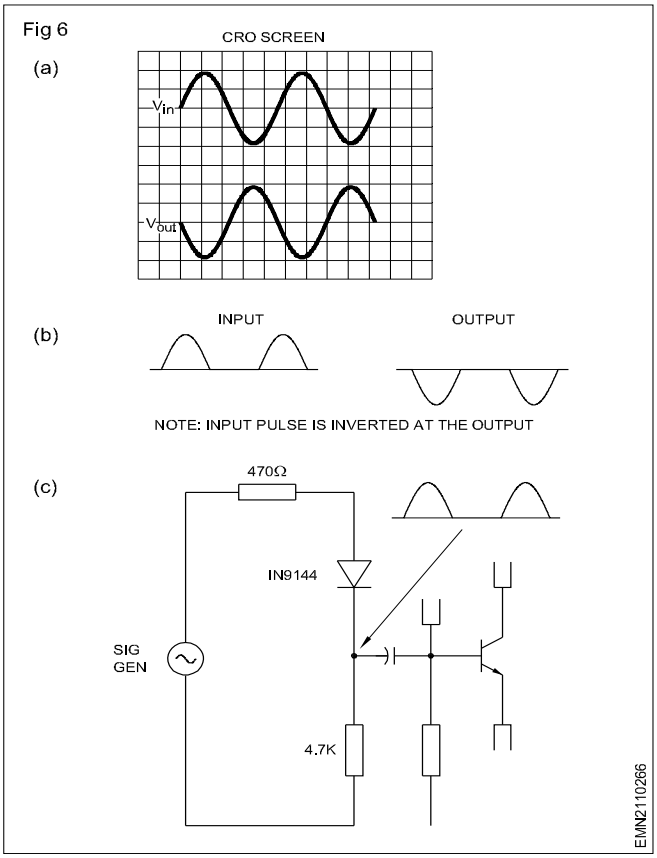
Method 2: If a single trace CRO is used, then instead of feeding complete sinewave to the input, feed only the positive signal pulses as shown in Fig 6b. These positive pulses can be generated using a simple half-wave rectifier

as shown in Fig 6c.

With the positive pulse fed at the input, the output of the CE amplifier will be negative pulse as shown in Fig 6b. Use the signal as an external trigger source for the CRO to view the waveform.

dB vs dBm

When a physical quantity, such as power or intensity, is measured relative to a reference level it is expressed in decibels (dB), which is a logarithmic unit. Decibel is considered as a dimensionless unit because it is a ratio of two quantities with the same unit thus cancellation takes place. It is used for quntifying the ratio between two values. The best example of this is the signal - to -noise ratio.



Sound pressure level is typically measured in dB but the unit is not limited to that quantity alone. There are a lot of uses of this measuring unit particularly in engineering. Since it is applicable in measuring signals, anything that can be expressed in waves may also be measured with dB. In the disciplines of acoustics electronics,dB is liberally utilized.

To be exact, decibel dB is expressed in this term: dB 10log (P1/P2). Where P1 and P2 are two different values of power.

It is primarily used because it can represent an extremely huge number into a convenient scale. Inradio link designs, values often differ enormously and to contrast these values decibel is used. Its logarithmic properties make calculation easier. With the implementation of dB, engineers and physicist are now able to calculate values with simple few numbers as an aiternative of arduous 9 to 10-digit ones.

dBm is different but definitely related to dB. dBm stands foran absolute power level. It is in reference to another unit of power the milliwatt.

Mathematically, dBm = 10* log (P/1mW)

The value of “P” is power in watts. Then, with further calculation, you can convert the absolute power unit “P” into dBm. The value of power level “P” is now referenced to 1 mW. The unit dBm is devised because in practice, 1 mW is a convenient reference point from which to measure power. dBm is considered as an absolute unit “a unit to measure power.

Additionally, based on what value the power is referred to, a particular absolute value of power can be in any kind. If dBm “which can be written in dBmW by the way - is acquired because of 1mW reference, a value can be in a form of dBW if it is referred to 1 watt.

Effect of bypass Capacitor in CE Amplifiers

Objectives: At the end of this lesson you shall be able to

- **state the effect of emitter resistor bypass capacitor on,**
  - **the gain of the amplifier**
  - **input impedance of the amplifier**
  - **quality of the amplified output.**

Figs 1a and 1b show common-emitter amplifiers. The difference between the two circuits is that in Fig 1a, there is a capacitor C_E connected across the emitter resistor R_E. This capacitor is known as a bypass capacitor.

The function of the bypass capacitor are;

– to provide a low resistance path for the AC signals

– to behave as open circuit for DC signals.

The effect of the bypass capacitor are;

– increased gain of the amplifier

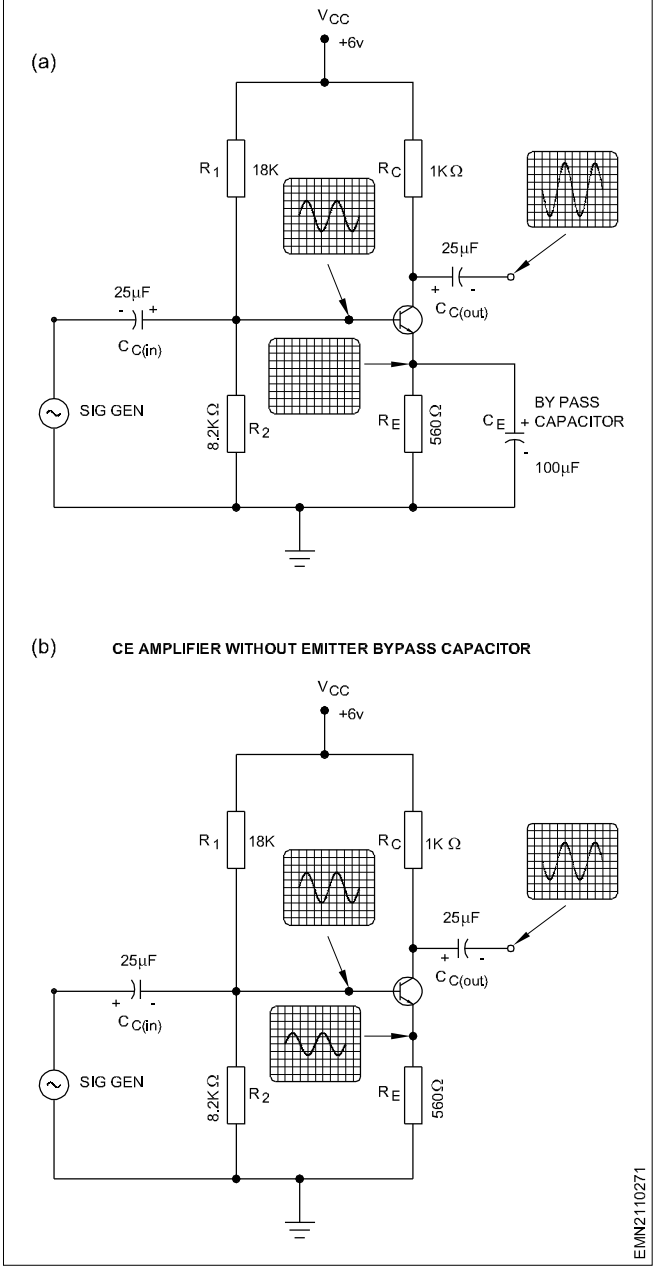
– decreased input impedance of the amplifier.

Effect of C_E on amplifier gain

To understand the effect of the bypass capacitor on the gain of the amplifier, observe the phase relationship of the waveforms at base,emitter and collector shown in Figs 1a and 1b.

As can be seen in Fig 1b, the AC signal at the emitter is

Fig 1 CE AMPLIFIER WITH EMITTER BYPASS CAPACITOR



in phase with the input signal. Recall that both input and output currents flow through the emitter resistor R_E.

If R_E is not bypassed as in Fig 1b, then,

– as the input signal increases, the collector current increases, and hence, the voltage drop across R_E increases. This result in increased voltage at the emitter terminal.

– the increased voltage at the emitter results in a reduced base-emitter voltage

– this reduced V_{BE} results in less forward bias of the transistor, and hence, the collector current decreases.

Therefore, the overall effect of an un-bypassed emitter resistor is that, the collector current is not allowed to freely increase for increase in the base current. Hence, the gain of the amplifier is held at almost a constant value.

If R_E is bypassed as in Fig 1a, then,

– as the input signal increases, the collector current increases. Since the emitter resistor is bypassed, the bypass capacitor provides a very low resistance path for the AC current, and hence, voltage at the emitter does not increase

– since the emitter voltage does not increase, the emitter-base junction remains at increased forward bias and the increased collector current continues to flow

Therefore, the overall effect of a bypassed emitter resistor is that the collector current is allowed to freely increase for increase in the base current. Hence, the gain of the amplifier increases.

Summarizing the above effect, in a CE amplifier with the emitter resistor bypassed, the gain of the amplifier is higher when compared to that of an un-bypassed emitter amplifier.

The input impedance of a emitter resistor bypassed CE amplifier is given by,

$$Z_{in} = R_1 \parallel R_2 \parallel \beta r'_e.$$

For the emitter bypassed amplifier shown in Fig 1a, the input impedance will be,

$$Z_{in} = 18\ K \parallel 8.2\ K \parallel 100(25).$$

$$= 1.73\ KW$$

Now if the emitter resistor is not bypassed by a capacitor as shown in Fig 1b, then, the input impedance is given by,

$$Z_{in} = R_1 \parallel R_2 \parallel \beta (r'_e + R_E).$$

The resistor R_E is now in series with r'_e.

For the un-bypassed amplifier shown in Fig 1b, the input impedance will be,

$$Z_{in} = 18\ K \parallel 8.2\ K \parallel 100(25 + 560)$$

$$= 5.14\ K\Omega.$$

The above comparison of Z_{in} for bypassed and un-bypassed emitter CE amplifier indicates that the input impedance of the amplifier decreases drastically when the emitter resistor of the CE amplifier is bypassed with a capacitor.

Summarizing, in a CE amplifier if the emitter resistor by passed the input-impedance of the amplifier reduces drastically when compared to the input-impedance of a CE amplifier with un-bypassed emitter resistor.

Disadvantage of bypassing emitter resistor

Although bypassing the emitter capacitor increases the gain of the amplifier, it has the following disadvantages which are very important to be considered;

– The reduced input impedance due to bypassed R_E has the loading effect on the source of the AC signal feeding

the amplifier. This is very important especially when the source feeding the input is a weak signal such as the output of a R/P head of a tape recorder, crystal pick-up of a gramophone etc.,

– In a bypassed R_E amplifier, the voltage gain changes throughout the input cycle. This changing voltage gain may results in a distorted output signal.

As a compromise between an unbypassed emitter resistor and a bypassed emitter resistor, some amplifier circuits use partially bypassed emitter resistor as shown in Fig 2.

The effect of partially bypassed emitter resistor on the gain and input impedance is given below;

$$V_{out} = i_C R_C$$

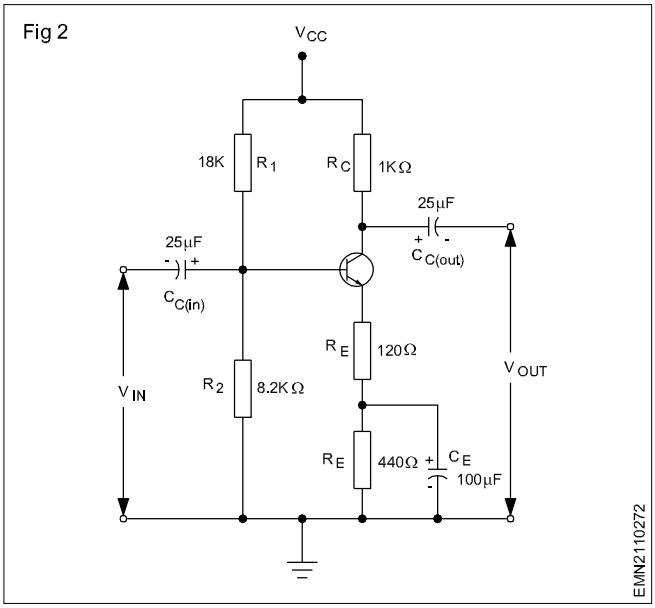
(The -ve sign indicates that output is 180 out of phase with the input)

The AC voltage across $r_E + r'_e$ is,

$$V_{in} = i_e (r_E + r'_e)$$

Therefore, voltage gain A_v is,

Fig 2



$$A_v = \frac{V_{out}}{V_{in}} = \frac{-i_c R_c}{i_e (r_E + r'_e)}$$

Since, $I_e \approx I_c$, $A_v = \frac{-Rc}{r_E + r'_e}$

In a fully bypassed emitter resistor, the value of Av was given by

$$A_v = \frac{-R_c}{r'_e}$$

The input impedance Z_{in} of the partially by passed emitter resistor is given by,

$$Z_{in} = R_1 \parallel R_2 \parallel \beta(r_E + r'_e)$$

For the values of R_E and r_E shown in Fig 2, the input impedance Z_{in} is,

$$Z_{in} = 18K \parallel 8.2K \parallel 100(120+25)$$

$$\approx 4.06\ K\Omega$$

Note that this value of Z_{in} is in between those of fully bypassed and unbypassed emitter resistor.

Frequency Response of Common Emitter Amplifier

Objectives: At the end of this lesson you shall be able to

- **state the meaning of frequency response of an amplifier**
- **state the effect of capacitors on the frequency response of a CE amplifier**
- **find the theoretical lower cut off frequencies of an amplifier, given the values of coupling and bypass capacitors.**

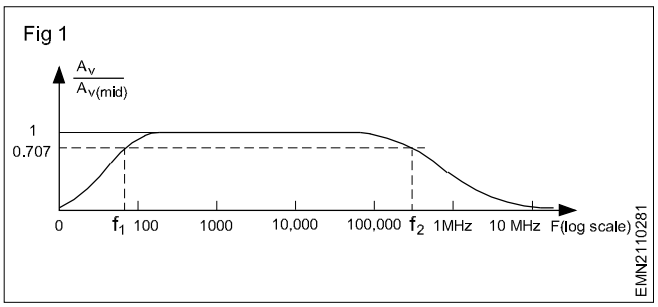
Recall, when a 1kHz sine wave is fed at the input of an amplifier, the output will be an enlarged 1 kHz sine wave. The amount, by which the output voltage is enlarged, depends on the voltage gain of the amplifier.

In the same amplifier, instead of a constant frequency 1kHz signal, if the frequency of the input signal is varied, from say 0 Hz (DC) to several tens of kilo Hertz, then the extent to which the input level is enlarged at the output will be different at different frequencies. In other words, the gain of the amplifier will not be the same for all frequencies.

The reason for the gain to be different at different frequencies is mainly due to the capacitors used in the amplifier circuit. In addition to these capacitors, the transistor itself is a reason for the gains to be different at different frequencies. But the effect of the transistor is negligible at low and medium frequencies.

Fig 1 shows a typical plot of gain of an amplifier at different frequencies. Note that in Fig 1, the Y axis represents the gain of the amplifier at different frequencies as a measure of the gain at mid frequency $A_{v(mid)}$.

From Fig 1, it is clear that in a capacitor coupled amplifier as in Fig 2a, the gain falls sharply towards *0* frequency



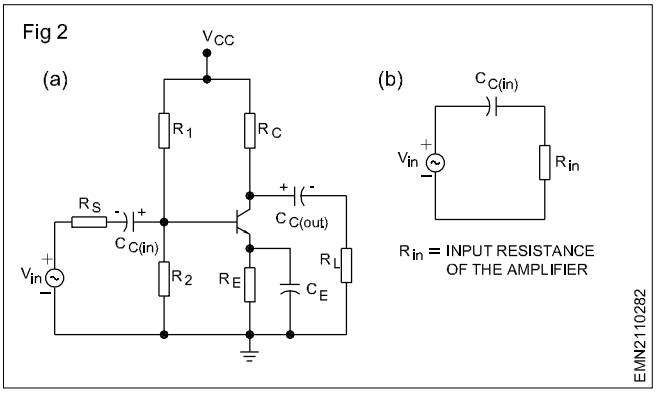
and also at high frequencies. The fall in gain in the lower frequency range is mainly due to the effect of coupling capacitor C_C and bypass capacitor C_E of the amplifier.

Effect of input coupling capacitor $C_{C(in)}$ on frequency response of CE amplifiers

Fig 2a shows the typical common emitter amplifier using coupling and bypassing capacitor. To understand the effect of $C_{C(in)}$, assume that the values of C_E and $C_{C(out)}$ are very large and have no effect on the frequency response of the amplifier.

The input section of the amplifier in Fig 2a can be simplified as shown in Fig 2b. In Fig 2b, R_{in} represents the input Resistance/Impedance of the amplifier.

Considering the effect of the coupling capacitor C_{Cin} for AC signals, the coupling capacitor has,



– very high resistance(impedance) X_C at very low frequencies and is almost infinity or open at zero frequency (DC).

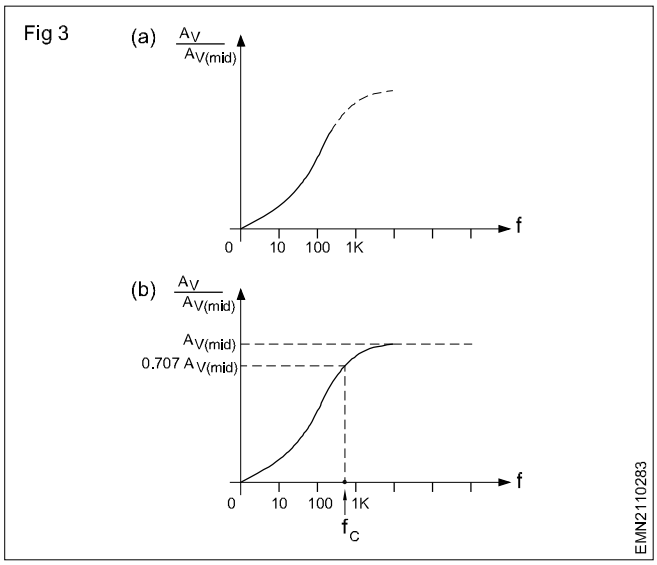
$$\left(\text{Recall } X_C = \frac{1}{2\pi fC}\right)$$

– no effect, or it behaves as a short at the mid-band frequencies, say greater than 1 kHZ and less than few hundred kHZ.

The above listed effects of the coupling capacitor $C_{C(in)}$ is because, the capacitive reactance X_C is inversely proportional to frequency f as given below;

$$X_c = \frac{1}{2\pi fc}$$

When f= 0 Hz, X_C = Infinity. Hence, the voltage across R_{in} will be zero. Therefore, at zero input frequency the output of the amplifier is 0. But as the frequency increases the voltage across R_{in} increases (as X_C decreases) and



hence, the output increases. This is shown in Fig 3a.

As the input frequency is further increased, X_C decreases and approaches zero. Therefore, all the applied input voltage V_{in} appears across the input of the transistor. Hence, the gain of the amplifier will be high as shown in Fig 3b.

Referring to the amplifier response at low frequencies shown in Fig 3b, at a particular frequency known as the cut-off frequency $f_{C(in)}$, the reactance X_C will become equal to R_{in}. At this frequency $f_{C(in)}$, the input section of the amplifier behaves as a AC voltage divider. Hence the output voltage of the input RC network shown in Fig 2a (also known as lag network) is given by,

$$V_{out} = \frac{R_{in}}{\sqrt{R_{in}^2 + X_c^2}} V_{in} \quad \ldots\ldots [1]$$

$$\frac{V_{out}}{V_{in}} = \frac{R_{in}}{\sqrt{R_{in}^2 + X_c^2}}$$

At cut-off frequency $f_{C(in)}$,

since, $X_C = R_{in}$,

$$R_{in} = \frac{1}{2\pi f_{c(in)} C_{c(in)}}$$

Therefore the critical frequency $f_{C(in)}$ is given by,

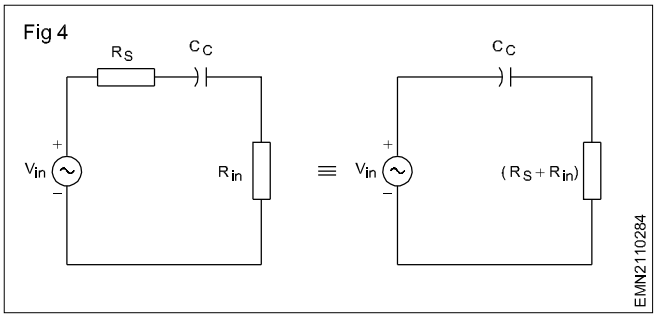
$$f_{c(in)} = \frac{1}{2\pi R_{in} C_{c(in)}} \ldots\ldots [2]$$

The source feeding the amplifier will have some amount of resistance coming in series as shown in Fig 4.

If this series resistance or the source resistance R_S is also considered in the input section of the amplifier, then the lower cut off frequency f_C is given by,

$$f_{c(in)} = \frac{1}{2\pi (R_s + R_{in}) C_{c(in)}} \ldots\ldots [3]$$

Example : In the CE amplifier shown in Fig 2a, R_{in} is



1.73KΩ and source resistance R_S is 1 KΩ. If the value of input coupling capacitor $C_{C(in)}$ is increased from 0.047μF to 10μF, the lower cut off frequency $f_{C(in)}$ for different values of $C_{C(in)}$ will be,

using the formula at equation ...{2},

for

$C_{C(in)}$ = 0.047μF = $f_{C(in)}$ = 1240 Hz

$C_{C(in)}$ = 0.47μF = $f_{C(in)}$ = 124 Hz

$C_{C(in)}$ = 4.7μF = $f_{C(in)}$ = 12.4 Hz

$C_{C(in)}$ = 10μF = $f_{C(in)}$ = 5.83 Hz.

From the above calculated values, it is clear that for the amplifier to work as an audio-amplifier(20Hz to 20 KHz), the value of the input coupling capacitor to be chosen should be 4.7μF or more.

Half-power point

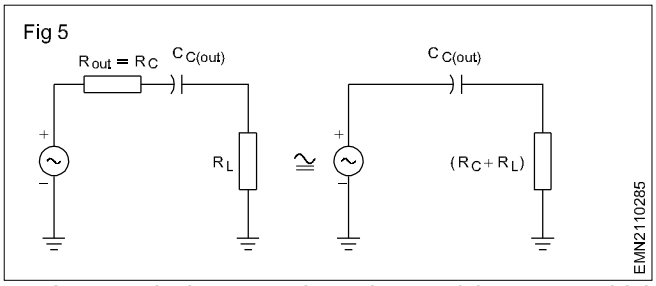
At the lower cut-off frequency $f_{C(in)}$, the reactance of the input coupling capacitor $X_C = R_{in}$. If we substitute this into equation ..(1), we get

$$\frac{V_{out}}{V_{in}} = 0.707$$

This means, the voltage gain at the cut-off frequency will be 0.707 times the gain at mid frequency $A_{v(min)}$. Hence, the cutoff point $f_{C(in)}$ is sometimes called the *half-power point* because at this point, the available output power is half of its maximum value.

Effect of output coupling capacitor $C_{C(out)}$ on frequency response of CE amplifiers

Fig 5 shows the equivalent circuit of the output section of a typical CE amplifier shown in Fig 2a. To understand the effect of $C_{C(out)}$, assume that the values of C_E and $C_{C(in)}$ are very large and have no effect on the frequency response of the amplifier.



In Fig 5, R_{out} is the output impedance of the stage, which is approximately equal to R_C. Making similar analysis as in the case of calculating the $f_{C(in)}$ due to $C_{C(in)}$, the cut off frequency $f_{C(out)}$ of the amplifier due to output coupling capacitor C_C is given by,

$$f_{c(out)} = \frac{1}{2\pi\,(Rc_c + R_L)\,C_{c(out)}} \quad .....[4]$$

Example : In the CE amplifier shown in Fig 2a, R_{out} is 1KW and R_L is 1.8KΩ. If the value of output coupling capacitor $C_{C(out)}$ is increased from 0.047μF to 10μF, the cut off frequency $f_{C(out)}$ for different values of $C_{C(out)}$ will be,

using the formula at equation ...{4}, for,

$C_{C(out)}$ = 0.047μF = $f_{C(out)}$ = 1210 Hz

$C_{C(out)}$ = 0.47μF = $f_{C(out)}$ = 121 Hz

$C_{C(out)}$ = 4.7μF = $f_{C(out)}$ = 12.1 Hz

$C_{C(out)}$ = 10μF = $f_{C(out)}$ = 5.7 Hz.

From the above values it is clear that for the amplifier to work as an audio-amplifier(20Hz to 20 KHz), the minimum value of the output coupling capacitor to be chosen should be 4.7μF.

Effect of emitter bypass capacitor on low frequency response

To understand the effect of the bypass capacitor C_E, assume that the values of $C_{C(in)}$ and $C_{C(out)}$ are very large and have no effect on the frequency response of the amplifier.

For the amplifier shown in Fig 2a, if the effect of the emitter bypass capacitor is considered,

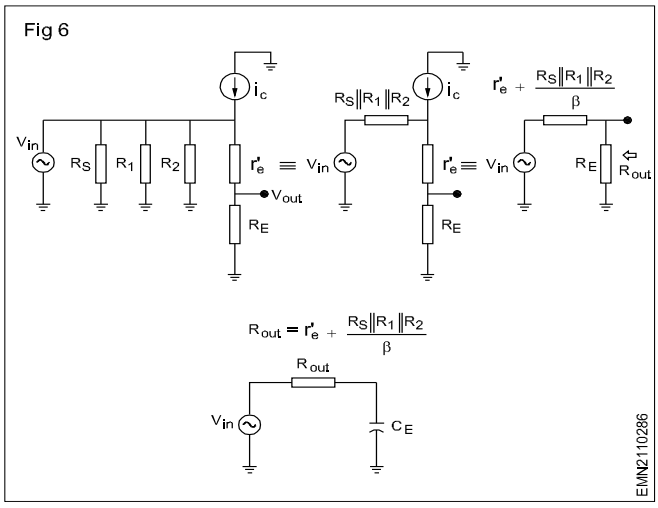
– In the mid-band C_E appears like a ac short, making R_{out} approximately equal to R_C

– below the mid-band the R_E no longer appears like a perfect ac short. Therefore the voltage gain decreases. (Recall effect of R_E bypass capacitor on amplifier gain.)

Fig 6 shows the resistance seen by the by-pass capacitor C_E under such a condition.

Then R_{out} becomes,

$$R_{out} \approx r_e' + \frac{R_S \| R_1 \| R_2}{\beta} \quad .....[5]$$



Analyzing Fig 6, in a similar way as done for coupling capacitors, the cut off frequency f_E due to the bypass capacitor C_E is given by,

$$f_E = \frac{1}{2\pi R_{out} C_E} \quad \ldots\ldots[6]$$

where

f_E = cut off frequency of emitter network

R_{out} = output resistance as seen by the bypass capacitor

C_E = emitter bypass capacitor.

Example : For the CE amplifier shown in Fig 4, if the b of the transistor is 100 and if the value of the bypass capacitor C_E is increased from 0.047μF to 10μF, the lower cut off frequency f_E for different values of C_E will be, using the formulae at equations ...[5] and [6], for,

C_E = 0.047μF, f_E = 101.4 kHz.

C_E = 0.47μF, f_E = 10.1 kHz.

C_E = 4.7μF, f_E = 1014 Hz.

C_E = 10μF, f_E = 476.75 Hz.

C_E = 100μF, f_E = 47.675 Hz.

C_E = 470μF, f_E = 10.14 Hz.

C_E = 1000μF, f_E = 4.77 Hz.

From the above values, it is clear that, for the amplifier to work as an audio-amplifier(20Hz to 20 KHz), the minimum value of the bypass capacitor to be chosen should be 470μF.

Due to the different values of the coupling capacitors and bypass capacitors used, the values of $f_{C(in)}$, $f_{C(out)}$ and f_E may be different. Whenever such two or three different cut-off frequencies are obtained, then, the higher of the cut-off frequencies is more important. This is because it is at this frequency the first break in the amplifier response occurs. This frequency is called the dominant lower cut-off frequency f_{CL} of the amplifier.

Example : In the CE amplifier shown in Fig 7, if b is 100 and if the values of capacitors were $C_{C(in)}$ = 0.47μF, $C_{C(out)}$ = 0.47μF and C_E = 100μF, then the dominant lower cut off frequency f_{CL} would be,

$$R_{in} = R_1 \parallel R_2 \parallel \beta r'_e$$

where r'_e is the AC resistance of the transistor given by,

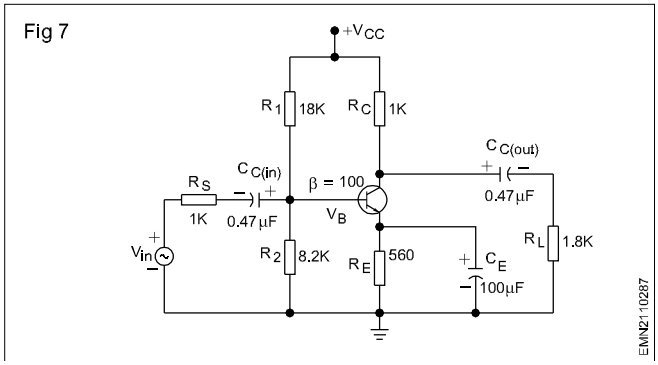
$$r'_e = \frac{25mV}{I_E}.$$

For the given circuit at Fig 7, Thevinins equivalence R_{TH} of resistors R_1 and R_2 is

$R_{TH} = R_1 \parallel R_2 = 5635.59\ \Omega$ and

$$V_{TH} = V_B = \frac{V_{CC} \cdot R_2}{R_1 + R_2} = 1.88 \text{ Volts}$$

Fig 7



Therefore, I_B is,

$$I_B = \frac{V_B - V_{BE}}{R_{TH} + (\beta + 1) R_E} = 18.97\ \mu A$$

Therefore, emitter current at Q point is,

$I_{EQ} = \beta I_B = 1.89$ mA.

Since , $I_{EQ} \spadesuit I_{CQ}$

$$r'_e = \frac{25mV}{I_E} = 13.2\,\Omega.$$

Therefore, $R_{in} = R_1 \parallel R_2 \parallel \beta r'_e = 1070$ W.

Lower cut-off frequency $f_{C(in)}$ due to input coupling capacitor $C_{C(in)}$ is given by,

$$f_{c(in)} = \frac{1}{2\pi (R_s + R_{in}) C_{c(in)}} = 163.67Hz.$$

Lower cut-off frequency $f_{C(out)}$ due to output coupling capacitor $C_{C(out)}$ is given by,

$$f_{c(out)} = \frac{1}{2\pi (R_c + R_L) C_{c(out)}} = 121Hz.$$

Lower cut-off frequency f_E due to bypass capacitor C_E is given by,

$$f_E = \frac{1}{2\pi(R_{out} C_E)}$$

where, $R_{out} \spadesuit r'_e + \frac{R_S \parallel R_1 \parallel R_2}{\beta}$

where, R_{out} = output resistance as seen by the bypass capacitor,

Therefore, R_{out} = 21.58W

Hence, f_E = 73.79 Hz.

Amongst the above calculated lower cut-off frequencies,

the dominant lower cut-off frequency is the highest of the calculated cut-off frequencies. i.e., 163 Hz due to the input coupling capacitor $C_{C(in)}$.

Hence, to improve the lower cut-off frequency of the amplifier, the value of $C_{C(in)}$ should be made larger.

Gain of the amplifier in the mid-range frequencies

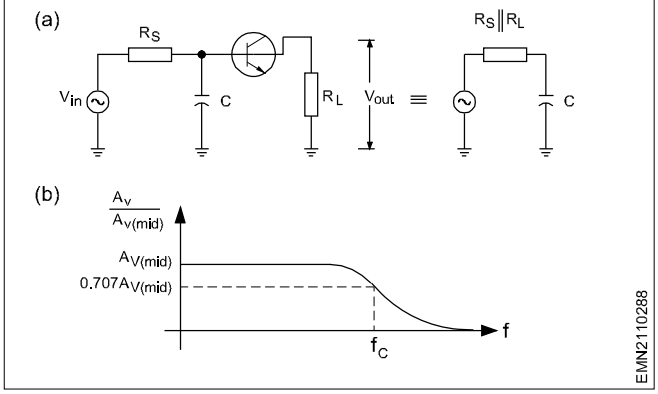
Above the dominant lower cut off frequency the gain of the amplifier remains almost constant over a wide range of frequencies, generally up to several tens of kilo hertz. But, once the input frequency becomes very high, the gain of the amplifier again reduces as shown in Fig 1.

High frequency response of CE amplifiers

Often capacitors come in parallel with the input and output of the amplifier. Then, at low frequencies, the capacitors behave as open circuits. But as the frequency increases the capacitors no longer behave as open and the output of the amplifier approaches zero.

Figs 8a and 8b, show the effect of capacitors coming in parallel with the amplifier.

Fig 8



At low frequencies, where the capacitor behave as open, the circuit acts like a voltage divider with a mid-band gain of,

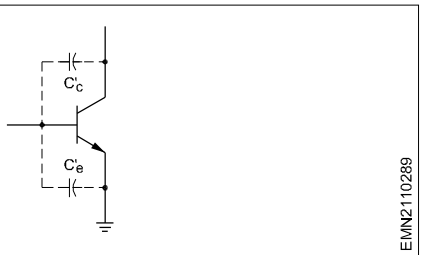
$$A_{mid} = \frac{R_L}{R_s + R_L}$$

At higher frequencies, the shunt capacitor begins to shunt ac current away from the load causing the voltage at the output to drop off.

In transistor amplifiers, the transistors will have internal capacitance C'_e across the emitter diode and C'_C across the collector diode as shown in Fig 9.

These internal capacitances of the transistors come in parallel with the input and output sections of the amplifier, and limit the highest frequency that can be amplified by an amplifier. Transistor data sheets give the values of internal capacitances of the transistors. The data sheets give another important data known as the current gain-band-width product, designated as f_T. This is the frequency at which the current gain of the transistor drops to unity.

Fig 9



Feedback in Amplifiers

Objectives: At the end of this lesson you shall be able to

- **state the meaning of the term feedback**
- **state the meaning and effect of degenerative feedback**
- **state the meaning and effect of regenerative feedback**
- **list the advantages of negative feedback in amplifiers**
- **state the equation for gain of the amplifier with a feedback**
- **calculate the feedback factor k from the circuit component values in a CE amplifier**
- **calculate the gain of a CE amplifier with and without feedback.**

Meaning and effect of feedback

The term feedback means, the output signal of a circuit is given back (fed back) to the input of the same circuit.

In feeding back the output signal to input, if the fed back signal is *180° out-of phase* with the input signal, then such a feedback is referred to as Negative feedback or degenerative feedback. This type of feedback is known as degenerative because, the fedback signal opposes the input signal lowering is magnitude. Hence, the gain of the amplifier decreases.

On the otherhand, if the fedback signal is in-phase with the input signal, then such a feedback is referred to as positive feedback or regenerative feedback. In a circuit with positive feedback, the fedback signal being in-phase with the input, increases the magnitude of the input signal resulting in high to very high gain of the amplifier. Positive feedback in amplifiers result in what is known as oscillations.

Although negative feedback results in reduced output of an amplifier, this type of feedback is extensively used in most of the electronic circuits because of the following advantages, negative feedback in amplifiers results in,

– stabilized voltage gain

– reduction in distortion of the amplifier output

– widening of the amplifier frequency band width

– increased input impedance

– reduced output impedance

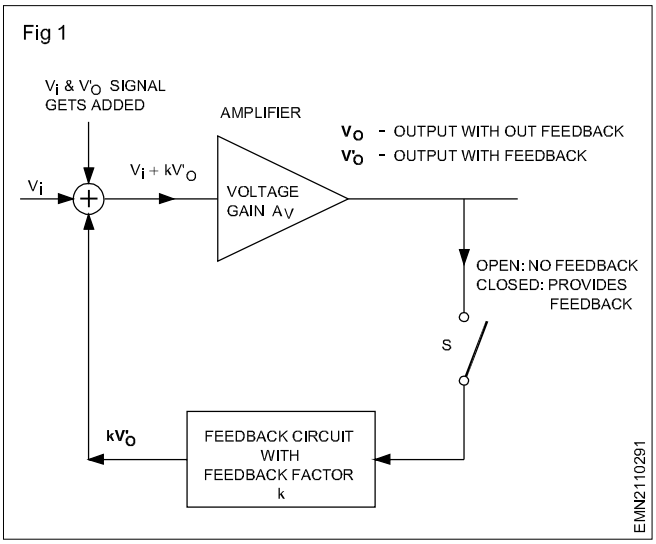
– reduced noise in amplifier.

All radios, tape recorders and televisions invariably use negative feedback in circuits for a function called Automatic volume control or Automatic gain control (AGC).

Positive feedback is used to generate AC signal using dc supply voltage in what are known as oscillators. Signal generators which generates sinusoidal signals invariably use positive feedback in their circuits.

Principle of negative feedback

The principle of feedback involving feeding a signal (voltage or current) back from the output of an amplifier or a system to the input of the amplifier is shown in Fig 1.



In Fig 1 above, if the feedback switch is open then there will be no feedback. The amplifier gain will then be,

$$A_V = \frac{V_0}{V_i}$$

If the feedback switch is closed, then a portion of the output gets added to the input and the new output of the amplifier would be V'_O.

If the feedback switch remains ON, then portion of the new output = kV'_O is added to the input V_i. Hence, the new input to the amplifier will be $V_i + kV'_O$.

If the phase of kV'_O is 180° out-of-phase with V_i then,

$V_i + kV'_O$ will be less than V_i. This is the condition of negative feedback.

If kV'_O happened to be in-phase with V_i, then, $V_i + kV'_O$ will be greater than V_i. This is the condition of positive feedback.

It can be shown that, the overall gain of the amplifier with the feedback being either positive or negative is given by,

$$A_{Vf} = \frac{V'_0}{V_i} = \frac{A_v}{1 - kA_v} \quad \text{..... [1]}$$

where,

A_{Vf} = voltage gain with feedback

A_v = voltage gain without feedback

k = feedback factor, usually between 0 and 1.

In the above equation, the term kA_v is known as the loop gain of the circuit. In negative feedback, kA_v is negative. Hence the denominator increases and, therefore, A_{Vf} decreases.

In regenerative or positive feedback kA_V, is positive; hence the denominator of equation [1] decreases, therefore A_{Vf} increases. This increase in A_{Vf} causes oscillations in the amplifier, and hence, converts the amplifier to an oscillator.

Example : If an amplifier has a voltage gain of –40 without feedback, find the gain of the amplifier with the following feedback:

(a) 10% negative feedback

(b) 20% negative feedback

(c) 1% positive feedback.

A negative sign in voltage gains indicates that output is 180° out of phase with the input.

Solution

(a) Gain of the amplifier without feedback, A_v=–40. With 10% negative feedback, the feedback factor k = 0.1 (10%).

Therefore, $kA_v = 0.1 \times -40 = -4$.

Using the formula at eqn.....[1]

$$A_{vf} = \frac{Av}{1 - kA_v} = \frac{-40}{1-(-4)} = \frac{-40}{5} = -8.$$

Note that the gain with 10% negative feed is much less than the gain without feedback.

(b) With 20% negative feedback

k = 0.2 (20%)

$kA_v = 0.2 \times -40 = -8$.

Therefore,

$$A_{vf} = \frac{A_v}{1 - kA_v} = \frac{-40}{1-(-8)} = \frac{-40}{9} = -4.4.$$

Note that the gain has further decreases with 20% negative feedback.

(c) With 1% positive feedback,

k = -0.01 (1%).

The negative sign for k value indicates that the output of the amplifier is further shifted by 180° such that the input V_i and the feedback signal are in phase.

Therefore, kA_v = -0.01 x -40 = + 0.4

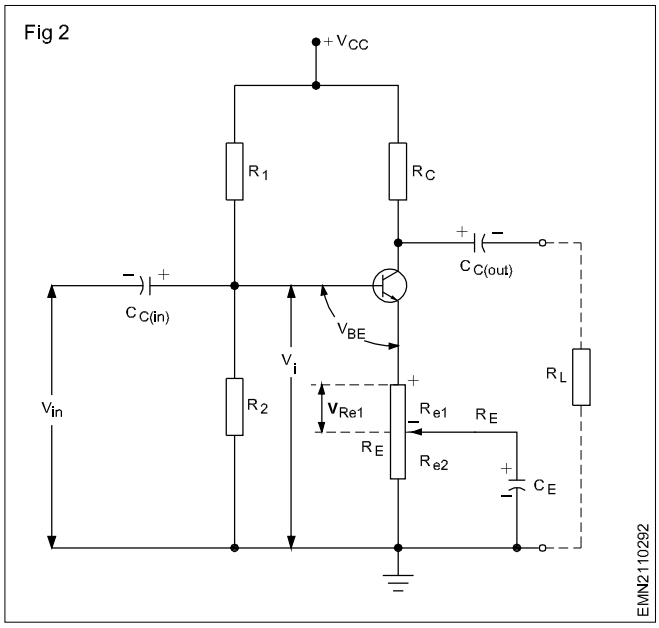
$$A_{Vf} = \frac{A_v}{1 - kA_v} = \frac{-40}{1-(+0.4)} = \frac{-40}{0.6} = -66.7.$$

Note that with positive feedback the overall gain of the amplifier has increased from –40 to –66.7.

Details of positive feedback is discussed in further lessons.

Negative feedback in common emitter amplifiers

Fig 2 shows one method of providing negative feedback in a common emitter amplifier.



In the amplifier at Fig 2, by not-bypassing the emitter resistor, an ac negative feedback occurs in the amplifier. The unshunted portion or the un-bypassed portion of the emitter resistor R_{e1}, has a voltage drop of V_{Re1}. This voltage V_{Re1} directly subtracts from the input voltage V_i, reducing the base emitter voltage of the transistor. That is, $V_{BE} = V_i - V_{Re1}$.

It can be shown that the amount of voltage feedback or feedback factor k is given by,

$$k = \frac{R_{e1}}{R_{out}}$$

where,

k is the feedback factor (dimension less)

R_{e1} is the un-bypassed emitted resistor in ohms.

R_{out} is the total ac load resistance = R_C / R_L in ohms.

Example: In the amplifier shown in Fig 2, R_C = 1 KW, R_E = 570W. When R_E is completely bypassed the input resistance of the amplifier R_{in} = 1070W. If transistor b is 100 calculate,

(a) Voltage gain without feedback

(b) Voltage gain without the emitter bypass capacitor

(c) Voltage gain when 180Ω of R_E is not bypassed

(d) Gain with feedback as in (c), with a load resistance R_L = 1KΩ.

Solution

(a) Given β or A_i, voltage gain A_v can be found using the formula,

Voltage gain, (A_v) = Current gain (A_i) x

$$\frac{\text{Output impedance } (R_{out})}{\text{Input impedance } (R_{in})}$$

Therefore,

$$A_v = \frac{R_{out}}{R_{in}} \approx \frac{R_{out}}{R_{in}} \beta$$

Since, in a CE amplifier, $R_{out} = R_C$

$$A_V = -\beta \frac{R_c}{R_{in}} = -100 \text{ x } \frac{1000}{1070} = -93.46.$$

(b) Voltage gain of the amplifier with the emitted bypass capacitor C_E, is not connected (with feedback).

$$k = \frac{R_E}{R_{out}} = \frac{R_E}{R_c} = \frac{570}{1000} = 0.57 \text{ or } 57\%$$

Therefore ,

$$A_{vf} = \frac{A_v}{1 - kA_v} = \frac{-93.46}{1-(0.57x - 93.46)} = -1.722.$$

(c) Voltage gain when 180ý of R_E is not bypassed (R_{e1} = 180Ω).

$$k = \frac{R_{e1}}{R_{out}} = \frac{R_{e1}}{R_C} = \frac{180}{1000} = 0.18 \text{ or } 18\%$$

Therefore ,

$$A_{vf} = \frac{A_v}{1 - kA_v} = \frac{-93.46}{1-(0.18 \text{ x} - 93.46)} = -5.24.$$

(d) When a load R_L = 1 KW is added, the voltage gain without feedback will change because, R_{out} now is,

$$R_{out} = R_C \| R_L = \frac{R_C R_L}{R_C + R_L} = 500\,\Omega.$$

The voltage gain without feedback with the new value of R_{out} is given by,

$$A_v = A_i \frac{R_{out}}{R_{in}} \approx -\beta \frac{R_{out}}{R_{in}} = -100 \text{ x } \frac{500}{1070} = -46.73$$

The feedback factor with new value of R_{out} is given by,

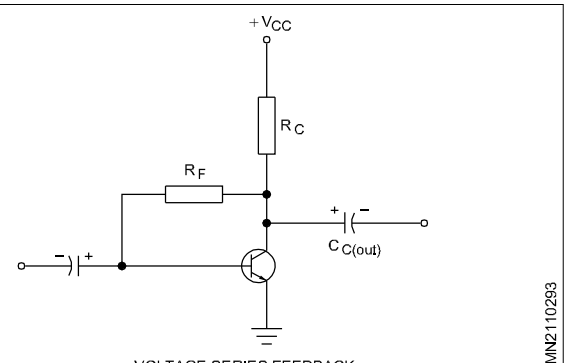
$$k = \frac{R_{el}}{R_{out}} = \frac{180}{500} = 0.36 \text{ or } 36\%$$

Therefore, gain with feedback R_{e1} and load R_L is given by,

$$A_{vf} = \frac{A_v}{1 - kA_v} = \frac{-46.73}{1-(0.36 \times -46.73)} = -2.62.$$

This type of negative feedback obtained in CE amplifiers, due to un-bypassed emitter resistor is known as *current series feedback*. In this type of feedback the output current ($I_C \simeq I_E$) is sampled and a proportional voltage (across unbypassed R_E) is made to come in series with the input. This type of feedback is also known as non-inverting current feedback because current at the input (Base) is in phase with the current at output (emitter) circuit.

Fig 3



VOLTAGE SERIES FEEDBACK

Fig 3 shows another type of negative feedback in a common emitter amplifier. This type of feedback is known as voltage series feedback.

The type of feedback shown in Fig 3, is also known as inverting voltage feedback. This method of connecting a resistor between the collector and base of a transistor resulting in a feedback is one of the methods of dc biasing of a transistor, and is also known as collector feedback configuration.

Other methods of negative feedback

In addition to the above discussed current series feedback and voltage series feedback, there are several other methods of providing negative feedback in amplifiers. Some of them are, voltage shunt feedback and current shunt feedback.

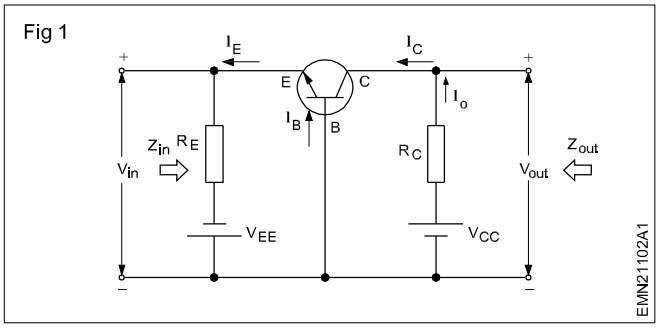
Common Base Amplifier

Objectives: At the end of this lesson you shall be able to

- **calculate the voltage gain,current gain,input impedance and output impedance of a common base amplifier**
- **list the typical applications of common base amplifiers.**

Fig 1 shows the typical circuit schematic of a **common base amplifier** (CB-amplifier).

Fig 1



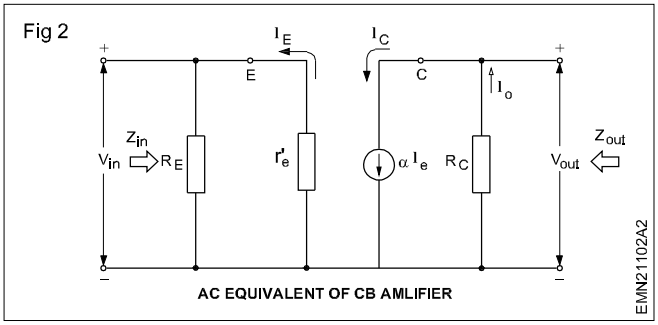
Common base amplifiers have a current gain of less than 1. Recall, the emitter current and the collector current of a transistor are almost equal. In a common base amplifier since the input current is I_E and the output current is I_C, the current gain, symbolically represented as a (alpha), is given by,

$$\text{Current gain } (\alpha) = \frac{\text{Output current}}{\text{Input current}} = \frac{I_C}{I_E}.$$

Since $I_E > I_C$, a will always be less than 1.

Fig 2 shows the ac equivalent of a common base amplifier, shown in Fig 1.

Fig 2



AC EQUIVALENT OF CB AMLIFIER

From Fig 2, the input impedance Z_{in} of CB amplifier is given by,

$$Z_{in} = R_E \parallel r'_e \qquad \text{.....\{1\}.}$$

Since R_E is generally much greater than r'_e, eqn..1 can be simplified as,

$$Z_{in} = r'_e$$

The equation for Z_{in} indicates that, the input impedance of a CB amplifier is very low and almost equal to the ac resistance r'_e of the emitter diode (recall r'_e will be generally 25Ω).

Referring to the AC equivalent network of the CB amplifier, the output impedance Z_{out} of CB amplifier is given by,

$$Z_{out} = R_C \qquad \text{.....\{2\}.}$$

Equation 2 indicates that the output impedance of a CB amplifier is relatively high, of the order of kilo ohms (because you can fix the value of R_C as you wish !).

From Fig 2, the output voltage V_{out} is

$$V_{out} = I_o R_C = I_c.R_C$$

Since $\alpha = \frac{I_C}{I_E}$, $I_C = \alpha.I_E$

Therefore, $V_{out} = I_C R_C = a.I_E.R_C$ .....{3}.

Since, $I_E = \frac{V_{in}}{r'e}$ equation 3 can be written as,

The voltage gain A_V of CB amplifier is given by,

$$A_V = \frac{V_{out}}{V_{in}} = \alpha \frac{V_{in}}{r'_e} R_C \frac{1}{V_{in}} = \alpha \frac{R_C}{r'_e} \quad .....\{4\}$$

Since r'_e is very small compared to R_C, the voltage gain A_V of the CB amplifier is quite high.

The power gain A_p of the CB amplifier is given by,

$$A_P = A_i.A_V$$

Power gain A_P will be medium because although A_i is less than or equal to 1, A_V of the CB amplifier is quite high.

Input/Output phase relationship

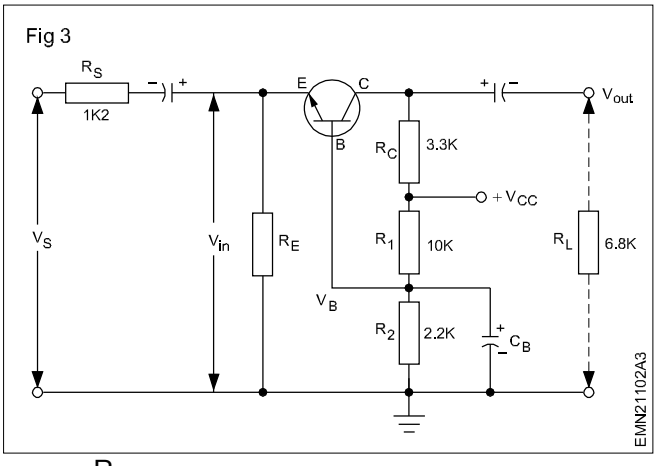
The input and output of a common base amplifier are in phase with each other. This can be found experimentally.

Fig 3 shows a CB amplifier with voltage divider bias.

In Fig 3, the base of the transistor is at ac ground due to the bypass capacitor C_B. The input signal drives the emitter and the output is taken from the collector. The biasing resistors R_1, R_2 will have negligible effect on the input impedance. Therefore, the input impedance of the CB amplifier is approximately equal to r'_e itself.

The voltage at the base (at T_1) is given by,

Fig 3



$$V_B = \frac{R_2}{R_1 + R_2} V_{cc}$$

$$= \frac{2.2K}{10K + 2.2K}.12V$$

$$= 2.16 Volts$$

The emitter current I_E is given by,

$$I_E = \frac{V_B - V_{EE}}{RE}$$

$$= \frac{2.16 - 0.7}{1.2K\Omega}$$

$$= 1.22mA$$

Therefore, r'_e is given by,

$$r'_e = \frac{25mV}{I_E}$$

$$= \frac{25mV}{1.22mA} = 20.5\Omega$$

Input impedance Z_{in} is given by,

$$Zin \approx r'_e = 20.5\Omega$$

The voltage gain A_v is given by,

$$A_v = \frac{R_c}{r'_e} = \frac{3.3K}{20.5} = 160.97 = 161\ \Omega$$

The output impedance Z_{out} is given by,

$$Z_{out} \approx R_c = 3.3K\Omega$$

The input V_{in} to the amplifier is given by (note that C_B bypas R_2 for AC signal),

$$V_{in} = \frac{r'_e}{R_s + r'_e} V_S$$

$$\frac{20.5\Omega}{1K\Omega + 20.5\Omega} 500mV = 10mV$$

Therefore the unloaded output voltage V_{out} is given by,

$V_{out(no\ load)} = A_v.V_{in}$

$= 161 \times 10mV$

$= 1610mV = 1.61$ volts

The output voltage of the amplifier with load R_L is given by,

$$V_{out\,(load)} = \frac{R_L}{R_C + R_L} x V_{out\,(noload)}$$

$$= \frac{6.8K}{3.3K + 6.8K} x1.61V = 1.08V$$

Class Room Assignment: Calculate the output voltage of the CB amplifier (as done in step above) if load resistor R_L was,

(i) R_L=3.3K

(ii) R_L=10K and,

(iii) R_L=100K

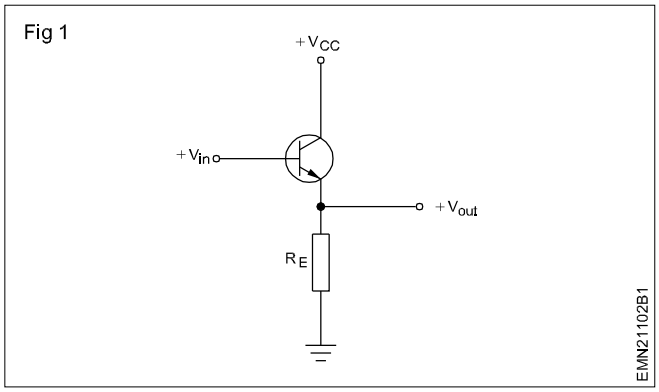
Emitter Follower

Objectives: At the end of this lesson you shall be able to

- **state the need for impedance matching**
- **state the popular application of an emitter follower amplifier configuration**
- **calculate the voltage gain, current gain, input impedance and output impedance of a transistor amplifier using circuit component values.**

Fig 1 shows another important transistor amplifier configuration. In this configuration, unlike in a common emitter amplifier where the output is taken from the collector, the output is taken from the emitter terminal of the transistor as shown in Fig 1.

Fig 1



Emitter follower can be used, to match a high impedance source to a low impedance output load. Hence, the emitter follower configuration is frequently used as an impedance matching circuit than as an amplifier.

Need for impedance matching

When a high impedance source is connected to a low impedance load, then most of the ac signal of the source gets dropped across the internal impedance of the source itself resulting in a very small portion of the signal appearing across the required load as shown in Fig 2a. One way to overcome this problem, i.e. to have almost all the signal from the source to be developed across the load, is to use an impedance matching device or a circuit between the high impedance source and the low impedance load as shown in Fig 2b.

The circuit used for impedance matching in Fig 2b, is an emitter follower transistor amplifier. This is because, the emitter follower has a very high input impedance and a very low output impedance. This can be compared to that of a matching transformer where a load is matched to the source impedance for maximum power transfer.

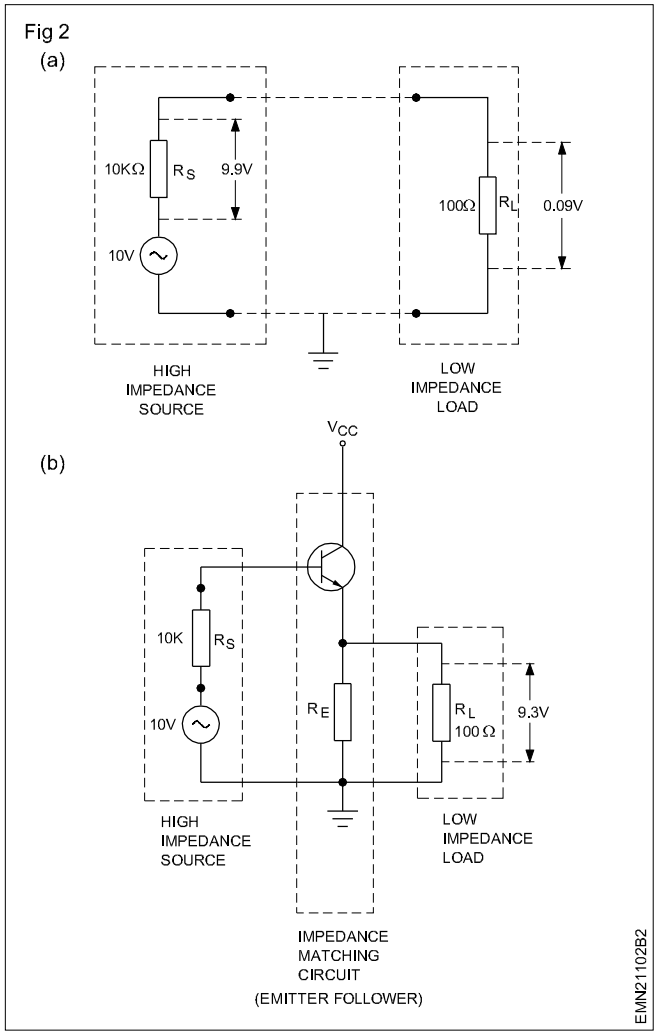
An emitter follower circuit is also called a common collector *amplifier* because, the collector behaves as the common terminal for ac signal between the input and the output.

Voltage gain of an emitter follower

As can be seen in Fig 3, the DC output voltage of the emitter follower is $V_{out} = V_{in} - V_{BE}$

Since, V_{BE} is almost a constant value (0.7 for silicon, 0.3 for germanium) the emitter voltage follows the base voltage. It is because the emitter voltage follows the base voltage, this circuit is called **emitter follower.**

Fig 2



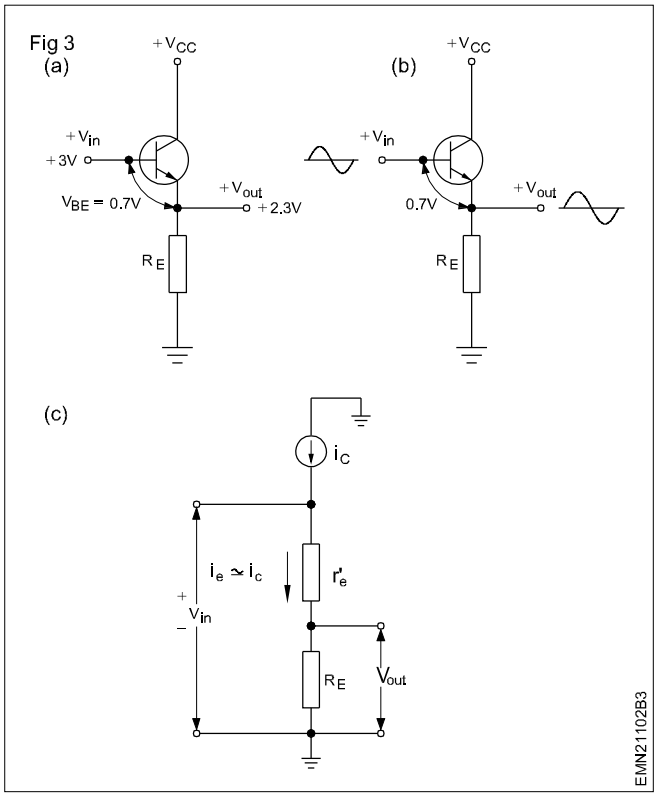
In Fig 3, if V_{in} is 3V, then V_{out} = 2.3V. If V_{in} is made 4\| then V_{out} increases to 3.3V. This means that changes in V_{out} is in phase wiwê changes in V_{in}. Therefore in an emitter follower the input and output signals are in phase as shown in Fig 3b. (recall, in a CE amplifier the input and output are 180° out of phase.)

Fig.3c shows the ac equivalent circuit of the emitter-follower shown in Fig 3a. The AC output voltage V_{out} is given by,

$$V_{out} = i_e R_E$$

Since the AC input voltage V_{in} is given by, $V_{in} = i_e (R_E + r'_e)$ the voltage gain A_V of the emitter follower is,

$$A_v = \frac{V_{out}}{V_{in}} = \frac{i_e R_e}{i_e (R_e + r'_e} = \frac{R_E}{R_E + r'_e} \quad \text{..... (1)}$$



In equation {1}, since the denominator will always be higher than the numerator, the value of voltage gain A_V will always be less than 1.

But since the value of r'_e is very small compared to R_E, the value of A_V approaches unity. We can therefore say that the voltage gain of the emitter follower is unity.

In Fig 3a, if $R_E = 4.7K\Omega$ and $r'_e = 25W$ then,

$$A_v = \frac{R_E}{R_E + r'_e} = \frac{4700}{4700 + 25} = 0.995 \approx 1$$

Input impedance of emitter follower

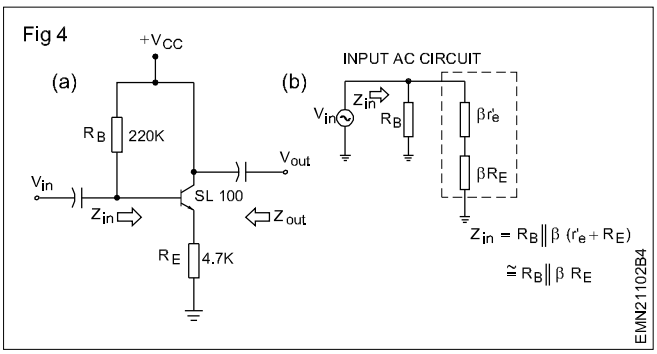
The input impedance of the emitter follower shown in Fig 3 is given by,

$$Z_{in} = \beta(R_E + r'_e) \qquad \text{..... \{2\}}$$

Since r'_e will be generally very small compared to R_E, equation ...{2} can be simplified as,

$$Z_{in} = \beta R_E$$

Fig 4a shows a practical emitter follower circuit using fixed biasing. The total input impedance including the biasing



resistor R_B in parallel with the input impedance can be found as follows;

Writing the AC equivalent of the input of the emitter follower shown in Fig 4b, the input impedance Z_{in} is given by,

$$Z_{in} = R_B \parallel \beta(r'_e + R_E) \qquad \text{.....\{3\}}$$

If r'_e is neglected,then, $Z_{in} = R_B \parallel \beta R_E$

Equation 3 indicates that the input impedance of a typical emitter follower is decided by the DC biasing resistance R_B. Hence, while designing an emitter follower to match a high source impedance, the values of R_B should be suitably chosen.

Example: In the emitter follower at Fig 4, if β of transistor is 100, R_B = 220 k and R_E = 4.7k the input impedance will be,

$$Z_{in} = R_{in} = R_B \parallel \beta R_E$$

$$= 220\ K \parallel \beta R_E$$

$$= 220\ K \parallel (100 \times 4.7K)$$

$$= 149.85\ K\ \Omega\ 150\ K\Omega$$

Output impedance of emitter follower

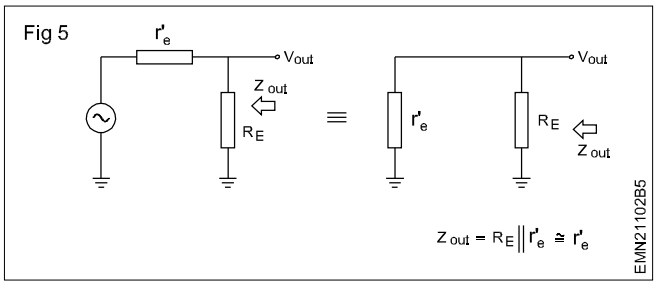


Fig 5 shows an AC equivalent or AC model of the output section of an emitter follower shown in Fig 4a.

Analysing Fig 5, the output impedance Z_{out} is given by,

$$Z_{out} = R_E \parallel r'_e \qquad \text{.....\{4\}}$$

Since R_E is usually a large resistance compared to r'_e, R_E in equation (4) can be neglected. Therefore, the output impedance of an emitter follower is approximately,

$$Z_{out} = r'_e$$

Example 1: Find the output impedance of the emitter follower shown in Fig 4 assuming $r'_e = 33\Omega$,

$$Z_{out} = r'_e \parallel R_E \quad r'_e = 33\Omega.$$

Current gain in emitter follower

Although the voltage gain A_V of emitter follower is approximately unity, the current gain of an emitter follower is high and is given by the equation;

$$A_i = \frac{\beta R_B}{(R_B + \beta R_E)} \quad \text{.....\{5\}}$$

Example 2*:* In the emitter follower shown in Fig 4, if β of the transistor is 100, then the current gain of the emitter follower is given by,

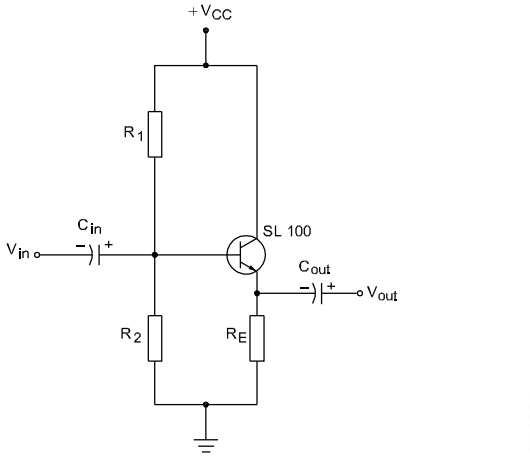
$$A_i = \frac{\beta R_B}{(R_B + \beta R_E)}$$

$$= \frac{(100)\ (220K)}{(220K) + (100)\ (4.7K)} = 31.88.$$

The current gain of the emitter follower can also be found as follows;

$$A_i = A_V \frac{Z_{in}}{R_E} = (0.995) \frac{150K}{4.7K} = 31.72.$$

Fig 6



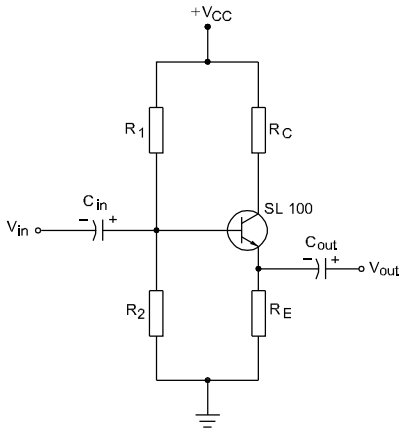
EMITTER-FOLLWER WITH VOLTAGE DIVIDER BIAS

Fixed bias was used in the emitter follower shown in Fig 4. Any other DC biasing could also be employed such as voltage divider bias as shown in Fig 6.

When voltage divider bias is used in an emitter follower, the equations for finding A_V, Z_{in}, Z_{out} and A_i remain the same, except for, that the fixed biased resistor R_B replaced by $R_1 \| R_2$.

Fig 7 which includes a collector resistor R_C also provides the input-output characteristics of an emitter follower. The input impedance Z_i and the output impedance Z_o are not effected by R_C since it is not reflected into the base or emitter equivalent network of the circuit. The only use of R_C will be to fix the quiescent collector current or Q point of the transistor.

Fig 7



Darlington Pair

Objectives: At the end of this lesson you shall be able to

- **define darlington pair**
- **calculate the current gain of darlington pair**
- **state the advantages and disadvantages of darlington pair**
- **define sziklai transistor pair.**

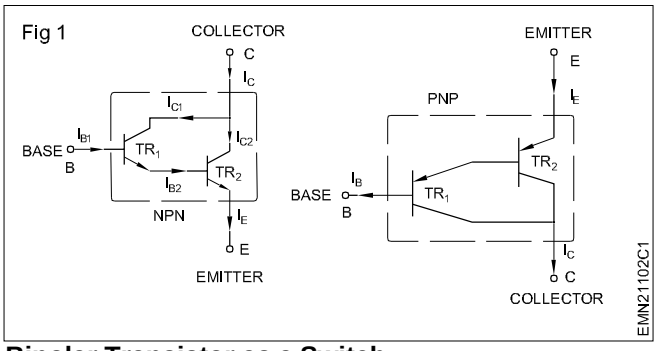
Darlington Transistors

Darlington Transistor pairs can be made from two individually connected bipolar transistors or a one single device commercially made in a single package with the standard: Base, Emitter and Collector connecting leads and are available in a wide variety of case styles and voltage (and current) ratings in Both NPN and PNP versions of dalington pair is shown in Fig1.

The Emitter of one transistor is connected to the Base of the other to produce a more sensitive transistor with a much larger current gain being useful in applications where current amplification or switching is required.

As we saw in our transistor as a switch tutorial, as well as being used as an amplifier, the bipolar junction transistor,(BJT) can be made to operate as an ON-OFF switch as shown.

Fig 1



Bipolar Transistor as a Switch

When the base of the NPN transistor is grounded (0 volts) and no base current, Ib flows,no current flows from the emitter to the collector and the transistor is therefore switched “OFF”. If the base is forward biased by more than 0.7 volts,a current will flow the emitter to the collector

and the transistor is said to be switched “ON”. When operated in these two modes, the transistor operator as a switch.

The problem here is that the transistors Base needs to be switched between zero and some large, positive value for the transistor to become saturated at which point an increased base current, Ib flows into the device resulting in collector current Ic becoming large while Vce is small. Then we can see that a small current on the base can control a much larger current flowing between the collector and the emitter.

The ratio of collector current base current (β) is known as the current gain of the transistor. A typical value of for a standard bipolar transistor may be in the range of 50 to 200 and varies even between transistors of the sam e part number. In some cases where the current gain of a single transistor is tooo low to directly drive a load, one way to increase the gain is to use a Darlington pair.

A **Darlington Transistor** configuration, also known as a "Darlington pair" or "super-alpha circuit", consist of two NPN or PNP transistors connected together so that the emitter current of the first transistor TR1 becomes the base current of the second transistor TR2. Then transistor TR1 is connected as an emitter follower and TR2 as a common emitter amplifier as shown in Fig1.

Also note in this darlington pair configuration, the colector current of the slave or control transistor, TR1 is “in - phase” with that of the master switching transistor TR2.

Basic Darlington Transistor Configuration

Using the NPN Darlington pair as the example, the collectors of two transistors are connected together, and the emitter of TR1 drives the base of TR2. This configuration achieves β multiplication because for a Base current ib, the collector current is β* ib where the current gain is greater than one, or unity and this is defined as:

$$I_C = I_{C1} + I_{C2}$$
$$IC = \beta_1 . I_B + \beta_2 . I_{B2}$$

But the base current, I_{B2} is equal to transistor TR1 emitter current, I_{E1} as the emitter of TR1 is connected to the base of TR2. Therefore.

$$I_{B2} = I_{E1} = I_{C1} + I_B = \beta_1 . I_B + I_B = (\beta_1 + 1) . I_B$$

Then substituting in the first equation:

$$I_C = \beta_1 . I_B + \beta_2 . (\beta_1 + 1) . I_B$$
$$I_C = \beta_1 . I_B + \beta_2 . \beta_1 . I_B + \beta_2 . I_B$$
$$I_C = (\beta_1 + (\beta_2 . \beta_1) + \beta_2) . I_B$$

Where β_1 and β_2 are the gains of individual transistors.

The overall current gain, β is given by the gain of the first transistor multiplied by the gain of the second transistor as the current gains of the two transistors multiply. In other words, a pair of bipolar transistors combined together to make a single Darlington transistor pair can be regarded as a single transistor with a very high value of β and consequently a high input resistance.The base of the Darlington transistor is sufficiently sensitive to respond to any small input current from a switch or directly from a TTL or 5V CMOS logic gate. The maximum collector current Ic(max) for any Darlington pair is the same as that for the main switching transistor, TR2 so can be used to operate relays, DC motors, solenoids and lamps, etc.as shown in Fig.---

Darlington Transistor Example No 1

Two NPN transistors are connectod together in the form of a Dralington Pair to switch a 12V 75W halogen lamp. If the forward current gain of the first transistor is 25 and the forward current gain (Beta) of the second transistor is 80. Ignoring any voltage drops across the two transistors, calculate the maximum base current required to switch the lamp fully- ON.

Firstly, the current drawn by the lamp will be equal to the Collector current of the second transistor, then:

$$I_C = I_{LAMP}$$
$$\therefore I_{LAMP} = \frac{P}{V} = \frac{75}{12} = 6.25 \text{ Amps}$$

Using the equation above, the base current is given as:

Fig 2

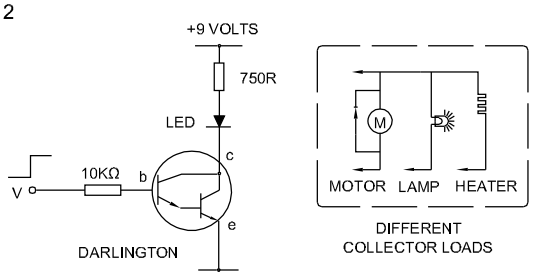
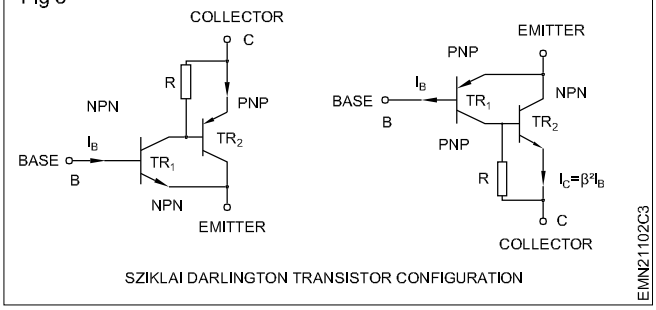


Fig 3



The base of the Darlington transistor is sufficiently sensitive to respond to any small input current from a switch or directly from a TTL or 5v CMOS logic gate. The maximum collector current Ic (max) for any darli ngton pair is the smae as that for the main switching transistor, TR_2 so can

be used to operate relays, DC motore, solenoids and lamps,ect as shown in Fig 2.

One of the main disadvantage of a Darlington transistor pair is the minimum voltage drop between the base and emitter when fully saturated. Unlike a single transistor which has a saturated voltage drop of between 0.3v and 0.7v when fully-ON, a Darlington device has twice the base-emitter voltage drop (1.2 V instead of 0.6 V) as the base-emitter voltage drop is the sum of the base-emitter diode drops of the two individual transistors which can be between 0.6v to 1.5v depending on the current through the transistor.

This high base-emitter voltage drop means that the Darlington transistor can get hotter than a normal bipolar transistor for a given load current and therefore requires good heat sinking. Also, Darlington transistors have slower ON-OFF response times as it takes longer for the slave transistor TR_1 to turn the master transistor TR_2 either fully-ON or fully-OFF.

To overcome the slow response, increased voltage drop and thermal disadvantages of a standard **Darlington Transistor** device, complementary NPN and PNP transistors can be used in the same cascaded arrangement to produce another type of Darlington transistor called a **Sziklai Configuration.**

Sziklai Transistor Pair

The Sziklai Darlington Pair, named after its Hungarian inventor George Sziklai, is a complementary or compound Darlington device that consists of separate NPN and PNP complementary transistors connected together as shown in Fig 3.

This cascaded combination of NPN and PNP transistors has the advantage that the Sziklai pair performs the same basic function of a Darlington pair except that it only requires 0.6v for it to turn-ON and like the standard Darlington configuration, the current gain is equal to β^2 for equally matched transistors or is given by the product of the two current gains for unmatched individual transistors.

We can see that the base - emitter voltage drop of the Sziklai device is equal to the diode drop of a single transistor in the signal path. However, the Sziklai configuration can not saturate to less than one whole diode drop, i.e.0.7v instead of the usual 0.2v.

Also , as with the Darlington pair, the Sziklai pair have slower response times than a single transistor. Aziklai pair complementary transistors are commonly used in push - pull and class AB audio amplifier output stages allowing for one polarity of output transistor only. Both the Darlington adn Sziklai transistor pairs are avilable in both NPN and PNP configurations.

Advantages

- Very high current gain
- Very high input impedance for overall circuit
- Darlingtor pairs are widely available in a single package or they can be made from two separate transistors
- Convenient and easy circuit configuration to use

Disadvantages

- Slow switching speed
- Limited bandwidth
- Introduces a phase shift that can give rise to problems at certain frequencies in circuit using negative feedback
- Higher overall base - emitter voltage =Vbe.
- High saturation voltage (typically around 0.7 V)which can lead to high levele of power dissipation in some applications

The Darlington pair transistor circuit configuration can be very useful in electronics circuit design. Although it has speed limitations, the circuit nevertheless very useful in many areas where high levels of current gain are required, particularly for emitter follower style applications.

Types of Cascaded Audio Amplifiers

Objectives: At the end of this lesson you shall be able to

- **state the need for cascading amplifiers**
- **state the need for coupling between the stages of amplifiers**
- **list the applications, advantages and disadvantages of direct-coupled amplifiers.**

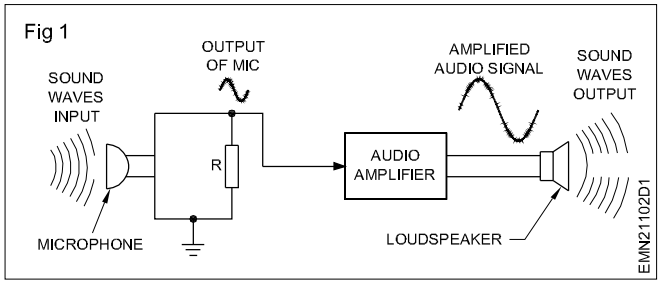
Cascaded audio frequency (A.F.) amplifiers

Amplifiers specially designed to amplify audio frequency signals (16Hz to 16kHz) are called to as audio frequency amplifiers or A.F. amplifiers.

Single transistor amplifiers discussed in unit 09 do not provide enough gain to be used with output transducers such as speakers. Therefore, several amplifiers are usually connected in series (cascaded) as shown in Fig.2 to obtain sufficient gain to drive a speaker.

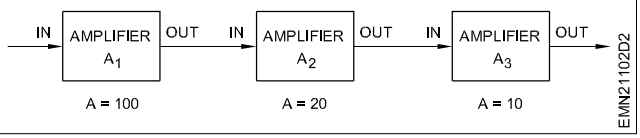
In Fig 2, the output of one amplifier, serves as the input for

Fig 1



the next amplifier, and so on, till the required gain is obtained. Although the individual amplifiers can be of any configuration, the most commonly used is the common-

Fig 2



emitter configuration especially in A.F amplifiers. This is because of the fact that, the voltage, current and power gain of CE amplifier is high.

In Fig 2, if the gain of stage A_1 is 100, A_2 is 20 and A_3 is 10, then the overall gain or the total gain of the cascaded amplifier will be,

= Gain of A_1 x Gain of A_2 x Gain of A_3 ..[2]

Total gain = 100 x 20 x 10 = 20,000

For instance, if stage A_1 is given an input signal of strength 1mv, the output signal level will be 20 V. Such cascaded amplifiers are also referred to as *multi-stage amplifiers*.

Such cascaded or multi-stage amplifiers are common in almost all A.F amplifiers used in tape recorders, public address amplifiers and so on.

Methods of coupling

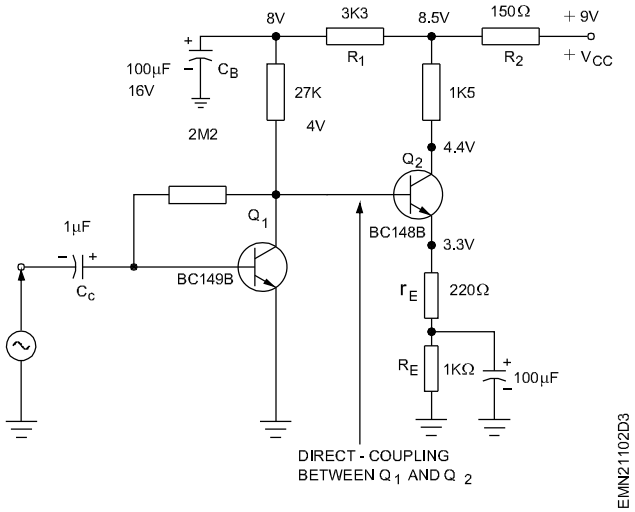
As shown in Fig. 2, in cascaded amplifiers the output of one amplifier stage has to be fed to the input of the next amplifier stage. While doing so, it is important to match the impedance between the two stages. It is even more important to have good impedance matching in low-level signal stages (initial amplifier stages) so that very little signal is lost in the process of feeding. This technique of connecting the output of one amplifier stage to the input of the next amplifier stage, such that, the impedance of the stages are matched enabling maximum transfer of signal from one to other is known as *coupling*.

There are several methods of coupling. A few of the most common methods of coupling are discussed in subsequent paragraphs:

Direct coupling

A typical direct coupled amplifier is shown in Fig 3.

Fig 3



In Fig 3, the collector of the first transistor, (first amplifier stage output) is connected directly to the base of the second transistor (second amplifier stage input). Since no components such as capacitors, transformers are used between the output of one stage and the input of another, this method of coupling is known as *direct coupling*. As there are no components involved in coupling, both the DC component of the signal and the AC component of the signal are passed to the input (base) of the 2nd amplifier. Also, since there are no frequency restricting components in the path of coupling, there is no frequency restriction in the coupled path.

In Fig 3, transistor Q_1 is self-biased. If β_{dc} of Q_1 = 100, then, the quiescent collector current I_C is given by,

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B \beta_{dc}} = \frac{8V - 0.7V}{27K + (2M2/100)} = 0.15mA$$

The advantage of using self-bias (feed-back bias) is that the transistor can never reach saturation, and hence, the distortion is minimum.

Please note that it is not compulsory to use self-bias. You may use divider bias also for Q_1. However, in most amplifier circuits the first amplifier stage generally use self-bias to prevent transistor getting saturated.

I_C of 0.15mA produces a drop of approximately 4 V across 27 K. Therefore, collector of Q_1 will be at 4V with respect to ground. Allowing 0.7 V for the emitter diode of Q_2, 3.3 V will be across 1 kΩ. Hence I_C of Q_2 is approximately 2.75 mA.

The voltage gain of the first stage (Q_1) is,

$$A_1 = \frac{R_C}{r'_{e_1}}$$

$$r'_{e_1} = \frac{25mV}{I_{E1}} = \frac{25mV}{0.15mA} = 166.7\ \Omega$$

Therefore,

$$A1 = \frac{27KW}{166.7W} \approx 162$$

The voltage gain of the second state (Q_2) is,

$$A_2 = \frac{R_C}{r_E + r'_{e2}}$$

$$= r'_{e2} = \frac{25mV}{I_{E2}} = \frac{25mV}{2.75mA} = 9.09\ \Omega$$

$$A_2 = \frac{1K5\ \Omega}{220\ \Omega + 9.09\ \Omega} = 6.55$$

The overall gain of the two stages is,

$A_{12} = A_1 \times A_2 = 162 \times 6.55 = 1061.1$

Although the theoretical gain is very high, due to resistance tolerance variations and impedance mis-matching, in practice A_{12} will be slightly lower.

DC potentials

In Fig 3, it is very important to note, that there is no separate DC biasing provided to the transistor Q_2. This is because, the base of the transistor Q_2 is at the same DC potential as the collector of Q_1 (4V).

Resistors R_1(3K3) and R_2(150Ω) are provided to obtain suitable DC voltages for the different stages of the amplifier using a common V_{CC} supply of +9Volts.

Applications of direct-coupled amplifiers

– For amplification of DC control voltages in industrial electronic applications (DC amplifiers).

– At the input stages of audio-amplifiers for good low frequency response down to 0Hz.

– In some applications, direct coupling is used just for economy, as this method eliminates the need of coupling capacitors.

– Direct coupling is used in circuits known as complemetary-symmetry which use PNP and NPN transistors.

Complemetry symmetry configuration is discussed in further lessons.

Disadvantages of Direct coupling

– Each successive stage of amplifiers needs progressively higher supply voltages. (V_{CC} of Q_1 and Q_2 in Fig 3.)

– Transistor characteristics like V_{BE} vary with temperature. This causes collector currents and voltages to change.

– Any undesired change in dc voltage in Q_1 affects all the potentials for Q_2.

– The power supply must provide very good filtering of the 50 Hz ripple (Hum), which otherwise will be amplified by the direct coupled amplifier (DC amplifier).

RC, LC Transformer Coupling

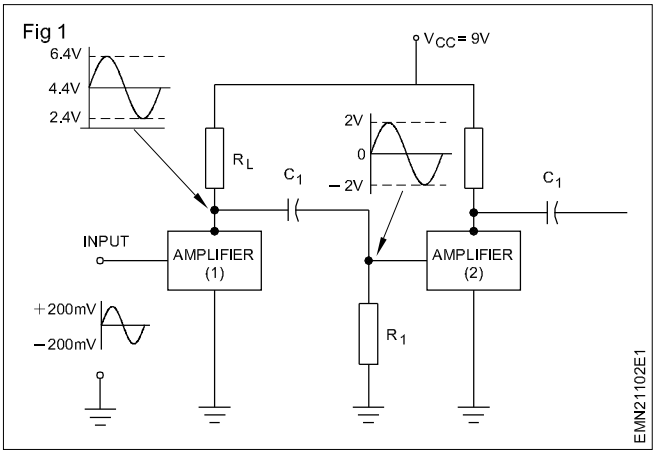
Objectives: At the end of this lesson you shall be able to

- **explain how DC is blocked and AC is coupled in AC coupling**
- **explain the effect of coupling capacitor on the frequency response of the amplifier**
- **explain LC coupling, its advantages, disadvantages and applications**
- **explain transformer coupling, its advantages and limitations.**

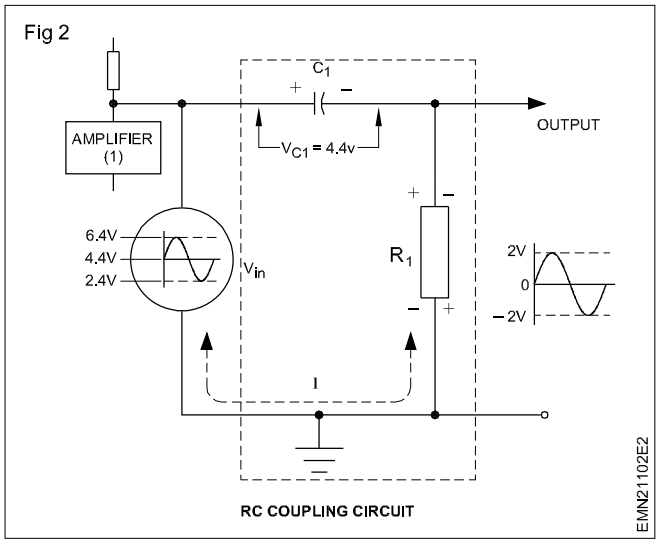
Very popular method of coupling is known as Resistance-Capacitance (RC) coupling. Amplifiers using this type of coupling are called RC coupled amplifiers.

Resistance - capacitance (RC) coupling

Fig 1 shows the method of RC coupling between amplifier stages.



The output of amplifier-1 is fed through, the C_1R_1 coupling circuit, to the input of amplifier-2. The R_1C_1 coupling is shown separately in Fig 2 for analysing how the DC component is blocked and only the AC signal variations is passed on to the next amplifier.



In Fig 2, V_{in} is the output of the amplifier (at output of A_1) and is also the input to the coupling circuit formed by C_1R_1. In Fig 2, the values of V_{in} are:

Average DC voltage level	= +4.4 V
AC variations around 4.4 V	= ±2 V
Maximum instantaneous value	= +6.4 V
Minimum instantaneous value	= –2.4 V

With no input AC signal, the capacitor is charged to DC level of 4.4 V as shown in Fig 2. Since all the voltage is across C_1, the voltage across R_1 with respect to ground is zero. This is shown as the x axis reference at the output terminals.

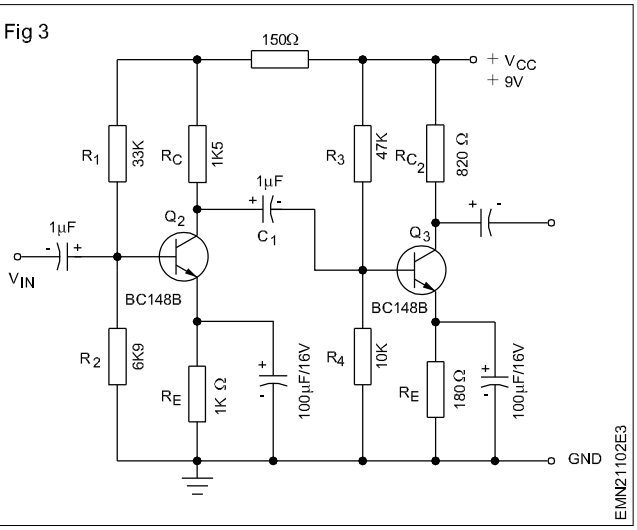
When V_{in} rises to 6.4V, C_1 charges above 4.4 V and up to the maximum instantaneous value of +6.4V. The charging current through R_1 produces a positive voltage drop across R_1. All the changes of V_{in} between 4.4V to 6.4V provide a +ve half cycle of 2 volts across R_1 as shown in Fig 2.

When V_{in} falls below 4.4 V, C_1 discharges. The discharge current through R_1 produces negative voltage across R_1. All changes of V_{in} between 4.4 V and 2.4 V provide a negative half cycle across R_1 as shown in Fig 2.

Therefore, from Fig 2, it can be seen that the voltage across R_1 is equal to only the magnitude of changes that occurred on the DC value of 4.4V at the input of the R_1C_1 network. The DC 4.4V is blocked across capacitor C_1 of the R_1C_1 network. Hence, the available output of R_1C_1 network or input to the next stage amplifier, (Amplifier 2 in Fig 1) is only the ± variations of the AC signal at the collector of amplifier 1.

It is important to note that the frequency of input signal is such that the capacitive reactance of X_{C1} is very small compared to R_1. Alternatively, the value of C_1 should be high enough such that X_{C1} is negligible compared to R_1 for the input signal frequency range. Otherwise a major portion of the AC signal gets dropped across X_{C1} and not across R_1. If so the input to the next amplifier stage (A2) will be much less than the output of the previous stage (A1).

Fig 3



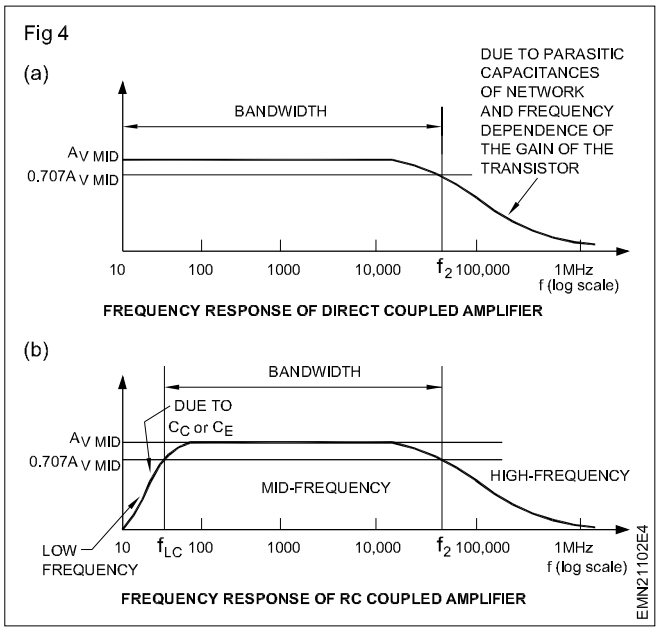
RC coupling is a very popular method of coupling in almost all A.F amplifiers. Fig 3 shows a two stage RC coupled amplifier.

In RC coupling since DC voltage at collector Q_2 is blocked by capacitor C_1, transistor Q_3 is given separate DC bias voltage using resistors R_3 and R_4. R_3 and R_4 provide a DC bias voltage of 1.5 V at the base of Q_2 in Fig 3.

Frequency-response of RC-amplifiers

Fig 4 shows the frequency-gain responses of a typical direct coupled and RC coupled amplifiers.

Fig 4



In the frequency response curve of a direct-coupled amplifier shown in Fig 4a, the response is a flat from almost 0Hz up to the upper cut-off frequency. Indirect coupled amplifiers the upper cut-off frequency is determined by, either the parasitic capacitance of the circuit or the dependence of the gain of the active device (transistor) used. There is no lower cut-off frequency as there are no coupling capacitor to cause drop in gain at low frequencies.

In the frequency-response curve of an RC-coupled amplifier shown in Fig 4b, there is drop in gain at low frequencies. This is due to, the increased reactance of coupling capacitor C_1. The upper frequency limit in RC-coupled amplifiers is again determined by the parasitic capacitance of the circuit and the frequency dependence of the gain of the active device (transistor).

In the RC coupled amplifier circuit at Fig 3, the 3db low frequency cut-off f_{LC}, of the amplifier due to the RC coupling between transistors Q_2 and Q_3 is given by,

$$f_{LC} = \frac{1}{2\pi(R_c + R_{in})C_c}$$

where,

R_C is the collector resistor of Q_2

R_{in} is the input impedance of Q_3

C_C is the value coupling capacitor C_1 used between Q_2 and Q_3.

$$Z_{in} \text{ or } R_{in} \text{ of } Q_3 = R_3 \parallel R_4 \parallel \beta_{Q3} r'_{e(Q3)} \approx \beta_{Q3}\, r'_{e(Q3)}$$

$$r'_{e2} = \frac{25mV}{I_{E(Q3)}} = \frac{25mV}{5mA} = 5\Omega$$

If β_{dc} of Q_3 = 100

then,

β_{Q3}. $r'_{e(Q3)}$ = 500Ω

Therefore,

$$FLC = \frac{1}{2\pi(1K5+500\Omega)x10^{-6}} \approx 80 \text{ Hertz.}$$

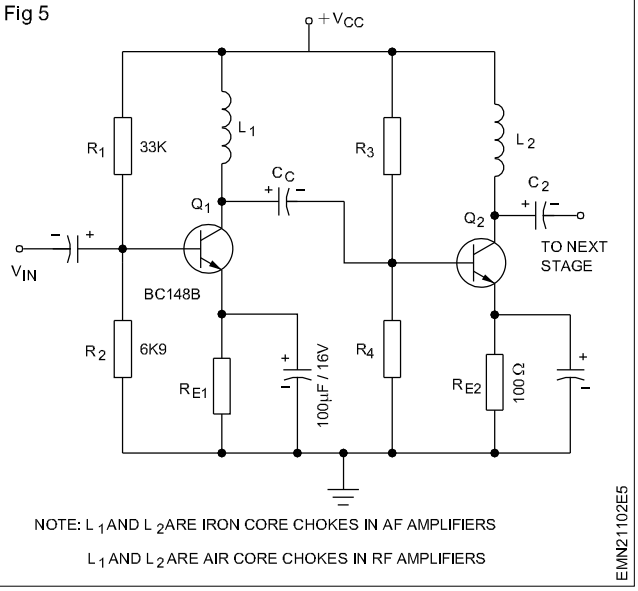
Refer previous unit on transistors where the effect of coupling and bypass capacitors on frequency response are discussed.

The low gain at low frequencies, imposed by the coupling capacitor is the major disadvantage of RC coupled amplifiers. However, RC coupling of amplifier stages overcome the disadvantages associated with the DC coupled amplifiers such as, need of progressively higher supply voltages and the changes in DC supply resulting in undesirable changes in amplifier output.

LC coupling or Impedance coupling

Fig 5 shows a Inductance-Capacitance (LC) coupled amplifier, in which, an inductance is used as the collector load of the amplifier instead of a resistor. However, C_C is still required to block the DC voltage.

Fig 5



Iron core chokes L_1 and L_2 are used in A.F amplifiers, whereas air-core chokes are used in high frequency (HF) amplifiers.

The advantage of using a choke in the collector is its low DC resistance but high AC impedance. Low dc resistance results in small I_R drop, which allows most of V_{CC} to be available at the collector of the transistor amplifier. The high ac impedance for the signal results in high gain.

The disadvantages of LC coupling are,

– For A.F amplifiers, the physical size of suitable inductance value chokes will be bulky and occupies large space.

– Since the impedance of an inductor varies with frequency (X_L = 2pfL), LC amplifiers do not have uniform frequency response.

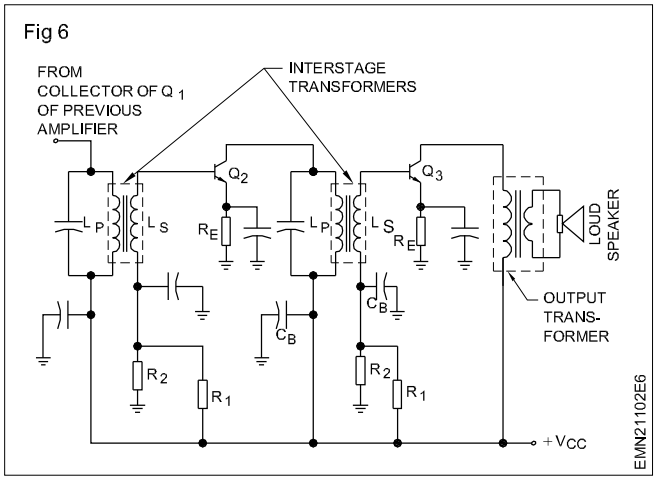
– LC coupling is expensive compared to RC coupling.

Although LC coupling is rarely used in AF amplifiers, LC coupling is extensively and invariably used in radio frequency amplifiers (RF) in which frequencies much above a few hundred KHz is used. At such high frequencies the physical size of L will be very small.

Transformer coupling

Fig 6 shows a transformer-coupled amplifier.

Fig 6



The primary winding L_P of the transformer provides the necessary load impedance for the amplifier as in LC or impedance coupling. The AC signal current in L_P induces signal voltage in L_S by transformer action. Since L_S is an isolated winding, the DC component of the primary voltage and current is not transferred to L_S and hence to the next amplifier stage.

Resistors R_1 and R_2 provide the necessary DC bias for the transistors. The bypass capacitors C_B at the bottom of each primary and secondary winding provide AC ground. Hence AC signals get transferred from one stage to the subsequent stage only through transformer action.

In audio amplifiers, transformer coupling may be used between two amplifier stages or at the last stage to drive a loud speaker as shown in Fig 6. Audio output transformers are generally voltage step-down to match low impedance values of the speaker (4 to 16W).

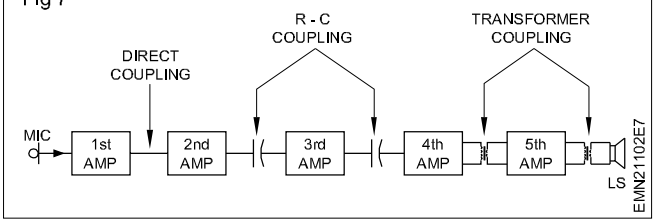
Recall lesson on transformers-impedance matching properly.

Transformer-coupled audio amplifiers were widely used once upon a time. Due to their bulkiness and high cost they are less frequently used in present day audio amplifiers. However, transformer coupling is still used extensively in radio frequency amplifiers such as radio receivers, TV receivers etc. At these higher frequencies the size and the cost of transformers will be smaller and less expensive.

Coupling using more than one method

When several amplifier stages are cascaded to obtain large gains, one or more methods of coupling may be combined as shown in Fig 7 to get the best of each method.

Fig 7



A practical 3-stage amplifier using direct coupling between the first two stages and RC coupling between the 2nd and the 3rd stage is shown in Fig 8. This amplifier can be used to amplify the weak signals coming from transduces like, microphones.

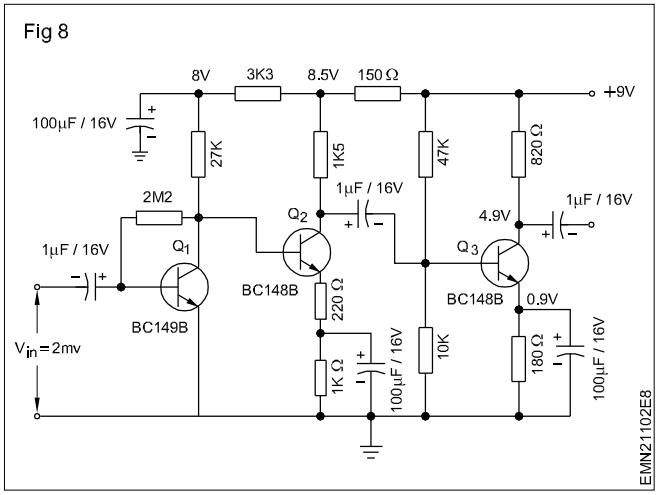
Points for discussion in the class room

1 Voltage gain of each stage and overall gain of the cascaded amplifier (assume β_{dc} of each transistor as 100).

2 Low frequency 3db cut off (f_{LC}) due to RC coupling.

3 Advantage of direct coupling in the first amplifier stage.

Fig 8



4 Advantage of self-biasing in the first amplifier stage.

5 Absence of divider-biasing for Q_2.

6 V_{CC} levels at the top end of collector resistors of Q_1, Q_2 and Q_3.

Class A Power Amplifiers

Objectives: At the end of this lesson you shall be able to

- **list the two main classifications of amplifiers**
- **list the classifications of amplifiers based on the amount of bias**
- **state the amount of biasing to be given for Class A amplifier**
- **list the disadvantages of Class A amplifiers**
- **list the applications of Class A amplifiers.**

Amplifier classification

In addition to the various classifications previous amplifiers can also classified as,

– Voltage amplifiers

– Power amplifiers.

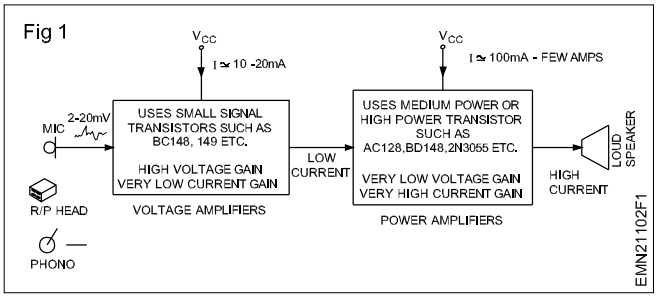
The amplifier circuits discussed in previous lessons were small signal voltage amplifiers. This means these amplifiers are intended to amplify very weak signals in the range of µ volts to millivolts. These amplifiers were concerned with increasing the weak signal voltage into a few volts. But the output of such amplifiers cannot be used to operate devices such as loudspeakers.

In order to operate loudspeakers, in addition to voltage amplifiers, amplifiers known as *Power amplifiers* are required. A power amplifier is essentially a current amplifier. A power amplifier may or may not provide any significant voltage gain. Fig 1 illustrates voltage and power amplifiers.

An easy way of identifying whether an amplifier is a voltage amplifier (small signal amplifier) or a power amplifier is by checking the type of transistors used in the amplifier. This is shown in Fig 1.

Another method of classifying amplifiers is based on the amount of DC bias given to the amplifier in its quiescent state. Based on this the amplifiers may be mainly classified as,

Fig 1



– Class A amplifiers

– Class B amplifiers

– Class C amplifiers.

Class A amplifiers

An amplifier is said to be operating as a Class A amplifier if the amplifier is active and current are flowing through the different paths of the amplifier even when no AC signal is fed to it for amplification.

The above statement means that the transistor of the amplifier is operating in the active region at all times whether or not the input ac signal is present.

To ensure that the transistor is always in active region, suitable DC biasing arrangement is necessary. Fig 2a shows a transistor amplifier with DC biasing such that it works in Class-A mode (always active) of operation.

In the CE amplifier of Fig 2, an AC voltage V_{in} drives the

base, producing an AC output voltage V_{out}.

The biasing arrangement and the DC load line of the CE amplifier at Fig 2 is below;

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{9}{820 + 180} = 9mA$$

$$V_B = \frac{R_2}{R_1 + R_2} . V_{CC} = \frac{10K\Omega}{57K\Omega} 9V = 1.58V$$

$$I_{EQ} = \frac{V_B - V_{BE}}{R_E} = \frac{1.58V - 0.7V}{180\Omega} \approx 5mA$$

$V_{CEQ} = V_{CC} – (I_{CQ}.R_C + I_{CQ}.R_E) = 9-(4.1 + 0.9) = 4$ volts.

From the above values the DC load line is drawn in Fig 2b.

Loaded voltage gain (A_{VL})

The unload gain (with R_L open) of the amplifier is given by

$$A = \frac{R_C}{r'_e}$$

When load R_L is connected, then the resistance seen by the collector of transistor (call it r_{out}) is given by,

$$r_{out} = R_C \parallel R_L$$

In Fig 2,

$$r_{out} = 820W \parallel 1500W = 530W$$

Therefore, the loaded voltage gain is given by,

$$A = \frac{r_{out}}{r'_e}$$

$$r'_e = \frac{25mV}{I_{EQ}} = \frac{25mV}{5mA} = 5\Omega$$

Therefore in Fig 2, loaded voltage gain is,

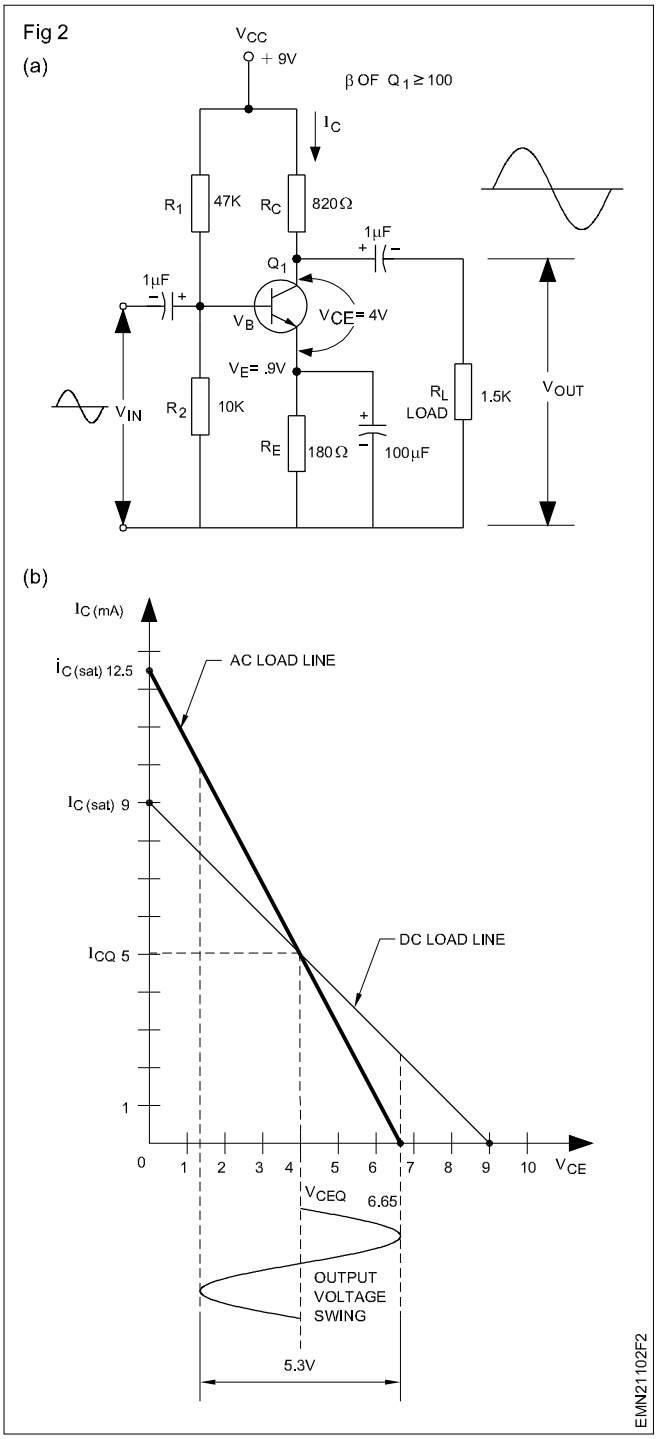
$$A_{VL} = \frac{530\Omega}{5\Omega} = 106$$

$$A_{VL} = \frac{530\Omega}{5\Omega} = 106$$

Current gain (A_i)

Current gain of the transistor A_i is,

Fig 2



$$A_i = \frac{i_c}{i_b} \approx \beta_{dc} \approx 10$$ of the transistor

In Fig 2, $A_i \approx \beta_{dc} \approx 100$

Power gain (A_p)

In Fig 2, the ac input power to the base is,

$$P_{in} = V_{in}.i_b$$

The ac output power from the collector is,

$$P_{out} = – V_{out}.i_c$$

The power gain (A_p) of the amplifier is,

$$A_p = \frac{-V_{out}.i_c}{V_{in}.i_b} = \frac{V_{out}}{V_{in}}.\frac{i_c}{i_b} = A_{VL}.Ai$$

$$A_p = A_{vL}.A_i$$

In Fig 2, $A_p = A_v.A_i$ = (106) (100) = 10,600

This means that an ac input power of 1µ watt results in an ac output power of 10,600µ watts or 10.6m watt.

Load power

n Fig 2, the *ac power* into the load resistor R_L is given by,

$$P_L = \frac{V_L^2}{R_L}$$

where,

P_L = AC load power

V_L = rms load voltage

R_L = load resistance

Since $V_{L(rms)} = 0.707\ V_p$

and $V_P = \frac{V_{pp}}{2}.V_L = 0.707V_p = \frac{0.707V_{pp}}{2}$

Therefore, V_L^2 can be written as $V_P = \frac{V^2pp}{8}$

Hence, AC power into the load P_L can be written as,

$$\frac{V_{pp}^2}{8R_L}$$

This is the maximum AC load power that a class A amplifier can produce without output distortion or clipping.

AC load line

The saturation and cut-off points of AC load line are different from those of DC line.

The *AC* saturation current $i_{c(sat)}$ is given by,

$$i_{c(sat)} = I_{CQ} + P_L = \frac{V_{CEQ}}{R_{out}}$$

For Fig 2,

$i_{c(sat)}$ = 5mA + = 12.5mA

The AC cut-off voltage V_{ce} is given by,

$V_{ce} = V_{CEQ} + I_{CQ}\ V_{out}$

For Fig 2,

V_{ce} = 4V + (5mA.530W) = 6.65 volts.

These values of $i_{c(sat)}$ and V_{ce} are plotted on Fig 2b to get the AC load line.

AC output compliance

The AC output compliance is the maximum unclipped peak-to-peak AC voltage that an amplifier can produce. This AC output compliance can be obtained by drawing DC and AC load lines.

As can be seen in Fig 2b, the AC compliance is,

AC compliance (peak-to-peak)

= $(V_{ce} - V_{CEQ})$ x 2 = (6.65-4) x 2

= 5.3 volts (peak-to-peak)

Maximum AC load power

The AC output compliance (peak-to-peak) equals the maximum unclipped voltage, therefore, maximum AC load power P_L is given by,

$$P_{L(max)} = \frac{[\text{Output compliance (peak} - \text{to} - \text{peak}]^2}{8R_L}$$

For the circuit at Fig 2.

$$P_{L(max)} = \frac{(5.3V)^2}{8(1500\Omega)} = 2340\mu3 = 2.34W$$

Transistor power dissipation

When there is no input signal, transistor is still in conduction in Class-A amplifier hence power is dissipated. This power P_Q is given by,

$P_Q = V_{CEQ}.I_Q$

For Fig 2,

P_Q = (4V) (5mA) = 20mW

The DC current drawn by the biasing resistor R_1 and R_2 is

$$I_1 = \frac{V_{CC}}{R_1 + R_2} = \frac{9V}{47K + 10K} = \frac{9}{57K} = 158\mu5 \text{ or } 0.16mA$$

The DC current through the collector in quiescent state is I_{CEQ},

In Fig 2, I_{CEQ} = 5mA

Therefore the total current drawn in quiescent state is,

$I_{TQ} = I_{CQ} + I_1$ = 5mA + 0.16mA = 5.16mA

The power input to the amplifier is quiescent state is

$P_{TQ} = I_{TQ}.V_{CC}$ = (5.16mA)(9V) = 46mW

Efficiency of class A amplifier stage

$$\eta = \frac{P_{L(max)}}{P_{TQ}} x100\%$$

where,

η = state efficiency

$P_{L(max)}$ = maximum AC load power

P_{TQ} = DC input power

For Fig 2,

$P_{L(max)}$ = 2.34mW and P_{TQ} = 46mW

Therefore, efficiency of the amplifier stage η is,

$$\eta = \frac{P_{L(max)}}{P_{TQ}} \times 100\% = \frac{2.34mW}{46mW} \times 100 = 5\%$$

From the above calculation the efficiency of the Class-A amplifier is only 5%. This low efficiency is the main disadvantage of Class-A amplifiers. With even best design it only possible to get an efficiency of less than 30% in Class-A amplifiers. But this disadvantage is compensated in Class-A by the quality of undistorted amplified output. Typical value of distortion in Class-A amplifiers is less than 5%.

Application of Class A amplifiers

Due to the advantage of minimum distortion, Class A amplifiers are used as the first amplifier stage to amplify weak signals coming out of devices like microphones, play head of tape recorders etc. If the first stage is not providing minimum distortion, the distortion gets amplified in further stages and makes the sound garbled. Hence, Class A is the most common way of making transistors work in *Linear circuits* because these circuits lead to the simplest and most stable biasing circuits.

Many Class A amplifiers use fixed-bias because of its inherent advantage that the transistors will never go to saturation and hence, distortion is minimised. Class A amplifiers with transformer coupling are sometimes used as power-amplifier stage in which case stage efficiency up to 50% can be obtained.

Class-B Amplifiers

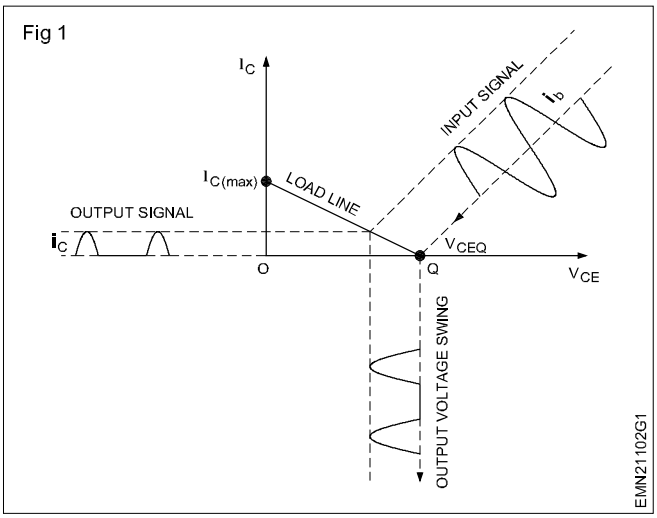
Objectives: At the end of this lesson you shall be able to

- **state the biasing of Class-B amplifiers**
- **explain the working principle of transformer coupled Class-B amplifier**
- **explain the meaning of the term push-pull**
- **list the advantages and disadvantages of Class-B push-pull amplifier**
- **explain the meaning of single ended and double ended outputs**
- **explain the working principle of a complementary symmetry Class-B amplifier**
- **explain the need of a driver stage for complementary symmetry Class-B amplifier**
- **find the impedance and gain of a driver and complementary symmetry Class-B amplifier.**

Class-B Amplifiers

In applications like, battery-powered radios, tape recorders and other portable systems, where current drain and amplifier stage efficiency are very important considerations, Class A amplifiers are not used because of its low efficiency. As an alternative to Class-A amplifiers, a number of other classes of operation of amplifiers have evolved. One of these is the Class-B operation or the Class-B amplifiers.

Fig 1



In Class B amplifiers the values of bias resistors are selected such that the quiescent collector current I_{CQ} is close to zero or zero. This means that the DC bias is at or near the cut-off value as shown in Fig 1. Because of this the output current flows only for 180° or approximately one-half of the cycle.

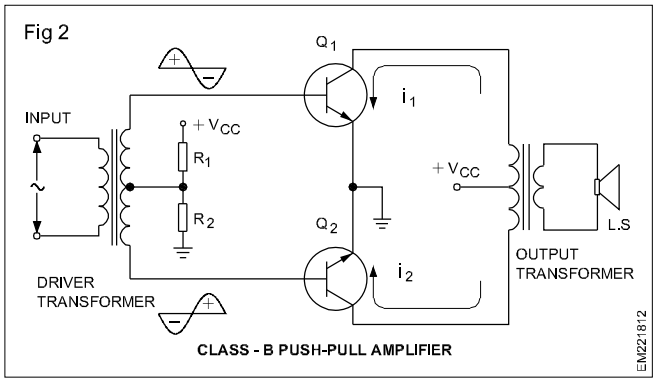
As can be seen from Fig 1 only the positive half cycles of the input signal get amplified and the output current swing up to maximum value. The negative half cycles of the input signals are cut off in the output. From Fig 3, it is evident that for Class B operation more AC signal drive signal is required compared to Class A.

In a single transistor amplifier, if Class B operation is adopted, the output will look like the output of a half-wave rectifier.

Transformer coupled Class-B push pull amplifiers

In practical audio amplifier circuits using Class B operation use two transistors instead of one for one stage of amplification as shown in Fig 2. One transistor will provide amplification for the positive half cycle of the input signal and the other for the negative half cycle of the input signal. Of such two transistor Class B amplifiers, the most common is the push-pull amplifier shown in Fig 2.

The circuit at Fig 2 is known as transformer coupled push-pull amplifier. Push-pull operation means, when the current in one transistor is increasing, the current



in the other transistor will be decreasing. However, the opposite changes will reinforce each other at the output transformer load instead of getting canceled.

The circuit at Fig 2 uses a centre tapped driver transformer to provide opposite polarity signals to the two transistor inputs. The output transformer will drive the load, generally a loudspeaker.

During the first half cycle of operation, transistor Q_1 is driven into conduction whereas transistor Q_2 is driven off. The current i_1 flows through the transformer during the first half cycle of the signal.

During the second half-cycle of the input signal, Q_2 conducts, whereas Q_1 is driven off. The current i_2 flows through the transformer during the second half-cycle of the signal. The overall output is developed across the load which will be a full sine wave which is an amplified form of the input signal.

Advantages of push-pull amplifiers

– All other signals such as noise, AC hum etc., other than the push-pull input signal get canceled at the output. This means push-pull amplifiers provide good noise rejection.

– Non-linear amplitude distortion caused by the output signal not having the same relative amplitudes as the input signal is reduced.

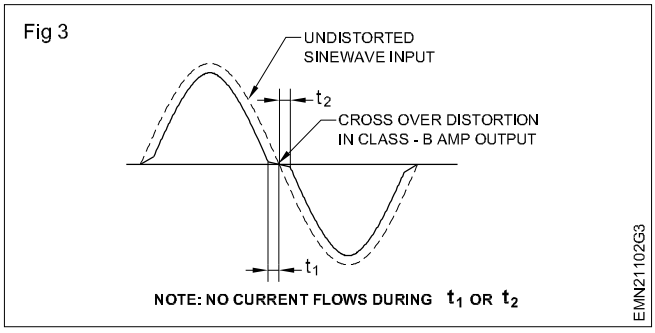
– Higher stage efficiency, typically around 50 to 80%.

Disadvantages of push-pull amplifiers

– Lack of symmetry in the amplitude of the signal applied to the two transistors results in distortion at the output known as second harmonic distortion.

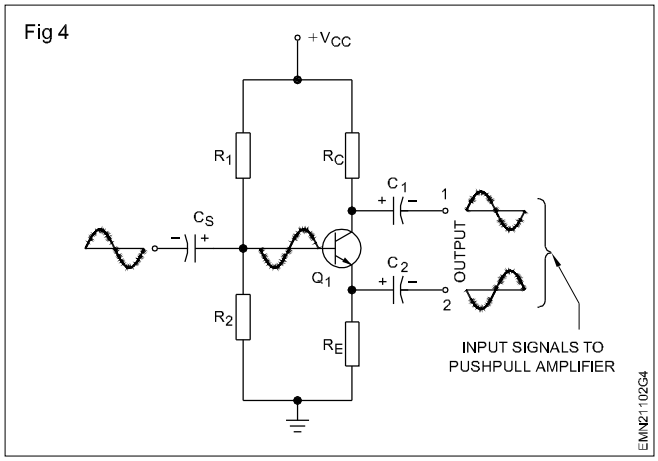
– In Class-B push-pull amplifier, when the transistors cross over to conduction, it results in distortion known as cross-over distortion. In fact, both the transistors may remain OFF for a short time before one of them turns ON. Fig 3 shows a distorted output due to cross-over distortion.

– The two transistors used in push-pull amplifiers should have perfectly matched characteristics. Otherwise, the advantage of balance and symmetry in the output currents cannot be obtained resulting in loss of efficiency and increased distortion.



In the Class-B push pull amplifier shown in Fig 2, the driver transformer was made use of in feeding phase inverted signals to the two transistors Q_1 and Q_2 from a single input signal. Another method of obtaining phase-inverted signals from a single input signal without using a transformer is shown in Fig 4.

If the gain of the amplifier in Fig 4 is made nearly 1 for each output, signals of same magnitude appears at both outputs as shown in Fig 4. These phase inverted outputs can now be fed as input signals to a push-pull amplifier.



Single ended/double ended outputs

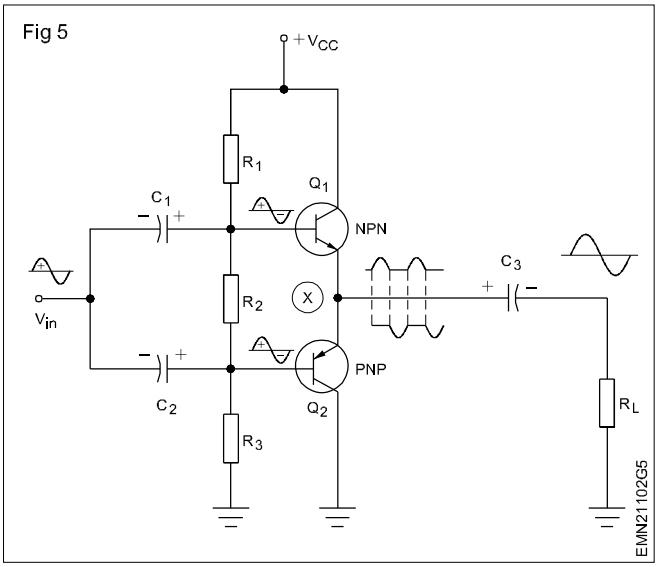
Single ended output amplifiers are those amplifiers which have only one output terminal with respect to ground. Examples of single-ended output amplifiers are the Class A amplifier discussed in earlier lessons. On the other hand as shown in Fig 2, push-pull amplifiers have two output terminals (connected to the two ends of output transformer in Fig 4) with respect to ground. Such amplifiers are known as double-ended output amplifiers.

Complementary-Symmetry Class B amplifiers

Due to the bulkiness of the driver and output transformers used in transformer coupled push pull amplifiers, other push-pull configurations have been devised. One of the most popular of these is the complementary-symmetry push-pull amplifier shown in Fig 5.

In Fig 4, one of the main functions of the output transformer is to combine the two half signals amplified by the two NPN transistors. It is possible to obtain a full cycle output across a load using complementary transistors, i.e one PNP and one NPN transistor as shown in Fig 7. Hence the need of transformer is eliminated if, two complementary transistors are used instead of two NPN transistors.

Fig 5



In the circuit at Fig 5, the audio signal is coupled to both Q_1 and Q_2. The single ended input delivers the same polarity to both NPN and PNP transistors. Resistors R_1, R_2, R_3 provide the required forward bias for the transistors. In Fig 5, as the input signal increases in +ve direction, increased base voltage makes transistor Q_1 (NPN) to conduct resulting in increased collector current and hence across load R_L. At this instant, the increased +ve base voltage for PNP transistor (Q_2) decreases the collector current below the quiescent current of this transistor. Turning the next half-cycle, as the input signal is negative going, it makes the base voltage less +ve for both the transistors.

Therefore, the collector current of $Q_{1(NPN)}$ decreases but the collector current of $Q_{2(PNP)}$ increases. The result is a push-pull amplifiers circuit with single-ended input and output.

The complementary-symmetry push pull amplifier shown in Fig 5 is a very popular audio power amplifier circuit used in most portable audio systems like radio, tape recorders. In Fig 4, the audio signal is fed to load R_L (generally a loud speaker) through a high value capacitors. More I_E in $Q_{1(NPN)}$ makes point X more positive and allows the output capacitor C_3 to charge. More I_E in $Q_{2(PNP)}$ makes point X less positive which means C_3 will discharge. Thus the opposite half cycles of the signal cause the capacitor C_3 to charge and discharge producing voltage across load $R_{L(speaker)}$.

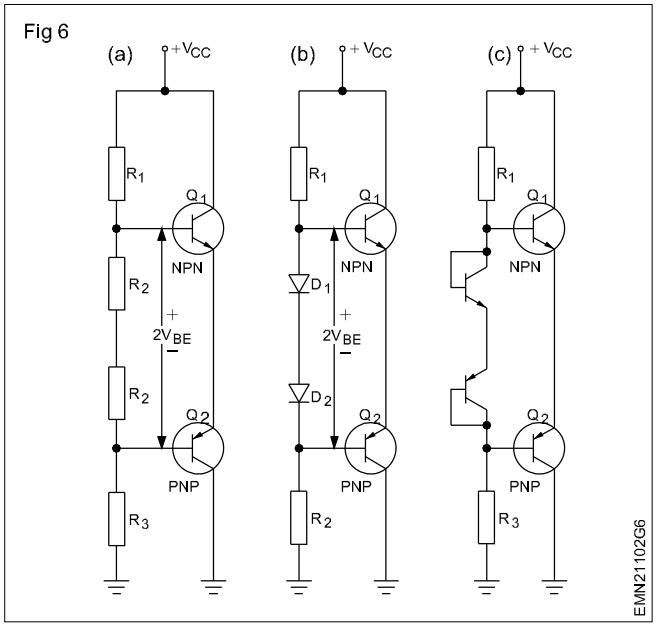
Biasing Class B amplifiers

The most crucial aspect of designing a Class B amplifier is the setting up of a stable Q point near the cut-off. Some of the biasing methods to solve this problem is illustrated in Fig 6.

In the DC biasing methods for Class-B amplifiers shown in Fig 6, the Q point is set slightly above the cut off (i.e somewhere between 0.6 to 0.7V) to avoid cross-over distortion (see Fig 3).

In Fig 6a, the value of R_2 should be so chosen that the voltage across the base of Q_1 and Q_2 is $2V_{BE}$. Data sheets of transistors indicate that an increase of 60 mV in V_{BE}

Fig 6



produces 10 times higher emitter current. Because of this it is extremely difficult to find standard resistors that can produce correct V_{BE} and also because of resistance tolerance. Hence, an adjustable resistor, such as pre-set can be used in place of R_2 to solve this problem.

To avoid the problem associated with R_2 resistor in setting correct V_{BE} and also to solve the temperature problem (recall V_{BE} decreases by 2 mV per degree rise in temperature), the best way is to use two diodes for providing $2\,V_{BE}$ biasing voltage to the emitter diodes of the transistors as shown in Fig 6b. The use of diodes also avoids the thermal run away due to temperature.

Fig 6c shows a transistor connected as diodes (base-collector shorted) instead of diodes. This method is advantageous because it is easier to match the diode curves with the V_{BE} curves, when the same transistor type is used as a diode and as a transistor.

Driver circuit for Class-B, complementary-symmetry amplifiers

In Fig 5, capacitors were used to couple the AC signal to Class B amplifier. There is a better way to drive a Class B amplifier. This is shown in Fig 7.

Fig 7

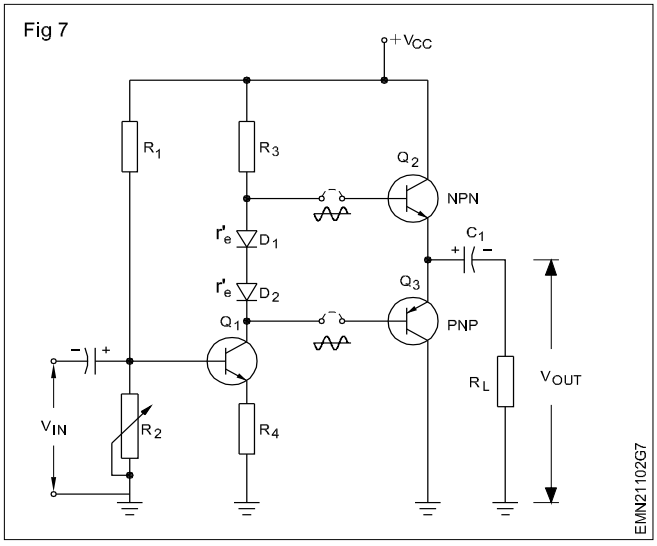


Fig 7 shows a direct coupled CE driver stage to a push-pull complementary-symmetry amplifier. Transistor Q_1 is a current source that sets up the DC biasing current through the diodes. By adjusting R_2, the DC emitter current through R_4 can be controlled.

Practical amplifier

Fig 8 is a practical amplifier circuit using two stages of voltage amplification (Q1 and Q2), a Class-B driver amplifier (Q_3) for the Class B complementary-Symmetry push-pull amplifier (Q_4 and Q_5) with single-ended output driving a loudspeaker as its load.

In Fig 8, the emitter resistor of driver stage has +0.87V across it. Therefore,

$$I_{EQ3} = \frac{0.87V}{180\Omega} = 4.8mA$$

The collector current I_{CQ3} will also approximately 4.8mA. In circuit like the one in Fig, because of the type of biasing the quiescent collector currents of transistors Q_4 and Q_5 will also be approximately equal to I_{EQ3} = 4.8mA.

The input impedance (Z_{in}) looking into the base of the conducting transistor (Q_4 or Q_5) is given by,

$$Z_{in(base)} \approx \beta_{dc}.R_L$$

Assuming a β_{dc} of 140 for Q_4 and Q_5

$$Z_{in(base)} \approx (140).(8\Omega) = 1120\Omega$$

Considering the AC equivalent circuit of Q_4 or Q_5, the input impedance $Z_{in(base)}$ (calculated above) will be in parallel with the collector resistor of driver transistor Q_2. Therefore, ac input resistance r_c is,

$$r_c = Z_{in(base)} \quad R_{CQ3}$$

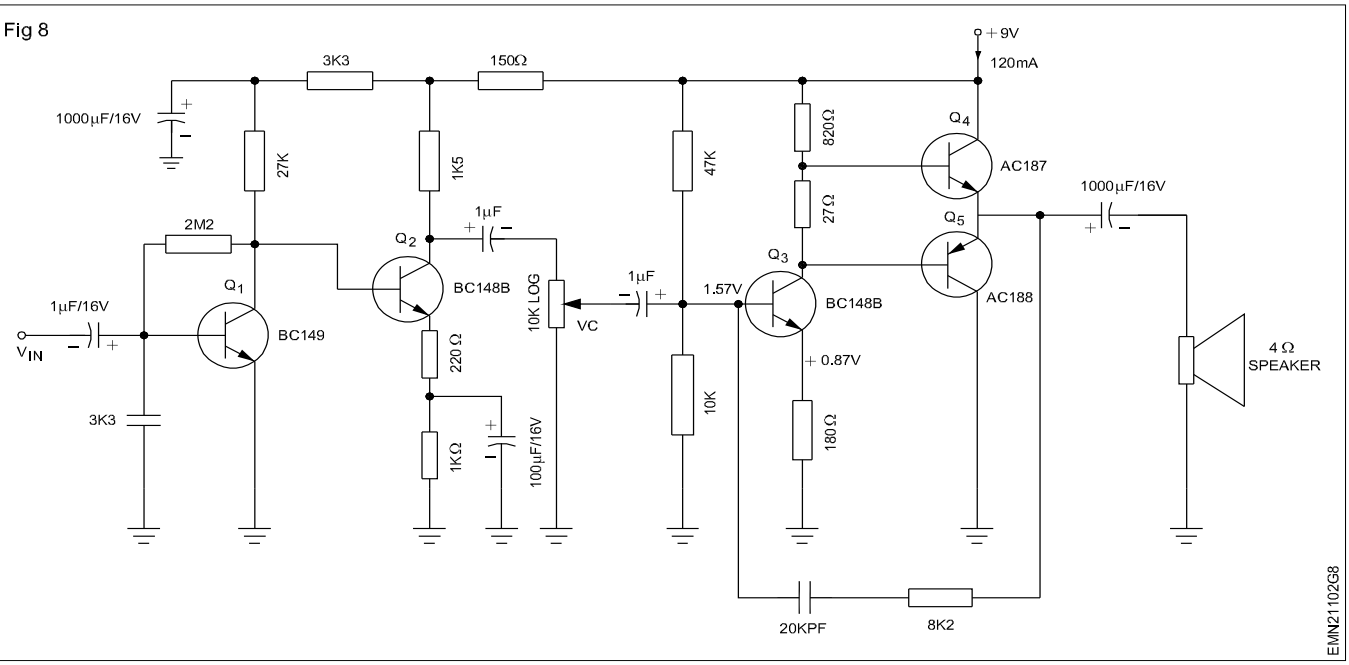
$$r_c = 1120\Omega \quad 820\Omega = 473\Omega$$

Therefore the loaded gain A_{VL} of the driver stage is,

$$A_{VL} \approx \frac{r_c}{R_E} = \frac{473\Omega}{180\Omega} = 2.6$$

The amplifier at Fig 8 can be used to amplify either a microphone signal or a play head output of a tape recorder. The input signal strength can be as low as 1 mv.

Fig 8



Characteristics	Class A	Class B	Class AB	Class C
Angle of input signal amplifier by each	360 degree	180 degree	More than 180 degree and less than 360 degree	Less than180
Efficiency	Transformer coupled is about 50%, RC coupled about 25%	Theriticaly 78.5% but practically 70 to 80%	50to 70%	Above 80%
Noise or distortion	Very less	Cross over distortion presents and noise more than class A	Remove cross over distortion and noise more than class A	More noise
Q point on load line	Centre of active	At exact point of cut	In active region but just	In cut off region

Tuned Amplifiers - Class C Amplifier

Objectives: At the end of this lesson you shall be able to

- **state the draw backs of audio amplifiers not suitable for radio frequency application**
- **define tuned amplifier**
- **explain the working of tuned amplifier**
- **state the advantages of tuned amplifier**
- **list the draw backs of tuned circuits not suitable for low frequency amplification**
- **explain about the frequency response of tuned amplifier.**

Introduction

Most of the audio amplifiers are working at radio frequencies i.e. above 50kHz. They suffer from two draw backs. They become less efficient at radio frequency and such amplifiers have mostly resistive loads and consequently the gain is independent of signal frequency over a large bandwidth. In other words, an audio amplifier amplifies a wide band of frequencies equally well and does not permit the selection of a particular desired frequency while rejecting all other frequencies.

Sometimes it is desired than an amplifier should be selective i.e. it should select a desired frequency or narrow band of frequencies for amplification. For instance, the radio receiver is required to pick up and amplify the radio frequency desired while discriminating all others. To achieve this, the simple resistive load is replaced by a parallel tuned circuit whose impedance strongly depends upon frequency. Such a tuned circuit becomes very selective and amplifies very strongly signals of resonant frequency and narrow band on either side. Such an amplifier is called a tuned amplifier.

Tuned Amplifiers

Amplifiers which amplify a specific frequency or narrow band of frequencies are called **tuned amplifiers.**

Tuned amplifiers are mostly used for the amplification of high or radio frequencies. It is because radio frequencies are generally single and the tuned circuit permits their selection and efficient amplification. However, such amplifiers are not suitable for the amplification of audio frequencies as they are mixture of frequencies as they are mixture of frequencies from 20Hz to 20kHz and not single. Tuned amplifiers are widely used in radio and television circuits where they are called upon to handle radio frequencies.

Fig. 1 shows the circuit of a simple transistor tuned amplifier. Here, instead of load resistor, we have a parallel tuned circuit in the collector. The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance at resonant frequency and very small impedance at all other frequencies. If the signal has the same frequency as the resonant frequency of LC circuit, large amplification will result due to high impedance of LC circuit at this frequency.

When signals of many frequencies are present at the input of tuned amplifier, it will select and strongly amplify the signals of resonant frequency while rejecting all others. Therefore, such amplifiers are very useful in radio receivers to select the signal from one particular broadcasting station when signals of many other frequencies are present at the receiving aerial.

Advantages of tuned amplifiers

(i) Small power loss.

(ii) High selectivity.

(iii) Smaller collector supply voltage.

Tuned circuits not suitable for low frequency amplification

(i) Low frequencies are never single. The low frequencies found in practice are the audio frequencies which are a mixture of frequencies from 20Hz to 20kHz and are not single.

(ii) High values of L and C. For low frequency amplification, we require large values of L and C.

This will make the tuned circuit bulky and expensive.

Fig 1

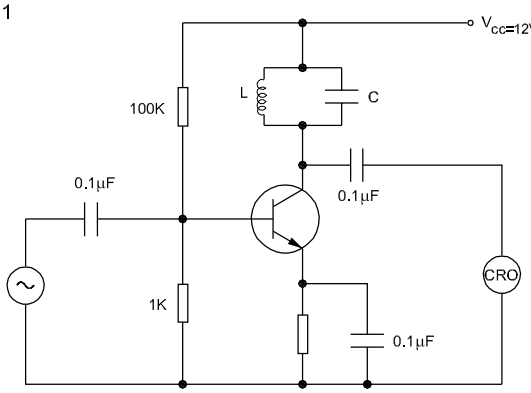
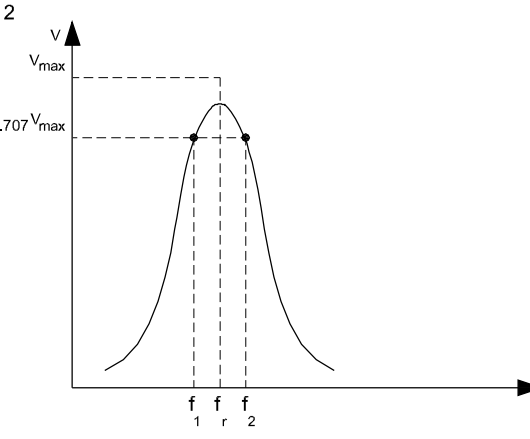


Fig.1 shows the practical implementation of tuned amplifier. The frequencies response of tuned amplifier is shown in Figure 2.

Fig 2



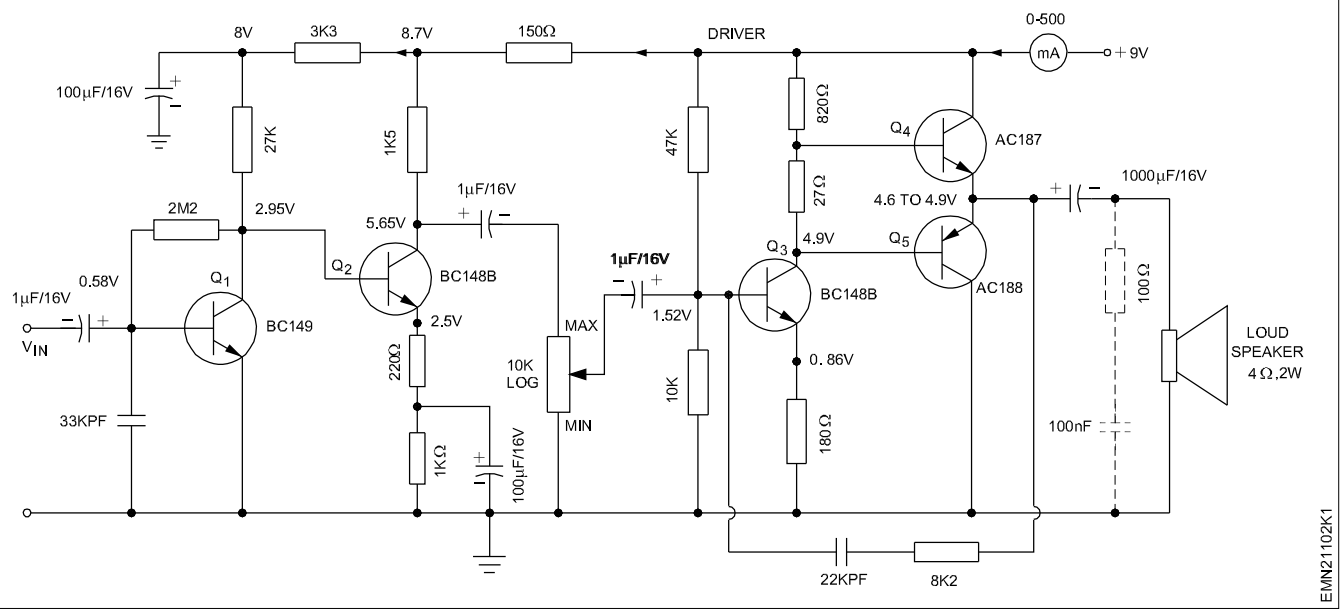
Troubleshooting of Cascaded Amplifiers

Objectives: At the end of this lesson you shall be able to

- **state the important points in troubleshooting of amplifiers**
- **state the two main types of tests carried out while troubleshooting**
- **list some of the probable faults in transistor cascaded amplifiers**
- **understand problem tree structures and identify cause(s) of defect(s).**

Fig 1 shows the schematic circuit of a 5 transistor amplifier. Fig 2 is the block diagram representating the audio amplifier shown in Fig 1. This amplifier consists of a pre-amplifier, pre-driver, driver and a complementary-symmetry output amplifier. Signal test points are numbered 1 through 10.

Fig 1



The following tips are very useful while troubleshooting cascaded audio amplifier;

– Begin the troubleshooting assuming that there is a single defect. When the first defect is found and rectified, other defects may be found. Tackle these defects in the same manner as done for the first defect.

– Follow a logical procedure instead of a trial and error method.

– Study the circuit or atleast its blocks and have a feel of the circuit's functioning.

– Observe the symptom, and from the symptom determine in which block the defect can be found.

– Trace the signal path using short cut techniques and find the block or the stage which has the defective component.

– Carry out voltage level tests of the stages and isolate the defective component.

– Analyze the cause for the defect. If the cause is independent, replace the defective component and test the circuit. If the cause is dependent, check the possible dependent causes before replacing the defective component.

To troubleshoot an amplifier circuit, there are two main types of tests to be carried out namely;

(1) **Dynamic test**: In this method a signal source is connected to the input of the amplifier and a CRO is used to test the progress of the signal along the circuit path.

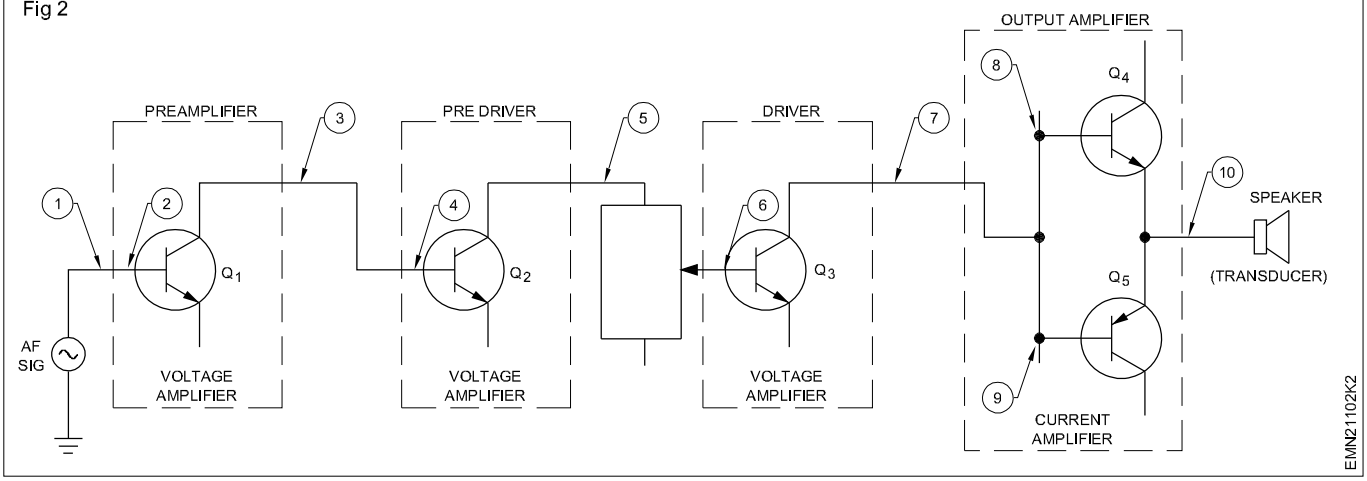
(2) **Static test**: This involves measuring the voltage levels and resistances at different points of a stage. This test is generally carried out once the particular stage in the circuit is identified as the problem zone.

A general procedure for troubleshooting cascaded amplifiers is given below;

– First check all the components external to the circuit board such as, the mains fuse, speaker, volume control etc., It is suggested to check these components starting from the output side to the input side. For instance, in Fig 1, check the speaker first before checking the volume control.

– Connect any signal source such as A.F signal generator signal injector, etc., to the input. Using a signal tracer or a CRO, trace the progress of the signal. The first test should be made at TP_5 i.e., the middle of the circuit. This is because signal is present here, it means that the first half of the amplifier is OK. This also means, the problem is either in Q_3 or Q_4, Q_5 stages. If there is no signal at TP_5, test at TP_4 and in this manner trace toward the input of the system. This divide-and-conquer method locates the defective stage much faster

Fig 2



than, following the signal from TP_1 to TP_2 to TP_3 and so on.

– Feed or inject the signal at the input of those stages(input of Q_3 in example above) and test the output of further stages. In this manner narrow down the source of the problem to one or two stages.

– Carry out static tests and identify the defective component of the faulty stage.

– Analyze whether the replacement of the component would lead to another or the same defect again. For instance, the cause for a blown-off fuse may be a short in the circuit. Hence, without locating and removing the short, if a new fuse is placed, it will blow off again. On the other hand, If your analysis of the defect says that it is an independent defect, for instance, worn out volume control pot replace the defective component and continue the test.

Dynamic troubleshooting (signal injection and signal tracing) requires a signal source with an adjustable output amplitude. Also for tracing the signal, shape and level a schematic diagram is a necessity. The circuit schematic will enable you to see atleast, the relationship of individual stages to the whole system and give a clue of signal levels. Input signal level must be known in order to adjust the source generator, so that, the injected signal is neither not too weak nor too strong. If too strong a signal is used, the amplifiers will operate in cut off or saturation and distortion will result. If too low signal is used, it might seem that a gain defect exist although it may actually not.

Each amplifier circuit you get for troubleshooting may be different. The technician must understand the procedure given above and learn to apply it to different systems and to make judgments based on the tests made. A schematic diagram should be on the bench beside the technician while troubleshooting schematic gives signal shapes and levels at each stage of the circuit, compare the measured value with the signal levels indicated before taking any decision.

Probable complaints in amplifiers

Some of the common complaints associated with defective amplifiers along with some of its causes are given below in the form of problem trees;

The causes shown are only a few amongst many for the wired cascaded amplifier

Fig 3

Complaint : DEAD AMPLIFIER
Symptom : Not even click sound when switched on
Pre Condition(s) : Not even click sound when switched on

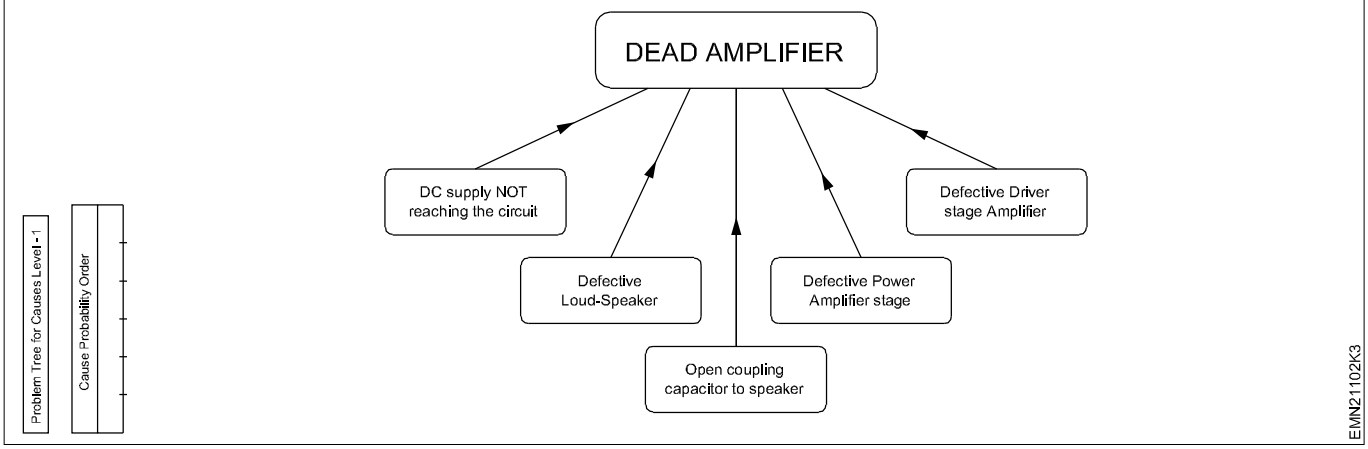
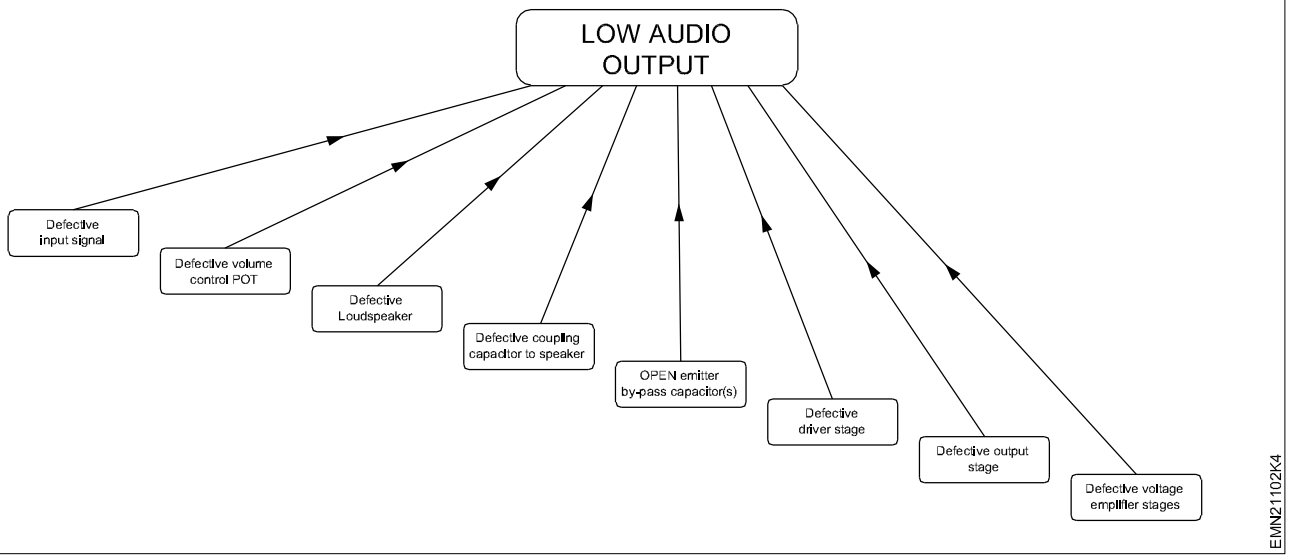


Fig 4

Complaint : LOW AUDIO OUTPUT
Symptom : Output sound exist but volume very low
Pre Condition(s) : DC Supply level normal, volume control in max-vol position



Troubleshooting of Simple CE Amplifier

Objectives: At the end of this lesson you shall be able to

- **list the possible defects in the components used in transistor CE amplifier**
- **state the steps involved in troubleshooting**
- **state the method of in-circuit testing of transistors**
- **state the method of in-circuit testing of resistors.**

Introduction

The following points were discussed in pervious lessons.

– activities involved in troubleshooting a circuit or a system or an equipment

– general steps involved in troubleshooting

– methods of trouble shooting.

For troubleshooting an amplifier, the approach and the steps are the same as in troubleshooting any other electronic circuit. That is,

[1] **Physical and sense tests**

[2] **Symptom diagnosis**

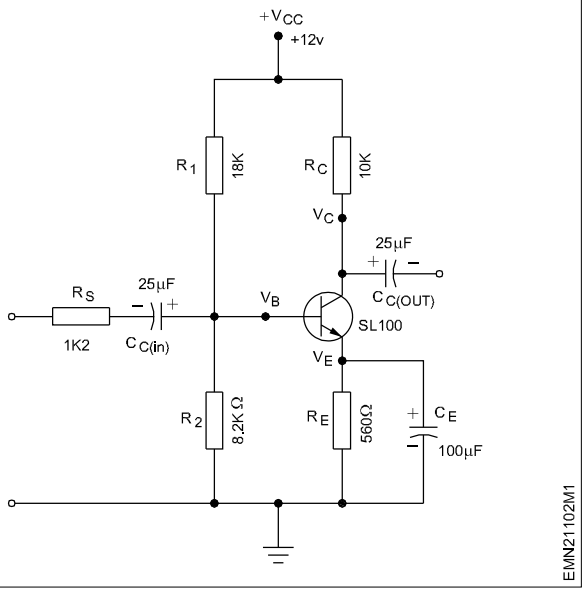
[3] **Testing for defective components in the probable order of their failure and replacing the defective components.**

After carrying out the physical tests in power off condition and sense tests in power-on condition, the nature of complaint(defect) it checked as a confirmation.

Once you have checked and confirmed that the given single transistor CE amplifier is not working, before going into troubleshooting, it is necessary to know the nature of fault that can occur in each type of component. Referring to the circuit diagram of the amplifier given in Fig 1, the probable faults with the components are given below:

In the order of highest to lowest probability, the probable faults in the amplifier circuit at Fig 1 are,

Fig 1



1 Open or Short or Leaky electrolytic capacitors

Electrolytic capacitors are the most troublesome components and these components fail most frequently.

2 Defective transistor (open/short junctions)

Transistors are very sensitive to voltage,current and temperature and, therefore, any error in the applied voltage level or polarity or wrong limiting resistor values may make the transistor faulty.

3 Open resistors

It is most unlikely that resistors may become faulty; however they do become faulty either because of their leads becoming loose with the resistor body or the resistors may burn out due to excess current through them. All these happens, if, the design of the amplifier is bad or low rating resistors are used.

With the above order of component failure probability, it is necessary to check these components in the same order.

Once all the electrolytic capacitors are checked by opening one of its ends and capacitor-action is tested using ohmmeter, the next component to be checked is the active device. The only active device in the given circuit is the transistor.

For testing the working condition of the transistor wired in a circuit, instead of removing the transistor out of the circuit and testing it, as a short cut method it is possible to check the voltage levels at various points of the transistor as shown in Fig 2.

If the amplifier was in good working condition, then, the transistor would be conducting. If the transistor is conducting, then there will be different voltage levels at the base, emitter and collector as shown in Fig 2.

For example, if the voltage at the collector is equal to V_{cc}, you can immediately say that, the transistor is not conducting.

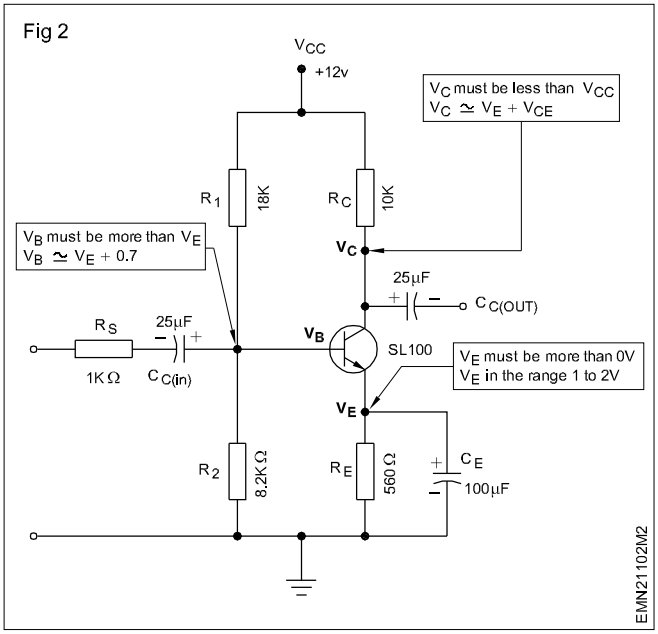
[H.I: Instructors may discuss the reasons with the trainees]

Similarly, if the voltage at the emitter is equal to zero, you can immediately say that the transistor is not conducting.

[H.I: Instructors may discuss the reasons with the trainees]

In addition to the above method of finding the condition of

Fig 2



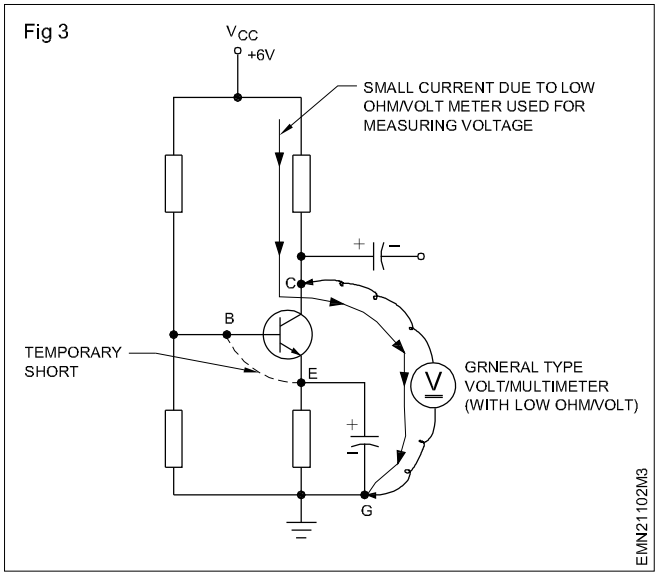
a transistor in a circuit, there is one more way by which you can find out whether or not the transistor is turning ON and OFF. To do this, temporarily short the base and emitter of the transistor as shown by dotted lines in Fig 3a, using a tweezer. This short, bypasses the base-emitter junction of the transistor. Hence the base-emitter is no more forward biased. This makes the collector voltage at the transistor to rise to V_{cc}. In this shorted condition, when the voltage at the collector is measured, if the voltage is equal to V_{cc}, you can say that the transistor is switching OFF as expected.

Once the temporary short between the base and the emitter is removed and the collector voltage measured, if the collector voltage becomes less than V_{cc}, it indicates that the transistor has again turned ON. So, by doing this test, you can confirm the switching ON/OFF of the transistor, and hence, conclude the condition of the transistor as good.

When the base-emitter shifting test is done as shown in Fig 1, to measure the voltage at the collector, preferably use a VTVM or a digital volt meter. This is because, in general type low cost voltmeters, a small current flows though the meter while measuring the voltage. Hence, current flows through the collector resistor as shown in Fig.3 causing a drop across it. Because of this voltage drop across the collector resistor, the collector voltage shown by the meter will be slightly less than V_{cc} even though the transistor is really OFF.

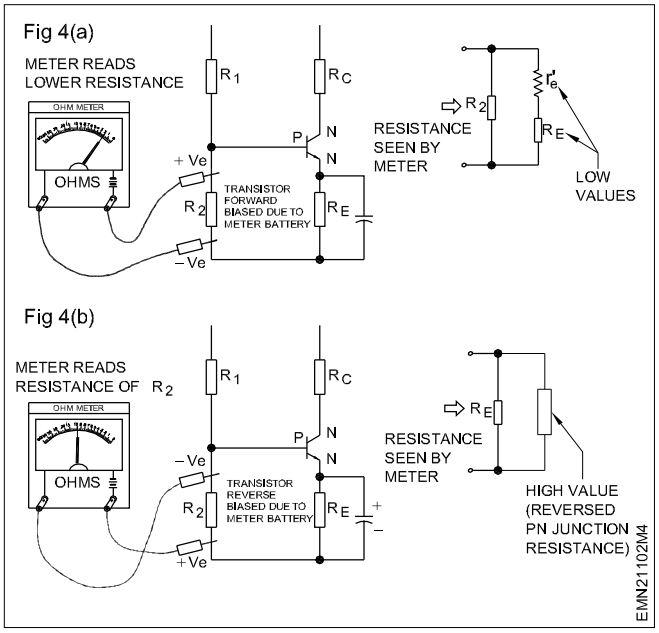
For testing the condition of resistors, either open one end of the resistor and check its resistance. Alternatively, you can measure the resistance across the resistor without opening the leads. But when resistance is measured without opening atleast one lead of the resistor, due to the other circuit components coming in parallel with it, the meter reading may be difficult to interpret. This problem can be solved to an extent if the polarity of the meter probes are such that the transistor junction is reverse

Fig 3



biased, and hence, the resistors on the other side of the transistor does not come in parallel with the resistor being checked. Figs 4a and 4b illustrates the effect of meter polarity while measuring resistance.

Checking resistances using ohmmeter should be done with DC supply to the circuit switched OFF.



After finding the defective components and replacing them with good working components, to declare the circuit as *working*, the following checks are necessary.

– Repeat checking the DC levels at base,emitter and collector of the transistor to confirm working of the transistor.

– Carry out the signal injection test, also known as dynamic test. In this test, inject a sinusoidal signal of 1 kHz of suitable level and observe the waveform at the output using a CRO. If the output waveform is undistorted and the amplifier has the required gain, then the amplifier can be confirmed as working normally.

The dynamic test on the amplifier may also be conducted as a first step of troubleshooting to confirm the complaint with the amplifier.

Once the circuit is serviced and found to be in working order, it is a good servicing habit to physically recheck for dry solders and solder sprays to ensure that the circuit will not come back for servicing too early again.

Series and Parallel Resonance

Objectives: At the end of this lesson you shall be able to

- **state the meaning of resonance in LC circuits**
- **list the characteristics of series LC circuits at resonance**
- **calculate the resonance frequency and impedance of series LC circuits**
- **define the terms selectivity and bandwidth of a LC circuit**
- **calculate the quality factor, a LC circuit**
- **explain the relationship between the Q factor and bandwidth**
- **list a few applications of series resonance circuits.**

SERIES RESONANCE CIRCUIT

Impedance of series resonance circuit

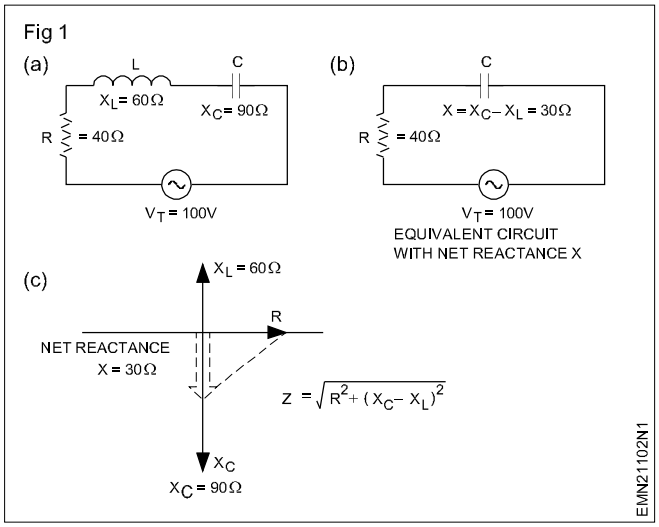
A simple series LC circuit shown in Fig 1. In this series LC circuit,

– resistance R is the total resistance of the series circuit(internal resistance) in ohms,
– X_L is the inductive reactance in ohms, and
– X_C is the total capacitive reactance in ohms.

In the circuit at Fig1, since the capacitive reactance(90W) is larger than inductive reactance(60W), the net reactance of the circuit will be capacitive. This is shown in Fig 1b.

If the capacitive reactance was smaller than inductive reactance the net reactance of the circuit would have been inductive.

All though the unit of measure of reactance and resistance is the same(ohms), the impedance, Z of the circuit is not given by the simple addition of R, X_L and X_C. This is because, X_L is +90° out of phase with R and X_C is -90° out of phase with R.



Hence the impedance Z of the circuit is the phasor addition of the resistive and reactive components as shown by dotted lines in Fig 1c. Therefore, Impedance Z of the circuit is given by,

$$Z = \sqrt{R^2 + (X_C - X_L)^2}$$

If X_L were greater than X_C, then the absolute value of impedance Z is will be,

$$Z = \sqrt{R^2 + (X_L - X_C)^2}$$

For the circuit in Fig 3(a), total impedance Z is,

$$Z = \sqrt{R^2 + (X_C - X_L)^2}$$

$$Z = \sqrt{40^2 + 30^2}$$

Z = 50W, Capacitive *(because $X_C > X_L$)*

Current I through the circuit is given by,

$$Z = \sqrt{R^2 + (X_C - X_L)^2}$$

$$I = \frac{V}{Z} = \frac{100}{50\,\Omega} = 2 \text{ Amps}$$

Therefore, the voltage drop across the components will be,

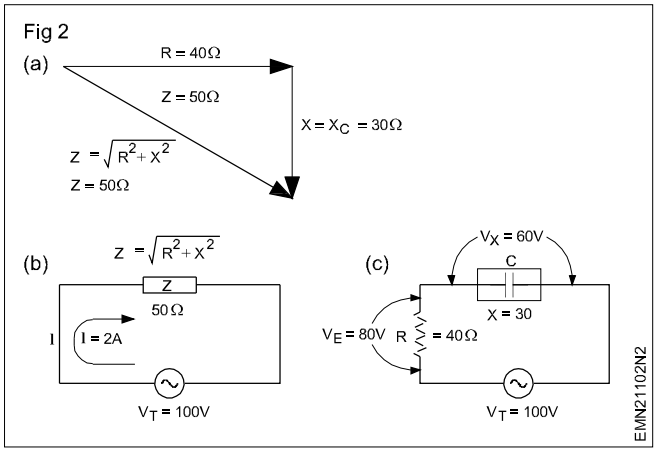
V_R = voltage drop across R = I.R = 2x40 = 80 volts
V_L = voltage drop across L = I.X_L = 2x60 = 120 volts
V_C = voltage drop across C = I.X_C = 2x90 = 180 volts.

Since V_L and V_C are of opposite polarity, the net reactive voltage V_X is = 180 - 120 = 60V as shown in Fig 2.

Note that the applied voltage is not equal to the sum of voltage drops across reactive component X and resistive component. This is again because the voltage drops are not in phase. But the phasor sum of V_R and V_X will be equal to the applied voltage as given below,

$$V_T = \sqrt{V_R^2 + (V_L - V_C)^2}$$

Fig 2



$$V_T = \sqrt{80^2 + 60^2} = 100 \text{ volts(applied voltage).}$$

Phase angle θ of the circuit is given by,

$$\theta = \tan^{-1}\frac{X_C - X_L}{R}$$

Condition at which current through the RLC Series circuit is maximum

From the formula,

$Z = \sqrt{R^2 + (X_C - X_L)^2}$ it is clear that the total impedance Z of the circuit will become purely resistive when, reactance $X_L = X_C$

In this condition, the impedance Z of the circuit will not only be purely resistive but also minimum.

Since the reactance of L and C are frequency dependent, at some particular frequency say f_r, the inductive reactance X_L becomes equal to the capacitive reactance X_C.

In such a case, since the impedance of the circuit will be purely resistive and minimum, current through the circuit will be maximum and will be equal to the applied voltage divided by the resistance R.

Series resonance

From the above discussions it is found that in a series RLC circuit,

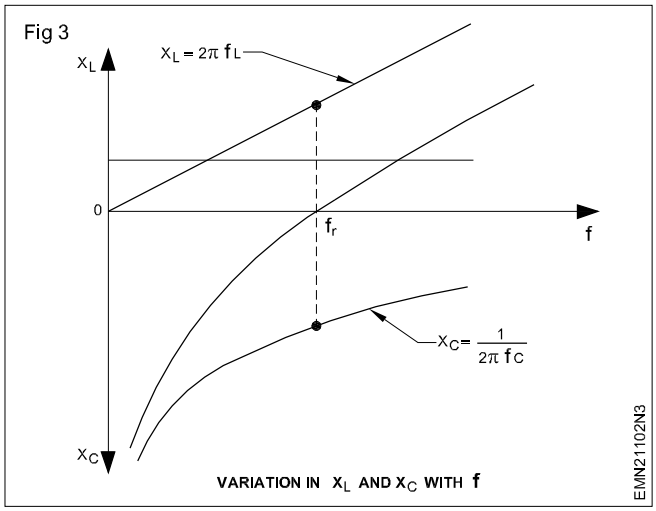
Impedance $Z = \sqrt{R^2 + (X_C - X_L)^2}$

Current $I = \frac{V}{Z}$, and

Phase angle $\theta = \tan^{-1}\frac{X_C - X_L}{R}$

If the frequency of the signal fed to such a series LC circuit(Fig 3) is increased from 0 Hz, as the frequency is increased, the inductive reactance(X_L = 2pfL) increases linearly and the capacitive reactance (X_C = 1/2pfL) decreases exponentially as shown in Fig 3.

Fig 3



As shown in Fig 3, at a particular frequency called the **resonance frequency, f_r**, the sum of X_L and X_C becomes zero($X_L - X_C = 0$).

From Fig 5 above, at resonant frequency f_r,

– Net reactance, X = 0 (i.e, $X_L = X_C$)
– Impedance of the circuit is minimum, purely resistive

and is equal to R

– Current I through the circuit is maximum and equal to V/R
– Circuit current, I is in-phase with the applied voltage V (i.e. Phase angle θ= 0).

At this particular frequency f_r called resonance frequency, the series RLC is said to in a condition of **series resonance**.

Resonance occurs at that frequency when,

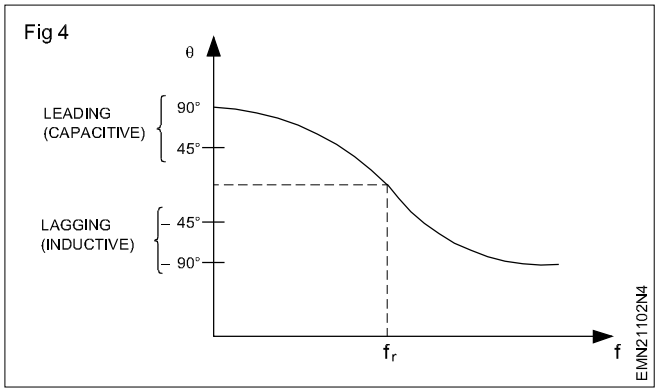
$X_L = X_C$ or 2pfL = 1/2pfC

Therefore, **Resonance frequency, f_r** is given by,

$$f_r = \frac{1}{2\pi\sqrt{LC}} \text{ Hz} \qquad \text{.... (1)}$$

Reactance of series RLC above and below resonance frequency f_r

Fig 4 shows the variation of net reactance of a RLC circuit with the variation in frequency.



From Fig 4 above,it can be seen that the,

– net reactance is zero at resonant frequency f_r
– net reactance is capacitive below the resonant frequency f_r
– net reactance is inductive above the resonant frequency f_r

Selectivity or Q factor of a series RLC circuit

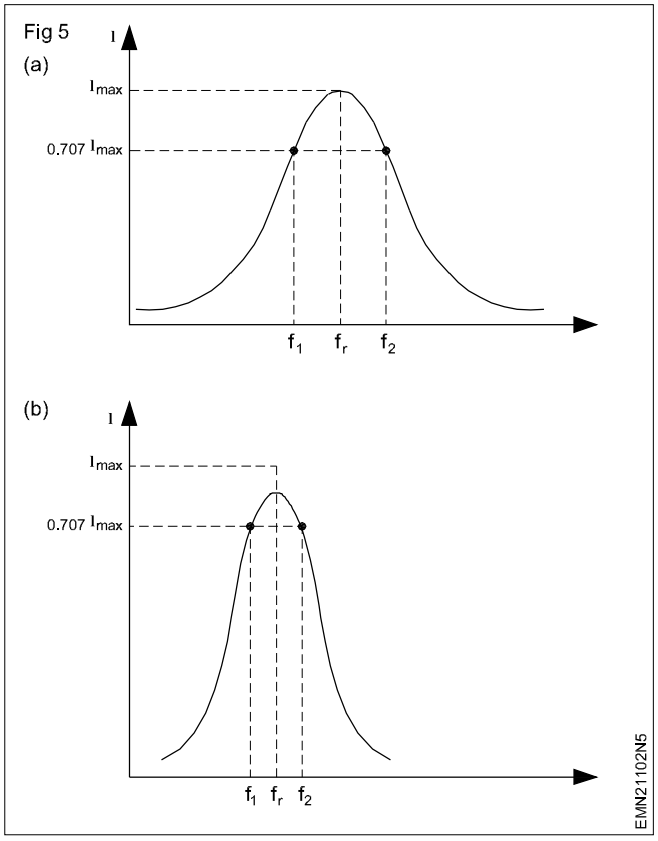
Figs 5a and 5b two graphs showing the current through series two different RLC circuits for frequencies above and below f_r. f_1 and f_2 are frequencies at which the circuit current is 0.707 times the maximum current, I_{max} or the -3dB points.

Fig 5 indicates that series RLC circuits select a band of frequencies around the resonant frequency, f_r. This band(f_1 to f_2 is called the **band width** f of the series RLC circuit.

Bandwidth = $\Delta f = f_2 - f_1$ Hz.

where, f_2 is called the upper cut off frequency and f_1 is called the lower cut off frequency of the resonant circuit.

Comparing Figs 5a and 5b, it is seen that the bandwidth of 5b is smaller than that of 5a. This is referred to as the **selectivity** or **quality factor, Q** of the resonance circuit.



The RLC circuit having the response shown in Fig 5b is more selective than that of Fig 5a. The quality factor, Q of a resonance circuit is given by,

$$\text{Quality factor} = Q = \frac{f_r}{\Delta_f} = \frac{f_r}{f_2 - f_1} \qquad \text{...[2]}$$

If Q is very large, the bandwidth f will be very narrow and vice-versa. The Q factor of the series resonance circuit depends largely upon the Q factor of the coil(inductance) used in the RLC circuit.
Therefore,

$$Q \text{ of coil} = \frac{X_L}{R} = \frac{2\pi f_r L}{R}$$

since,

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Q of the series RLC circuit is given by,

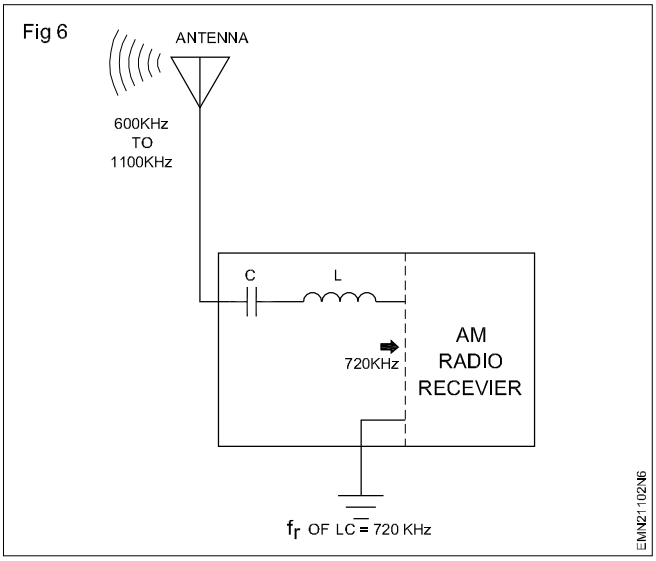
$$Q = \frac{1}{R} \cdot \frac{\sqrt{L}}{\sqrt{C}} \qquad \text{...[3]}$$

Application of series resonance circuits

A series resonance circuit can be used in any application where it is required to select a desired frequency. One such application is shown in Fig 6.

In Fig 6, the radio receiver antenna intercepts all the frequencies available in air. The series LC circuit when tuned to 720KHz(f_r) will allow only the signal corresponding to Chennai-A radio station and rejects all other signal frequencies.

Fig 6



A series resonance circuit can also be used to reject an undesired frequency(used as wave trap)

A wave trap is a resonant LC circuit tuned to the frequency to be rejected. Thus the output of the tuned amplifier will not have the frequency for which the trap is tuned. This is because, at resonance the series LC of the wave trap, provides very low impedance. As the trap is connected across the collector and ground, the rejection frequency component is grounded.

Such wave traps are extensively used in very high and ultra-high frequency circuits such as television receivers, communication receivers etc.

Parallel Resonance Circuits

Objectives: At the end of this lesson you shall be able to

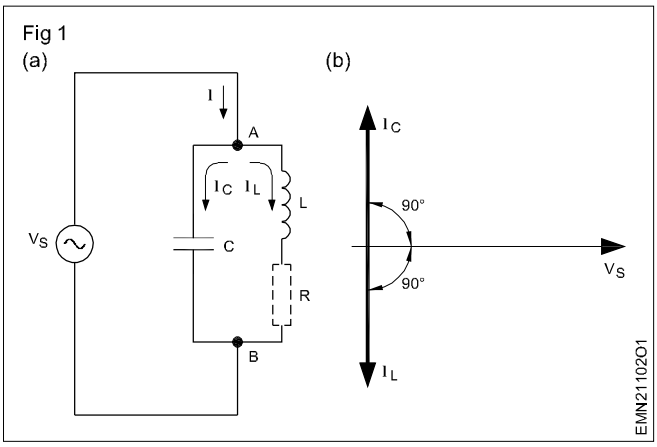
- **list the characteristics of LC parallel circuits at resonance**
- **explain the term Band-width in parallel LC circuits**
- **explain the storage action in parallel LC circuits**
- **explain the terms make up current and tank circuit**
- **list a few applications of parallel LC circuits**
- **compare the properties of series and parallel LC circuits at resonance, above resonance and below resonance.**

PARALLEL RESONANCE

The circuit at Fig 1, having an inductor and a capacitor connected in parallel is called parallel LC circuit or parallel resonance circuit. The resistor R, shown in dotted lines indicate the internal DC resistance of the coil L. The value of R will be so small compared to the inductive reactance, that it can be neglected.

From Fig 1a, it can be seen that the voltage across L and C is same and is equal to the input voltage V_S.

Fig 1



By Kirchhoff's law, at junction A,

$$I = I_L + I_C.$$

The current through the inductance I_L (neglecting resistance R), lags V_S by 90°. The current through the capacitor I_C, leads the voltage V_S by 90°. Thus, as can be seen from the phasor diagram at Fig 1b, the two currents are out of phase with each other. Depending on their magnitudes, they cancel each other either completely or partially.

If $X_C < X_L$, then $I_C > I_L$, and the circuit acts capacitively.

If $X_L < X_C$, then $I_L > I_C$, and the circuit acts inductively.

If $X_L = X_C$, then $I_L = I_C$, and hence, the circuit acts as a purely resistive.

Zero current in the circuit means that the impedance of the parallel LC is infinite. This condition at which, for a particular frequency, f_r, the value of $X_C = X_L$, the parallel LC circuit is said to be in parallel resonance.

Summarizing, for a parallel resonant circuit, at resonance,

$$X_L = X_C,$$

$$Z_p = ¥$$

$$I_L = I_C$$

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$I = \frac{v}{Z_p} \approx 0$$

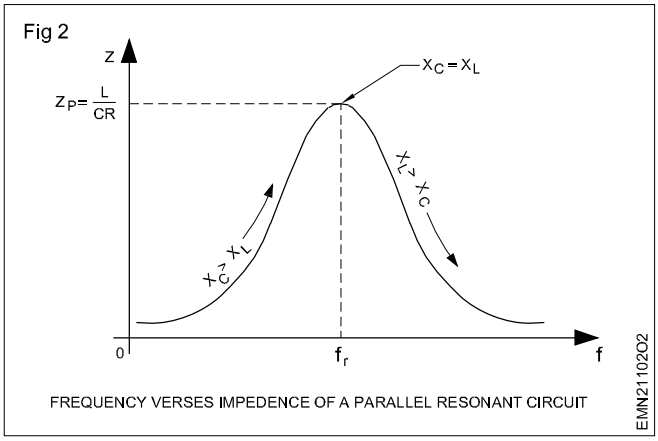
In a parallel resonance circuit, with a pure L(no resistance) and a pure C(loss-less), at resonance the impedance will be infinite. In practical circuits, however small, the inductor will have some resistance. Because of this, at resonance, the phasor sum of the branch currents will not be zero but will have a small value I. This small current I will be in phase with the applied voltage and the impedance of the circuit will be very high although not infinite.

Summarizing, the three main characteristics of parallel resonance circuit at resonance are,

– phase difference between the circuit current and the applied voltage is zero

– maximum impedance

– minimum line current.



FREQUENCY VERSES IMPEDENCE OF A PARALLEL RESONANT CIRCUIT

The variation of impedance of a parallel resonance circuit with frequency is shown in Fig 2.

In Fig 2, when the input signal frequency to the parallel resonance circuit is moved away from resonant frequency f_r, the impedance of the circuit decreases. At resonance the impedance Z_p is given by,

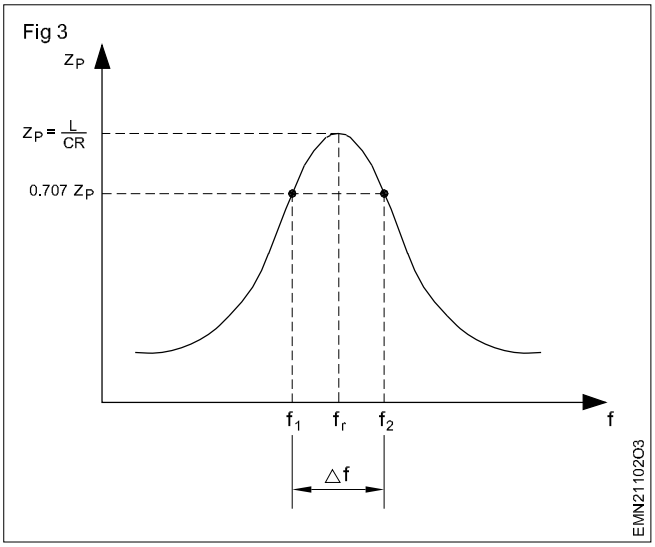
$$Z_p = \frac{L}{CR}$$

At resonance, although the circuit current is minimum, the magnitudes of I_L & I_C will be much greater than the line current. Hence, a parallel resonance circuit is also called current magnification circuit.

Bandwidth of parallel resonant circuits

As discussed in series resonance, all resonant circuits have the property of discriminating between the frequency at resonance(f_r), and those not at resonance. This discriminating property of the resonant circuit is expressed in terms of its **bandwidth(BW).** In the case of series resonant circuits the response of the circuit at resonance frequency(f_r) is in terms of the line current(which is maximum), and in a parallel resonant circuit, it is in terms of the impedance(which is maximum).

The bandwidth of a parallel resonant circuit is also defined by the two points on either side of the resonant frequency at which the value of impedance Z_p drops to 0.707 or



$\frac{1}{\sqrt{2}}$ of its maximum value at resonance, as shown Fig 3.

From Fig 3, the bandwidth of the parallel resonance circuit is,

Bandwidth, BW = $\Delta f = f_2 - f_1$

As can be seen in Fig 3, the value of Z_p is dependent on the resistance R of the coil (Z_p = L/CR). If R is less Z_p will be larger and vice versa. Since the bandwidth depends on Z_p and Z_p depends on R, we can say that the bandwidth of a resonant circuit depends upon the resistance associated with the coil. The resistance of the coil in turn decides the Q of the circuit. Thus, the Q of the coil decides the band width of the resonant circuit and is expressed as,

$$\text{Bandwidth(BW)} = (f_2 - f_1) = \frac{f_r}{Q}$$

Storage action of parallel resonance circuit

At parallel resonance, though the circuit current is minimum(ideally zero), I_L and I_C will still be there. This I_L and I_C will be a circulating current in the closed loop formed by L and C. This circulating current will be very high at resonance. This circulating current flip-flops between the capacitor and inductor, alternately charging and discharging each. When a capacitor or an inductor is charged, it stores energy. When it is discharged it gives up the energy stored in it. The current inside the LC circuit switches the stored energy back and forth between L and C. If the inductor had no resistance and if the capacitor was loss-free, then, no more external energy would be required to retain this flip-flop or oscillation of charging and discharging. But, in a practical circuit, since ideal L and C cannot be obtained, some amount of the circulating energy is lost due to the resistance of the coil and the loss due to capacitor. This lost energy is the only energy the power supply source(V_S) must supply in the form of circuit current,I. This current, therefore, is called as **make-up current.** It is this storage action of the parallel-resonant circuit which gives rise to the term **tank circuit**, often used with parallel resonant circuits. Hence, parallel resonant circuits are also called tank circuits.

Application of parallel resonant circuits

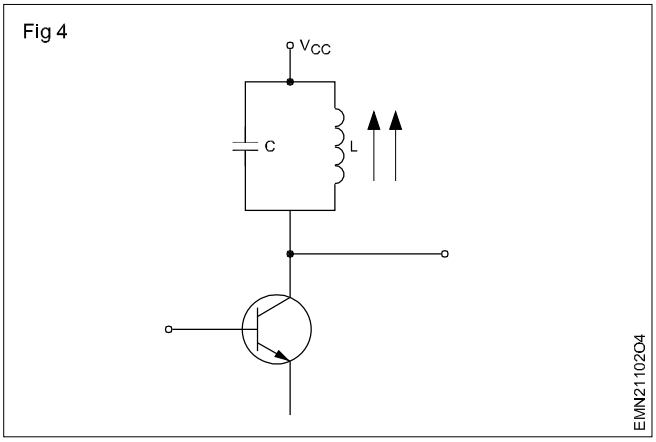
Parallel resonance circuits or tank circuits are commonly used in almost all high frequency circuits. Tank circuits are used as collector load in class-C amplifiers instead of a resistor load as shown in Fig 4.

Details of class-C amplifiers are discussed in further lessons.

Tank circuits are used in circuits known as oscillators which are designed to generate ac signals using dc supply.

Oscillators are discussed in detail in further lessons.

Fig 4



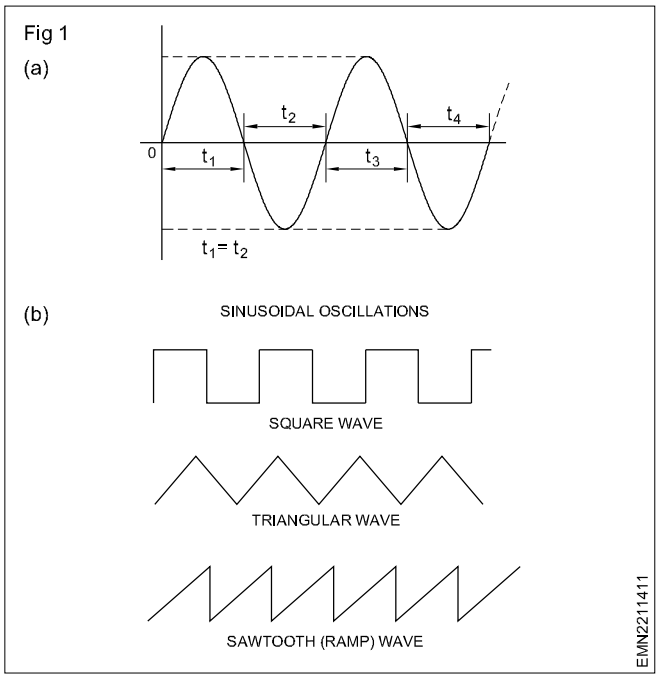
Property	Series circuit	Parallel circuit
	At resonant frequency	
Resonant frequency, f_r	$\frac{1}{2\pi\sqrt{LC}}$	$\frac{1}{2\pi\sqrt{LC}}$
Reactance	$X_L = X_C$	$X_L = X_C$
Impedance	Minimum ($Z_r = R$)	Maximum ($Z_r = L/CR$)
Current	Maximum	Minimum
Quality factor	$\frac{X_L}{R}$	$\frac{X_L}{R}$
Bandwidth	$\frac{f_r}{Q}$	$\frac{f_r}{Q}$
	Above resonant frequency	
Reactance	$X_L > X_C$	$X_C > X_L$
Impedance	Increases	Decreases
Phase difference	The current lags behind the applied voltage.	The current leads the applied voltage.
Type of reactance	Inductive	Capacitive
	Below resonant frequency	
Reactance	$X_C > X_L$	$X_L > X_C$
Impedance	Increases	Decreases
Phase difference	The current leads the applied voltage.	The current lags behind the applied voltage.
Type of reactance	Capacitive	Inductive

Oscillators

Objectives: At the the end of this lesson you shall be able to
- **state the function of an oscillator**
- **name the two main classifications of oscillators**
- **explain the principle of oscillation in a tank circuit**
- **state the Barkhausen criterion**
- **list the basic requirements for an oscillator**
- **list the feed back requirement for an amplifier to take-off and have sustained oscillations**
- **explain the working of parallel-fed Hartley oscillator with the help of a circuit**
- **calculate frequency of oscillations, for the given values of L & C.**

OSCILLATOR

An oscillator is a circuit for producing voltages that vary in a regular fashion with respect to time. The output wave forms of oscillators are repeated exactly in equal successive intervals of time as shown in Fig 1a and Fig 1b.



The output wave-form of an oscillator may be sinusoidal as shown in Fig 1a. Such oscillators are known as **sine wave oscillators** or **harmonic oscillators**.

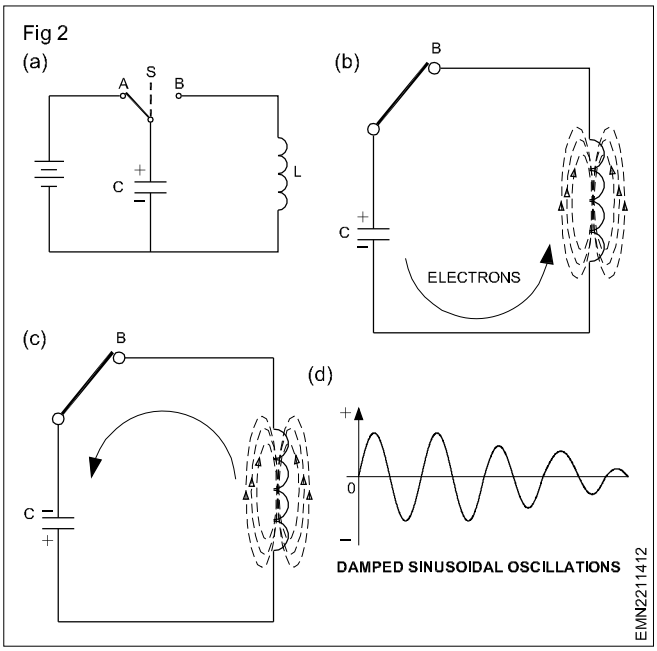
The output of oscillators may be square, triangular or saw-tooth waveform as shown in Fig 1b. Such oscillators are known as non-**sinusoidal oscillators** or **relaxation oscillators**.

Principle of sinusoidal or harmonic oscillations

Fig 2a shows an inductor and a capacitor connected in parallel as a parallel LC resonant circuit. A parallel LC circuit is also known as *tuned circuit* or *tank circuit*.

In Fig 2a, when switch S is put into position A, the capacitor gets charged with the bottom plate being negative and the top plate positive. This means, energy is stored in the capacitor in the form of an electric charge.

When switch S is put into position B, as in Fig 2b, the



capacitor starts discharging through the inductor, creating an expanding magnetic field around L. Since the inductor has the property of opposing any sudden change in current through it, the current builds up slowly.

Once the capacitor gets fully discharged, the magnetic field around L begins to collapse. The collapsing magnetic field, induces a voltage (back-emf) in L. This back emf tends to maintain the electron flow through L in the same direction as when C was discharging. Hence, this back emf in the inductor starts charging the capacitor with opposite polarity as shown in Fig 2c. After the magnetic field has totally collapsed, C would have got charged in the opposite direction as shown in Fig 2c.

Again capacitor C discharges through the inductor in the opposite direction. An expanding magnetic field appears around L but in the opposite direction.

This process continues back and forth, causing the electrons to oscillate in the tuned tank circuit. If the inductor was ideal(zero resistance) and the capacitor was totally loss-free, this process would have continued indefinitely, and would have resulted in a continuous sinusoidal waveform as shown in Fig 1a. However, owing to the resistance in an practical inductor, and the

losses in the capacitor due to the resulting I^2 R(heat loss), the amplitude of the oscillation decreases gradually(damped) and ultimately the oscillations die down as shown in Fig 2d.

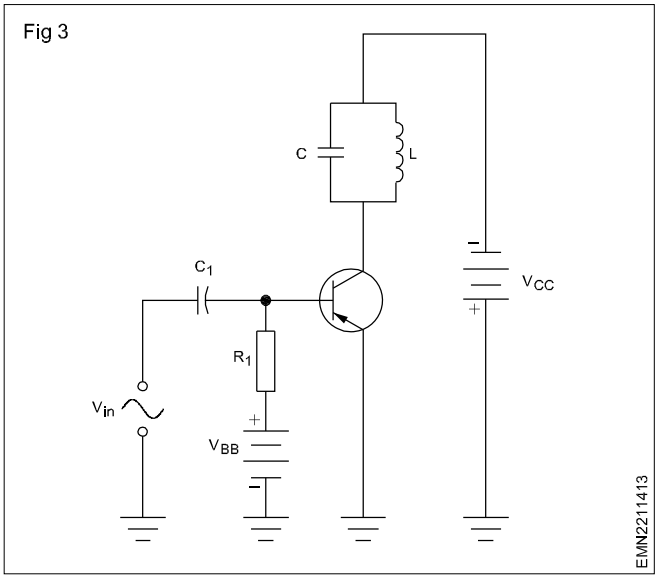
The frequency of oscillation produced by the resonant frequency is given by,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Overcoming losses in tank circuit for sustained oscillations

To avoid the damping of oscillations, when the energy fed into the circuit has been used up, it is necessary to supply more energy by charging the capacitor again. As shown in Fig 2a, by switching S between A and B at proper time, the oscillations can be maintained thus obtaining sinusoidal waveform of constant amplitude and frequency.

Fig 3



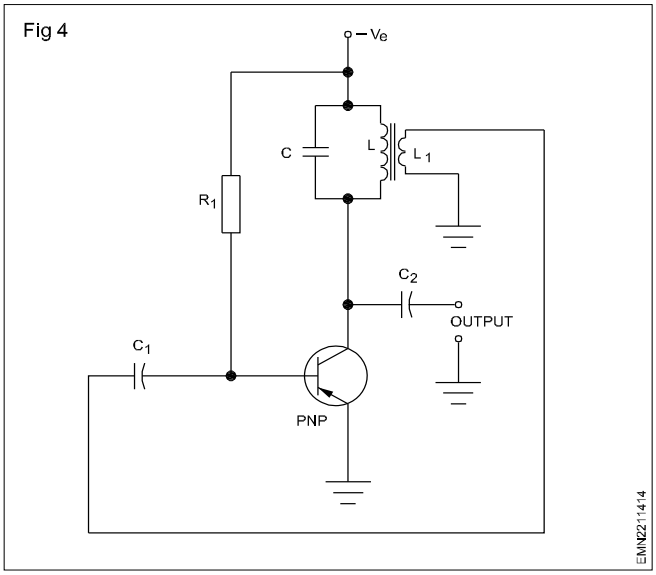
In Fig 4 a transistor amplifier connected in such a way that it will cause undamped oscillations without requiring any external signal. Such a circuit is known as an oscillator.

The oscillator circuit at Fig 4 is known as **tickler-coil** oscillator. Here L1 is inductively coupled to L. When power is first switched ON to the circuit, current flows in the transistor. As the current flows through L, it induces a voltage in L1 which is coupled to the base of the transistor and is amplified. If the phase of the feedback voltage is aiding, then there is an increase in the collector current. This action builds up a large current pulse which excites the LC tank into oscillations. The signal fed by L1 to the base of the transistor is a sine wave of the same frequency as that in the LC circuit and of proper phase to sustain the oscillations. The signal induced in the base thus eliminates the need for an external input to the oscillator and the LC tank will oscillate as long as the DC power to the circuit is ON.

The feedback given to the amplifier in Fig 4 in the proper phase so as to sustain(keep going) oscillations is referred to as positive feedback or **regenerative feedback**.

BARKHAUSEN CRITERION

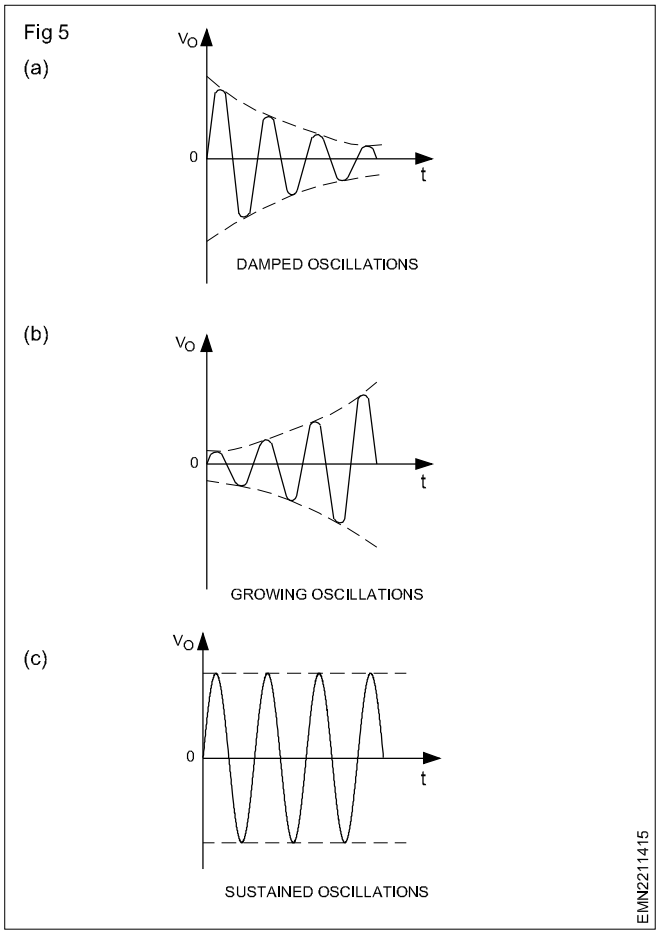
Fig 4



The mathematical analysis for an amplifier to oscillate on its own is given below:

– In the amplifier shown in Fig 4, assume that the gain of the amplifier is A and the feedback factor is β. If the product of $A\beta$ is less than 1 ($A\beta < 1$), then the output signal will be a damped oscillations which will die down as is shown in Fig 5a.

Fig 5



– if $A\beta > 1$, the output voltage builds up as shown in Fig 5b. Such oscillations are called growing oscillations.

– If $A\beta$ = 1, the output amplitude of oscillations remains constant as in Fig 5c.

When the feedback is positive(regenerative), the overall gain of the amplifier with feedback(A_f) is given by,

$$A_f = \frac{A}{1 - A\beta}$$

When $A\beta$ = 1, the denominator of the equation will be zero, and hence A_f=Infinity. The gain becoming infinity means, there is output without any input. i.e. the amplifier becomes an oscillator. This condition **$A\beta$ =1**, is known as **Barkhausen criterion for oscillations**.

Summarizing, the basic requirements for an oscillator are;

1 A stable DC power supply source

2 An amplifier

3 A regenerative (positive) feedback from output to input

4 A LC tank circuit to determine the frequency of oscillations.

Starting signal for oscillators

As discussed above an oscillator gives alternating output voltage without an input signal once the amplifier is given a regenerative feedback. But in a practical oscillator circuit, to start off oscillations, no starting input signal is provided. However, the starting signal of an oscillator is generated by the noise voltage while switching on the oscillator circuit. Such noise voltages are produced due to the random motion of electrons in resistors used in the circuit.

Noise voltage contains almost all the sinusoidal frequencies of small amplitude. However, it gets amplified and appears at the output terminals. The amplified noise now drives the feedback network, which is a resonant tank circuit. Because of this tuned tank circuit, the feedback voltage $A\beta$ is maximum at a particular frequency f_r, which will be the frequency of oscillations. Furthermore, the phase shift required for positive feedback is correct at this frequency f_r only. Thus although the noise voltage contains several frequency components, the output of the oscillator will contain a single sinusoidal frequency f_r the resonant frequency of the tank circuit.

To summarize, the following are the requirements of an oscillator circuit to take-off with oscillations and have sustained oscillations;

– There must be positive feedback.

– Initially the loop gain product $A\beta$ must be > 1.

– After the circuit starts oscillating, the loop gain product $A\beta$ must decrease to 1 and remain at 1.

Hartley Oscillator

One of the simplest of sinusoidal oscillators is the Hartley oscillator shown in Figs 6a and 6b.

Shown in Fig 6a is a series-fed Hartley oscillator. This circuit is similar to the ticker-coil oscillator shown in Fig 4, but the tickler circuit coil L1 is physically connected to L, and is hence a part of L(like an auto-transformer). This oscillator is called **series-fed** because, the high frequency oscillations generated and the DC paths are the same, just as they would be in a series circuit. Series-fed Hartley oscillators are not preferred due to their poor stability of oscillations.

Fig 6b is parallel-fed Hartley oscillator commonly used in radio receivers. Parallel-fed Hartley oscillators are known for their high stability of oscillations.

The circuit at Fig 6b is actually an amplifier with positive (regenerative) feedback to have sustained oscillations. The capacitor C_2 and inductor L_2 form the path for RF current in the collector to ground circuit.

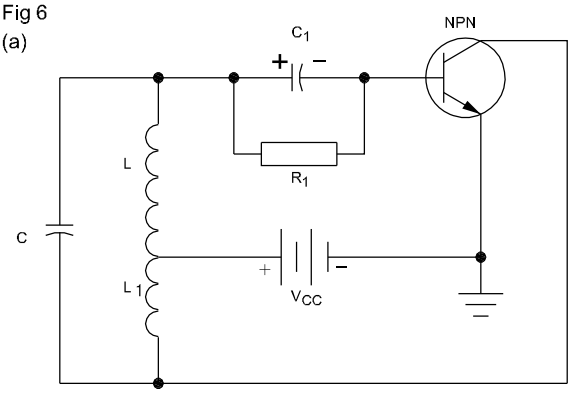
RF current through L_2 induces a voltage in L_1 in proper phase and amplitude to sustain oscillations.

The position of the tap at the junction of L_1 and L_2 determines how much signal is fed back to the base circuit.

The capacitor C and the inductors L_1 + L_2 forms the resonant tank circuit of the oscillator which determines

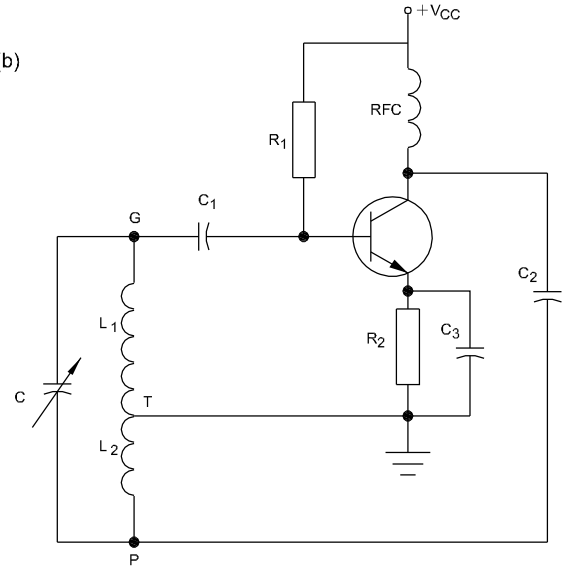
Fig 6

(a)



SERIES - FED HARTLEY OSCILLATOR

(b)



PARALLEL - FED HARTLEY OSCILLATOR

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the frequency of oscillations. Capacitor C can be made as a variable capacitor for tuning the oscillator to different frequencies. C_1 and R_1 form the RC circuit which develops the bias voltage at the base.

The RF choke at the collector keeps the high frequency AC signal out of the V_{CC} supply. In cheaper oscillator circuits the RF choke is omitted and is replaced by a resistor.

Resistor R_2 connected in the emitter provides DC stabilization. R_2 is bypassed by C_3 to prevent AC degeneration.

The Hartley oscillator coil has three connections. These are usually coded on the coil. If they are not, it is generally possible to identify them by a resistance check. The resistance between the taps T and P as shown in Fig 6b, is small compared with the resistance between T and G. If the coil connections are not made properly, the oscillator will not work.

Checking Oscillator Frequency

The frequency of an oscillator can be computed if the values of L ($L = L_1 + L_2$) and C are known using the formula,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

where, f is in hertz, L in henrys, and C in farads.

The frequency of an oscillator may be measured in two ways,

– Using a direct read-out frequency meter also known as frequency counter which is most accurate, popular and easy to use.

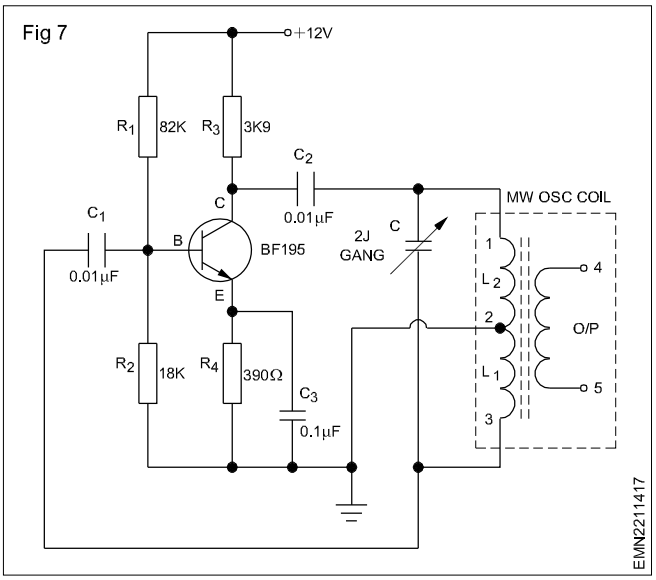
– Using an oscilloscope with a calibrated time base to measure the period of the wave-form. From the measured period, t frequency is calculated using the formula

$$f = \frac{1}{t}$$

where, **f** is the frequency in Hz and **t** the time period in seconds.

A practical Hartley Oscillator circuit using medium-wave oscillator coil as L is shown in Fig 7.

Fig 7



The advantage of using a medium wave oscillator coil for L is that the output can be taken out of the secondary winding (4 and 5) of the coil.

The transistor used is a silicon high frequency transistor (BF series) as the oscillator frequency is in the range of 1 MHz.

The divider biasing is provided to make the DC conditions such that the amplifier works as Class A. With the heavy feedback (large ß), the large feedback signal drives the base of the transistor into saturation and cut-off. This large feedback signal produces negative DC clamping at the base, changing the operation from Class A to Class C. The negative clamping automatically adjusts the value of Aß to 1. If the feedback is too large, it may result in loss of some of the output voltage because of the stray power loses.

When you build an oscillator, you can adjust the amount of feedback to maximize the output voltage. The trick is to use enough feedback to start under all conditions (different transistors, temperature, voltage etc.), but not so much that you lose more output than necessary.

The frequency of oscillations of the oscillator circuit at Fig 7 can be varied by varying the position of the shaft of the gang of the gang capacitor (C_4).

Colpitt's and Crystal Oscillator

Objectives: At the end of this lesson you shall be able to

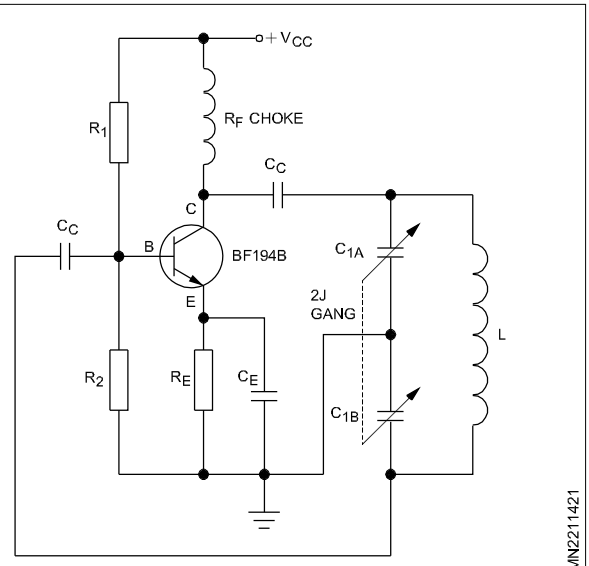
- **state the difference in the feed back method in a Colpitt's oscillator compared to Hartley oscillator**
- **calculate frequency of oscillations for the given the values of L and C**
- **state the main disadvantage of LC oscillators and give reasons**
- **describe the piezo electric property of crystals**
- **explain the AC equivalent circuit of piezo electric crystals**
- **describe the circuit of a crystal oscillator and explain the function of the components.**

COLPITT'S Oscillator

Colpitts oscillator is another type of sinusoidal oscillator or harmonic oscillator which uses a tank circuit for oscillations. Colpitts oscillators are very popular and are widely used in commercial signal generators and communication receivers.

A typical Colpitt's oscillator shown in Fig1 is similar to a Hartley oscillator. The only difference is that the Colpitts

Fig 1



oscillator uses a split capacitor for the tank instead of a split inductor used in Hartley oscillators.

The parallel-fed or shunt-fed Colpitt's oscillator shown in Fig1, uses the common emitter configuration. The capacitors C_{1A} & C_{1B} form the voltage divider used to provide the feedback signal. The voltage drop across C_{1B} determines the feedback voltage. All other components in this circuit have the same function as in the Hartley circuit.

The frequency of oscillations of the Colpitt's oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

where,

f is the frequency of oscillation in hertz,

L is the inductance of the coil in henry

C is the total capacitance in farads given by,

$$C = \frac{C_{1A} \cdot C_{1B}}{C_{1A} + C_{1B}}$$

The frequency of oscillations can be changed by using a miniature ganged capacitor for C_{1A} & C_{1B}.

By varying the shaft of the ganged capacitor, both the capacitances C_{1A} and C_{1B} get varied, and hence, the frequency of oscillations of the oscillator varies.

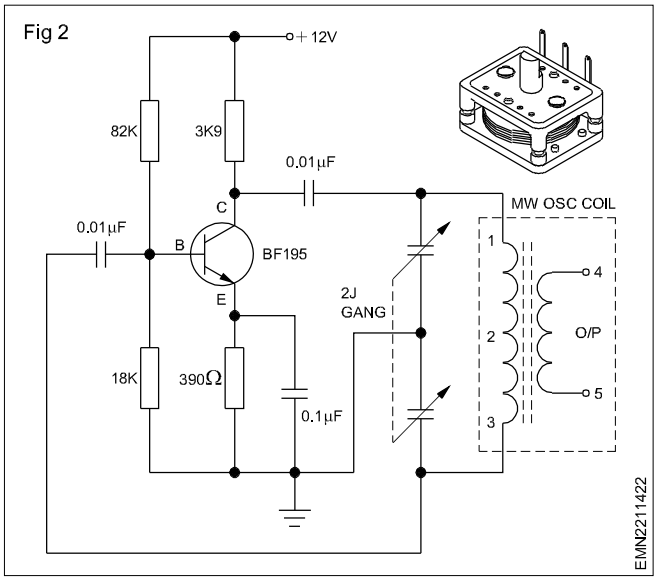
Colpitts oscillators are generally used for generating frequencies above 1 MHz.

A practical Hartley Oscillator circuit using a ganged capacitor for C_{1A} and C_{1B} and a medium wave oscillator coil for L is shown in Fig 2.

Crystal Oscillators

The LC oscillator circuits such as Hartley and Colpitts have the problem of frequency in-stability. The most important reason for the frequency drift in LC oscillators is, the change in value of capacitance and inductance of the tank circuit that occurs when temperature changes. As the temperature increases or decreases, the values of

Fig 2



L and C deviate causing the circuit to oscillate at a frequency different from the desired resonant frequency. Other reasons for frequency deviation are, the leads of transistor, inter electrode and wiring capacitances.

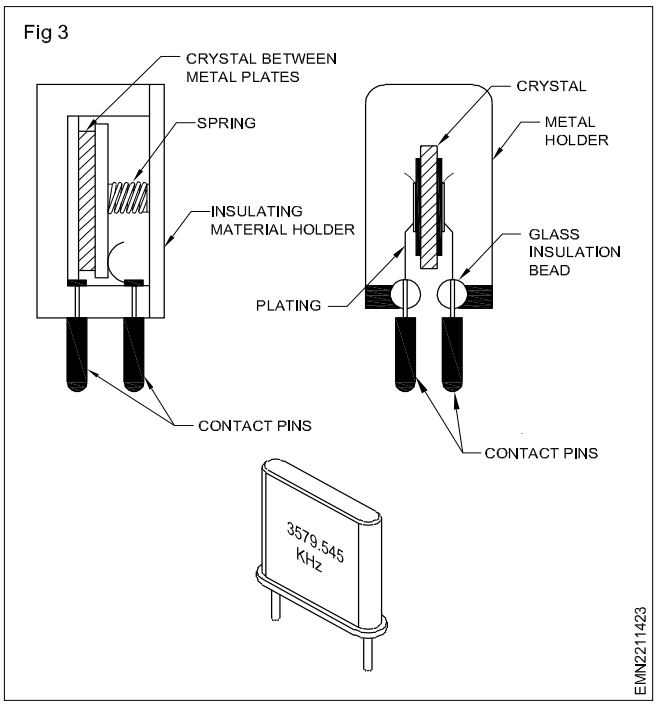
The problem of frequency drift can be largely overcome by using high Q coils and good quality capacitors. But, with ordinary inductors and capacitors, Q-values in excess of a few hundred is very difficult or impossible to achieve.

Large improvements in frequency stability can be achieved by using a **quartz crystal** in the place of the conventional tuned circuit. Such oscillator circuits are referred to as *crystal controlled oscillators*.

Piezo Electric Effect

It was discovered that certain crystals such as **quartz** and **Rochelle**, exhibit a special property known as piezo-electric property. A quartz crystal looks like a piece of thin frosted glass usually cut into 1/4 to 1 inch squares as shown in Fig 3.

Fig 3



When such a crystal is held between two flat metal plates and pressed together, a small emf will be developed between the plates as if the crystal became a battery for an instant. When the plates are released, the crystal springs back to its original shape and an emf of opposite polarity is developed between the two plates. In this way, mechanical energy/force is converted to electrical energy by the crystal. This property is made use of in the pick-ups for gramophone records. In a gramophone record, small mechanical vibrations are produced when the stylus tracks the groove on the gramaphone plate. This vibrating force gives rise to corresponding voltages representing the recorded sound at the pick-up terminals.

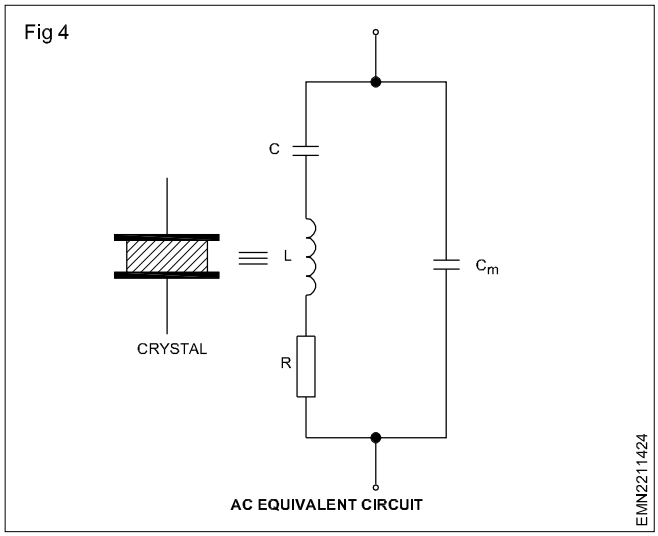
In addition to the above property of the crystal, when an emf is applied across the two plates of the crystal, the crystal will distort from its normal shape. If an opposite polarity emf is applied, the crystal will reverse its physical distorted shape. In this way, these crystals also convert electrical energy into mechanical energy.

The above two reciprocal actions of a crystal are known as **piezo-electric effect**. Such crystals are housed in crystal holders as shown in Fig 3.

Amongst several crystals having this piezo-electric property, the quartz crystal is most popular because, this material is almost perfectly elastic. If mechanical oscillations are started in this crystal it takes a long time for the oscillations to die away. Quartz crystals therefore, have a very high mechanical Q.

So far as the electrical properties are concerned, a quartz crystal is equivalent to the LC resonant circuit shown in Fig.4.

Fig 4



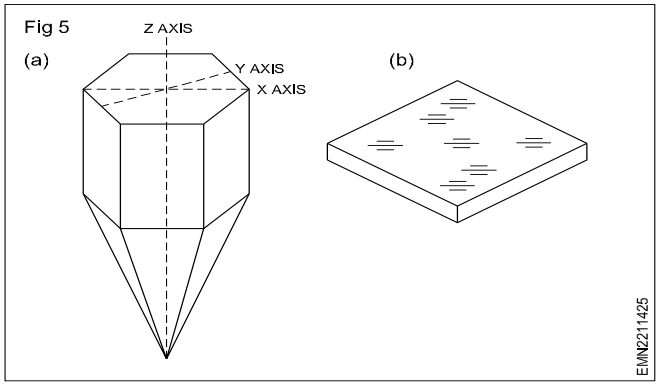
The values of L, R, C and C_m depend upon the physical size of the crystal and how the crystal is cut from the original mass. Capacitance C_m represents the mounting capacitance. For using the crystal in electronic circuits, two conducting electrodes are placed on to its two faces. Connecting leads are then joined to these electrodes. When the leads are connected to a source of oscillating voltage, mechanical vibrations are set up within the crystal. If the frequency of the oscillating voltage is close to a resonant frequency of the crystal, then the crystal forces the oscillating voltage to coincide with the oscillating frequency of the crystal. Hence, in an oscillator, by using the crystal in the place of an LC resonant circuit, the frequency of oscillation is determined almost entirely by the crystal. Q values in excess of 20,000 are easily obtained with readily available crystals resulting in highly stable oscillating frequency.

Hence, when accuracy and stability of the oscillation frequency are important, a quartz crystal oscillator is used instead of Hartley or Colpitts oscillators.

Crystal cuts

The natural shape of a quartz crystal is a hexagonal prism with pyramids at the ends as shown in Fig 5a.

Fig 5



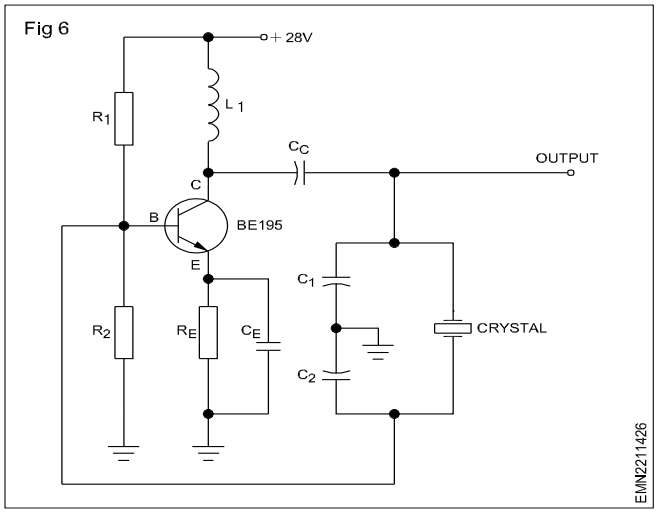
To get an usable crystal out of this, a rectangular slab is cut out of the natural crystal as shown in Fig 5b. Depending upon the angle of the cut and the thickness of the slab, the fundamental frequency of vibration of the crystal varies. The resonant frequency of a crystal is usually between 0.5 and 30 MHz.

Pierce crystal oscillator

The pierce crystal controlled oscillator shown in Fig 6 is often used because it requires very few components and has good frequency stability.

The pierce crystal oscillator is similar to the Colpitts oscillator but for the inductance coil replaced by a crystal. Here the crystal across the collector and the base terminals of the transistor determines the oscillating frequency. As in a Colpitts oscillator, capacitors C_1 and C_2 form a capacitive voltage divider for feedback. The AC voltage across C_2 provides the necessary positive feedback to the base.

Fig 6



In Fig 6, the crystal acts like an inductor that resonates with C_1 and C_2. In the base circuit, the R_1R_2 divider supplies forward bias voltage from the V_{cc}. Bias stabilization is provided by the R_E C_E combination in the emitter circuit.

In Fig 6, if the crystal resonant frequency is, say 3579.545 Hz, then the oscillator oscillates at the same frequency and gives a sinusoidal output of 3579.545 Hz.

Crystal oscillators are generally used in,

– mobile radio transmitters and receivers

– broadcast transmitters

– test equipments such as signal generators where exact frequency and very high frequency stability are of utmost importance. The frequency drift in crystal controlled oscillators will be less than 1 Hz per 10^6 Hz.

RC feedback oscillators

Objectives: At the end of this lesson you shall be able to

- **state why LC oscillators are not suitable for frequencies less than 50 kHz**
- **name the two important types of RC oscillators**
- **explain the circuit diagram of a wein-bridge oscillator**
- **calculate the frequency of oscillations using the values of the circuit components**
- **state the most suitable range in which a wein-bridge oscillator can be used.**

RC Oscillators

LC oscillators are not suitable for generating frequencies less than 1 MHz. To make audio frequency oscillators (<20 kHz) if LC oscillators are used, the LC values required will be too large. Hence, LC tuned circuit is not used in audio frequency oscillators.

For generating audio frequencies, resistors and capacitors(RC) can be used to provide the necessary phase shift for positive feedback. Then, the frequency of oscillations depends on the RC values. Two important types of RC oscillator are;

– the RC phase-shift oscillator

– the Wien-bridge oscillator.

Wein-bridge oscillator

Wein-bridge oscillator is a standard oscillator for generating low frequencies in the range of 10 Hz to 1 MHz. Wien-bridge oscillator is a RC feedback oscillator.

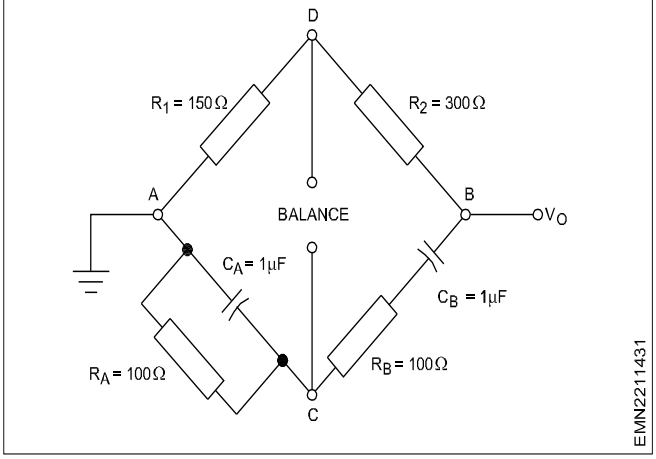
Positive feedback is applied through the path with R_B C_B and $R_A C_A$ to the + terminal. This feedback produces oscillations.

The circuit diagram of wein bridge oscillator is shown in Figure.

It is essentially a two stage amplifier with a RC bridge (known as wien bridge). The four arms of bridge consist of R_1 in series with C_1, R_2 parallel with C_2, R_3 and R_4. The wein bridge oscillator uses both positive and negative feedback-positive feedbacks through the path with R_1C_1 and R_2C_2 to the base of a. The negative feedback is through voltage divider R_3 & R_4. R_1 is normally in the form of temperature sensitive lamp. Whose resistance increase with increase in current.

The circuit oscillates only at the frequency at which the bridge is balanced. In this condition the positive feedback is balanced with negative feedback. The frequency at which the bridge will oscillate can be calculated using the formula.

Fig 1



$$f = \frac{1}{2\pi R C} Hz$$

In the bridge circuit if R_1 is series with C_1 produces a current lag R_2 in parallel with C_2 will produce a lead to one particular frequency. Hence the total phase shift of the bridge circuit will be zero.

The 360° phase shift (positive feedback) required for oscillator is obtained by using 2 stage amplifier. Q1 transistor introduces 180° phase shift and Q_2 transistor introduces another phase shift of 180°.

Operation: The circuit is set in oscillation by any random changes in base current of transistor Q_1 that may be due to noise inherent in the transistor or variation in voltage of dc supply. This noise or varion is base current is amplified by two stage amplifier and feedback to wien bridge. The bridge will allow only one particular frequency for which total phase shift will be zero. This frequency is further fed to amplifier and sustained oscillations are obtained.

Advantages

1 Provides a stable low distribution output over a wide range of frequency.

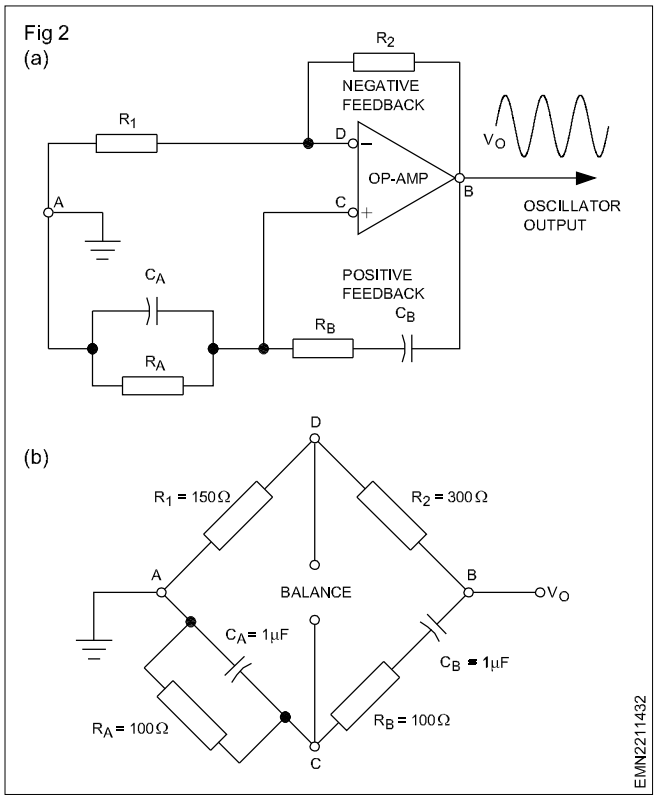
2 The frequency range can be selected simply by using decade resistance boxes.

3 The frequency of oscillation can be easily varied by varying C_1 & C_2 simultaneously.

Disadvantages

1 The circuit needs two transistors and a large number of other components.

2 The maximum frequency output is limited because of amplitude and the phase shift characteristics of amplifier.



RC Phase Shift Oscillator

Objectives: At the end of this lesson you shall be able to

- **state the essential requirements to make an oscillator**
- **state the value of the loop gain kA_v to have self- sustained oscillation**
- **state the schematic of a transistor RC phase-shift oscillator**
- **state the equation for frequency of oscillations in a transistor phase-shift oscillator**
- **state the equation for finding the required minimum β of the transistor in a RC oscillator.**

An oscillator will have no input AC signal at all, but it still generates AC signal. An oscillator will have only a DC supply. The oscillator circuit, makes use of the noise generated in resistors at the switching on time of DC supply and sustains the oscillations.

To build an oscillator, the following are essential;

1) An amplifier

2) A circuit which provides positive feedback from output to input.

The gain of an amplifier with feedback is given by,

$$A_{vf} = \frac{A_v}{1 - kA_v}$$

kA_v is known as the loop gain of the amplifier.

If the loop gain kA_v is made equal to 1, and, if the sign of kA_v is made positive, i.e. by feeding back signal which is in-phase with the input signal, then there will be an output signal even though there is no external input signal. In other words, an amplifier is modified to be an oscillator by positive feedback such that it supplies its own input signal.

Example: An amplifier has a voltage gain of 40 without feedback. Determine the voltage gains when positive feedback of the following amounts is applied.

(i) k = 0.01 (ii) k = 0.02 (iii) k = 0.025

SOLUTION

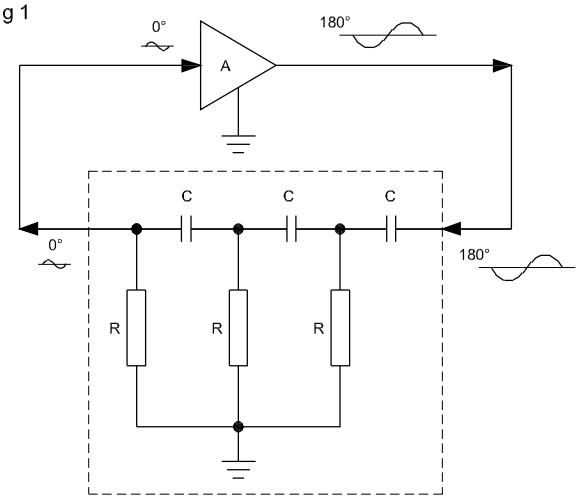
$$(i)\ A_{Vf} = \frac{A_V}{1 - kA_V} = \frac{40}{1 - 0.01 \times 40} = \frac{40}{0.6} = 66.7$$

$$(ii)\ A_{Vf} = \frac{A_V}{1 - kA_V} = \frac{40}{1 - 0.02 \times 40} = \frac{40}{0.2} = 200$$

$$(iii)\ A_{Vf} = \frac{A_V}{1 - kA_V} = \frac{40}{1 - 0.025 \times 40} = \frac{40}{0} = \alpha$$

In (iii) the gain of the amplifier become infinite when the loop gain kA_v = +1. This is known as the critical value of the loop gain kA_v. It is important to note that the output voltage cannot be infinite. Instead the amplifier will start working as an oscillator without the need of any separate input. If the feedback path contains a frequency selective network, the requirement of kA_v = 1 can be met at only one particular frequency, such that, the output of the oscillator will be a sinusoidal signal of a particular frequency. Such oscillators are known as sine wave oscillators.

Fig 1



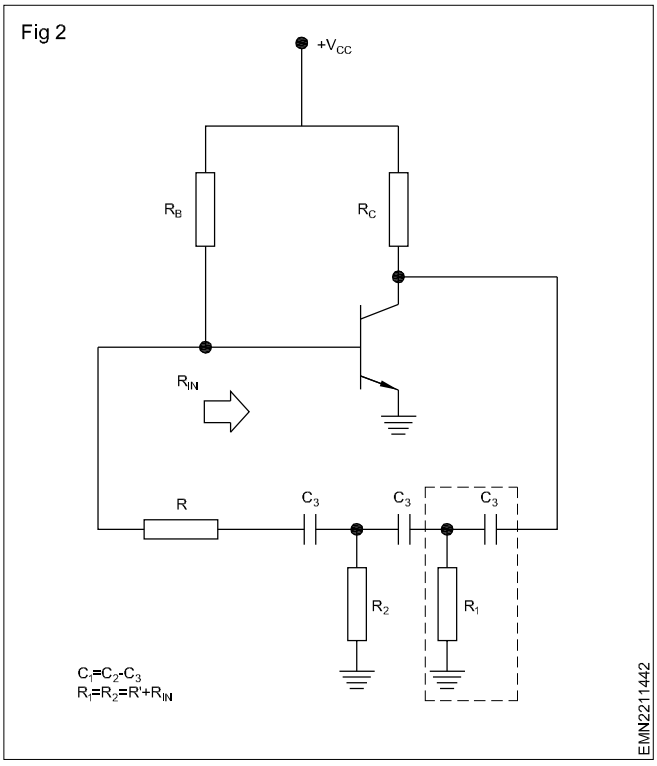
One of the simplest form of sine wave oscillators is the phase shift oscillator. Fig 1 shows the principle behind an R.C phase shift oscillator.

The feedback network shown in Fig 1 consists of resistors and capacitors which provide the required phase shift of 180° at a particular frequency f given by,

$$f = \frac{1}{2\pi\ C\sqrt{6}} \qquad .....[1]$$

The other condition to be satisfied for oscillations to occur is that, the loop gain kA_v should be equal to unity. To satisfy this condition, using classical network analysis, it can be found that, the value of k should be, $k = \frac{1}{29}$

Fig 2



Therefore, the voltage gain of the amplifier A_v stage must be greater than 1/k or greater than 29 so that kA_v becomes equal to 1.

Transistor RC phase shift oscillator

Fig 2 shows a single transistor phase shift oscillator using resistors and capacitors in a feedback network.

There are three sections of R and C in the feedback network. Each RC section provides a 60° phase shift at a specific frequency, resulting in a 180° phase shift as required for positive feedback. This satisfies one of the two required conditions for oscillations.

In Fig 2, the feedback signal is coupled through a feedback resistor R' in series with the amplifier stage input resistance R_{in}. Resistor R' can be made variable for adjusting the oscillator frequency. For each of the three sections of R_C phase shift network to produce 60° phase shift, it is necessary that $C_1 = C_2 = C_3$ and $R_1 = R_2 = R' + R_{in}$.

The other required condition for oscillation, i.e. loop gain kA_v to be unity is satisfied by the circuit at Fig 2, when b of the transistor used in the circuit is,

$$h_{fe} \approx \beta = 23 + 29\frac{R}{R_c} + 4\frac{R_c}{R} \qquad .....[2]$$

where, $R_1 = R_2 = R$

When β is atleast the value given by equation [2] or greater than, the circuit at Fig 2 it will oscillate.

Practical transistor RC phase shift oscillator

Fig 3 shows a practical transistor RC phase shift oscillator which is similar to that shown in Fig 2.

In Fig 3 note that resistor R_3 (in Fig 2 it is denoted as R') used for frequency adjustments is connected in series with one of the resistors of the RC section. Resistor R_4 provides the necessary bias stabilisation for the transistor operation. Note that a small value capacitor C_4 is connected in shunt with the input. The purpose of C_4 is to bypass the unwanted high frequency oscillations to ground. The value of R_3 can be varied to adjust the frequency of oscillations. However, the variation that can be obtained by R_3 is limited.

For the circuit at Fig 3, the frequency of oscillation is given by,

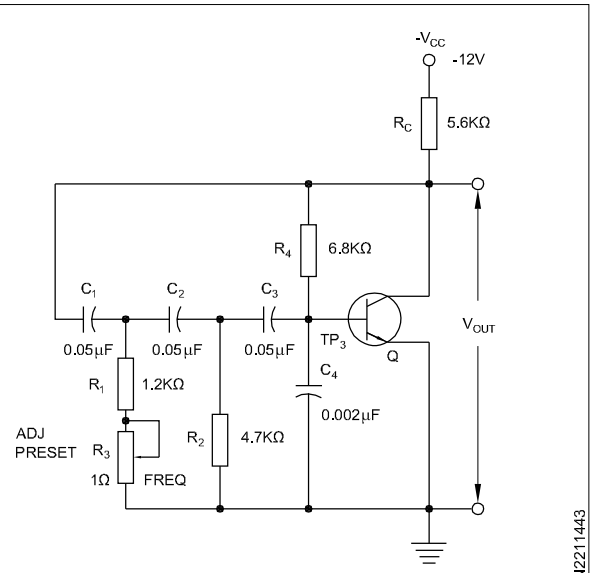
$$f = \frac{1}{2\pi\sqrt{6R_1^2 + 4R_1R_c}} \qquad .....[3]$$

where, $C = C_1 = C_2 = C_3$

The minimum value of h_{fe} or b of the transistor used in the circuit at Fig 3 should be,

$$h_{fe} \approx \beta = 23 + 29\frac{R_1}{R_c} + 4\frac{R_c}{R_1}$$

Fig 3



Using the component values at Fig 3, the b of the transistor used should be a minimum of,

$$\beta = 23 + 29\frac{1.2K}{5.6K} + 4\frac{5.6K}{1.2K} = 47.89$$

The frequency of oscillations can be increased by decreasing the value of R or by decreasing the value of C.

In the practical circuit at Fig 3, collector feedback bias is employed to ensure that the transistor will never go to saturation. Other biasing techniques such as voltage divider bias can also be used for dc biasing of the transistor. Since the frequency of oscillations is decided only by the feedback phase shift network, biasing resistors will not have any effect on the frequency of oscillations. The important point to be noted is that the b of the transistor should be higher than the minimum b given in equation 2 to have sustained oscillations.

RC time Constant

Objectives: At the end of this lesson you shall be able to

- **explain the importance of RC time constant**
- **state the need of universal time constant curve**
- **list a few applications of RC time delay circuits**
- **explain the use of oscilloscope in measuring time delay.**

RC time constant τ while charging

When a capacitor is connected across a battery or a source of dc voltage as shown in Fig 1a, it charges almost instantaneously. This is because there is no resistance in the charging circuit to limit the charging current. On the other hand, if a resistor is connected in series with the capacitor, as shown in Fig 1b, the resistance limits the maximum current that can flow in the series circuit. This limiting of charging current causes delay in the time required for the capacitor to charge up-to the source voltage.

Even if a resistor were not connected in the circuit , the resistance due to connecting wires, leads internal resistance of the supply source acts as a lumped resistance to delay the charging. The exact time required for the capacitor to charge depends on both the resistance (R) in the charging circuit, and the capacitance (C) of the capacitor(recall higher capacitance value allows higher current in the circuit, I = CV/t).

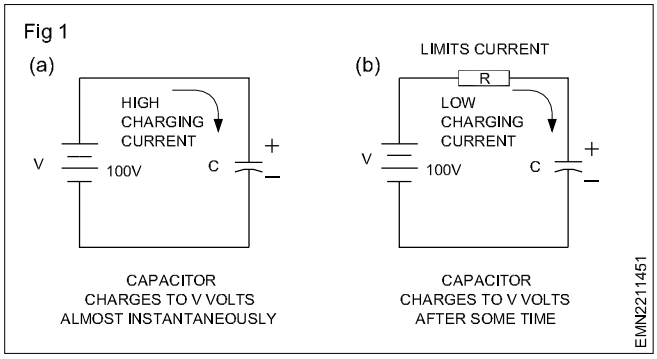
This relationship between resistance, capacitance and the charging time is expressed by the equation,

t = RC

where t (spelled as tow) is the capacitive time constant or RC time constant, representing the time required for the capacitor to charge to 63.2% of its full charge voltage.

It is interesting to note that, in each succeeding time constant t , the voltage across the capacitor increases by

Fig 1



an additional 63.2 % of the remaining voltage. Thus, after the second time constant (2t) the capacitor would have charged to 86.4 % of its maximum voltage,

– after 3t, 94.9 percent, of its maximum voltage,

– after 4t, 98.1 percent, of its maximum voltage

and – after 5t, more than 99 percent of its maximum voltage.

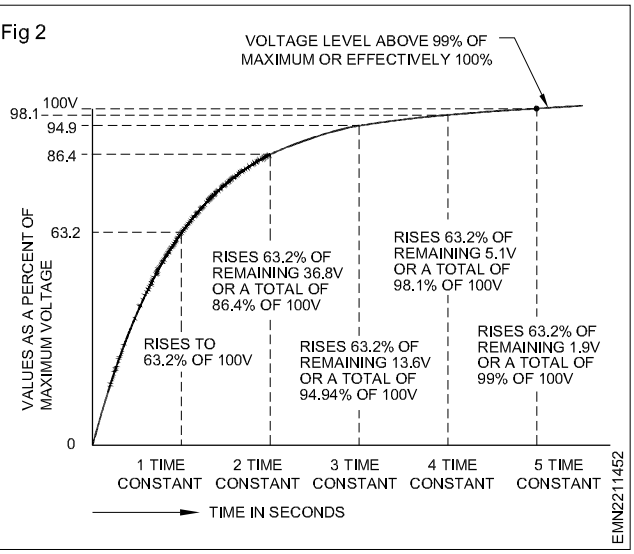
Fig 2 shows the charging curve of the resistor - capacitor (RC) circuit shown in Fig 1 and its relationship with RC time constant, t.

Hence, the capacitor is considered to be fully charged only after a period of more than five time constants or atleast five time constants.

RC time constant while discharging

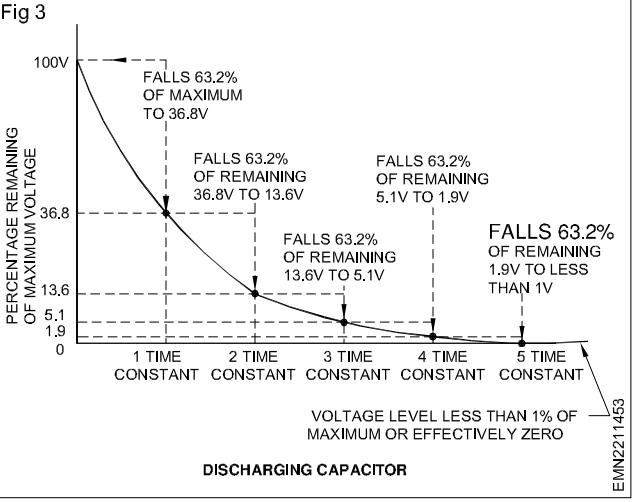
As in charging, while a capacitor is discharging, there is time delay in discharging the stored charges depending

Fig 2



upon the value of resistance and capacitance. This discharge time constant t, is also given by RC. This time constant gives the time required for the voltage across a discharging capacitor to drop to various percentages of its maximum value as shown in graph at Fig 3.

Fig 3



Notice the similarity between the capacitive time constant and the inductive time constant, discussed in previous lessons. The similarity is that, the voltage across a capacitor and the current through an inductor builds up/rises and drops off/falls exactly in the same way.

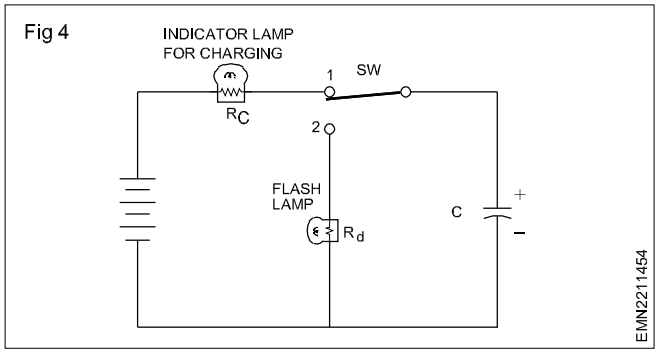
Application of capacitor in camera flash units

A typical circuit of a flash unit is shown in Fig 4. A flash unit produces a short duration, high current pulse without drawing a large current from the supply.

When the flash unit is charging, switch SW is in position 1. The lamp resistance R_C will be large. This high resistance limits the peak charging current I_C to a low value such that the capacitor charges gradually with a large time constant $t_1 = R_C C$.

When the switch is thrown to position 2, the low resistance R_d of the flash lamp allows a high discharge current through it. Hence the bulb glows very brightly for a very small duration. The duration of this current is determined by the time constant $t_2 = R_d C$.

Fig 4



All similar system of obtaining high surge current is used in applications like, electric spot welding, radar transmitter tubes etc.

Universal time-constant curves

To determine the voltage and current in a capacitor at times other than 1 τ ,2 τ ,....5 τ time constants, the universal time-constant curves are used. Refer pocket table book, table no.14 for the universal time-constant curve.

The universal time-constant curves give the instantaneous voltage across the capacitor as a percentage of the initial or final values, with time given in time constants t. From the graph, note that at one time constant t, the capacitor would have charged to 63% of its final steady-state voltage. Also at this point the charging current has dropped to only 37% of its initial maximum value current. Note that, in either case, a change of 63% occurs in one time constant.

From these curves it can also be confirmed that, the Charging or discharging of a capacitor is complete after five time constants.

For the circuit at Fig 5, using the universal time constant curves, determine the capacitor voltage after 3.5 seconds.

SOLUTION

$\tau = R_1 C$

$= 220 \times 10^3 W \times 10 \times 10^{-6} F$

$= 2.2$ seconds.

Allowed charge time t = 3.5s

Equivalent number of time constants is equal to

$$= \frac{3.5s}{2.2s/\tau} = 1.59\ \tau \approx 1.6\ \tau$$

From the universal graph

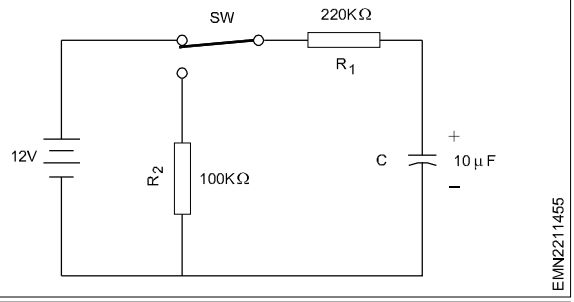
where $\tau = 1.6\ \tau$, V_C is almost = 80% of V (the final value).

Therefore,

V_C = 80% of 12 volts

= 0.8 x 12 V = 9.6 volts.

Fig 5



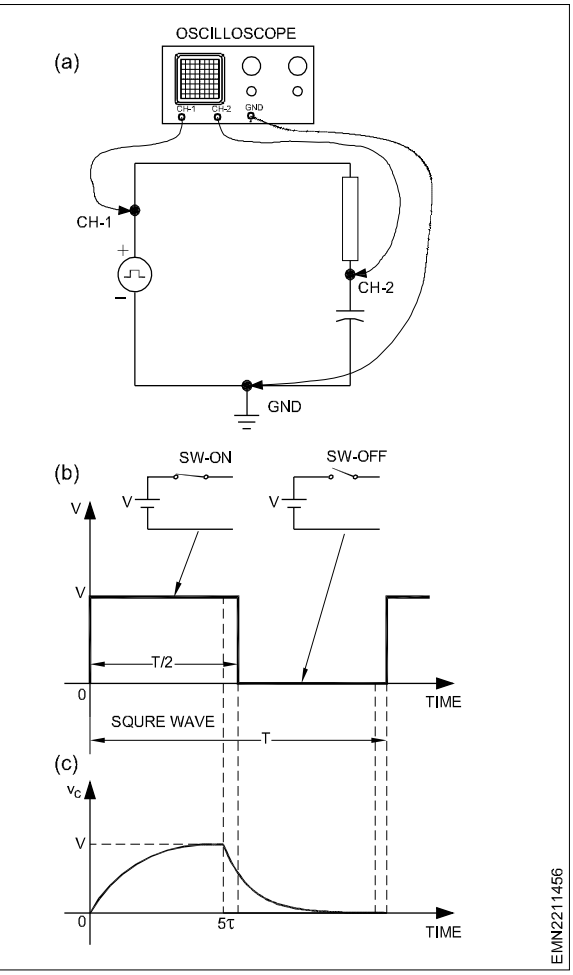
While calculating the discharge time constant, the total series resistance R_1+R_2 must be considered.

Measurement of voltage levels and capacitance using oscilloscope

A charging and discharging wave-form of a R-C circuit can be seen using an oscilloscope. However, it is difficult to view the charging and discharging of a R-C circuit having a switch similar to the one shown in Fig 5. This is because, the wave-forms appear and disappear on the screen. Hence, instead of a switch, a square wave signal as shown in Fig 6b, whose voltage level changes between 0 and V, just as a switch repeatedly switched ON and OFF, can be more conveniently used.

The advantage of using a square waveform is that, the rate of switching (ON/OFF) can be increased or decreased by increasing or decreasing the frequency of the wave-form (more optly known as pulse repetation rate, PRF).

Fig 6



The output of a square wave signal generator is connected to the capacitive circuit as shown in Fig 6a. The frequency of the waveform (rate of switching ON/OFF of circuit) is adjusted until the voltage wave-form across the capacitor is similar to that as in Fig 6c. Here, half-period of the square wave output (T/2) is equal to or greater than five time constants, that is T/2 ³ 5 RC(τ).

With the oscilloscope connected across the capacitor, as shown in Fig 6a, the time required to reach 63% of the final voltage is the time constant, t. The voltage levels at 1t, 2t etc can be easily measured if the Time/Div of the CRO is made equal to the time constant t.

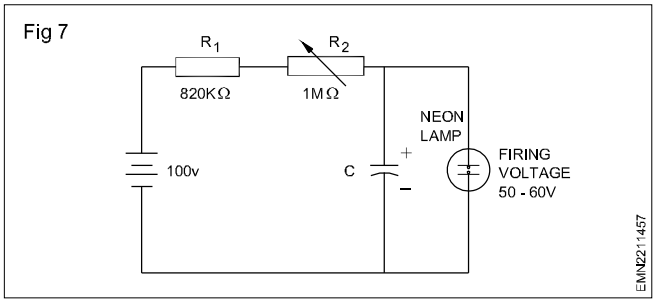
If the total resistance of the circuit is known, the capacitance of the capacitor, if unknown, can be calculated using the formula,

$$C = \frac{T}{R} \text{(Derived fromthe formula,T= RC)}$$

Application of R-C delay circuits

An RC circuit with a large time constant can be used to introduce delay in a circuit as shown in Fig 7.

Fig 7



Here, the neon lamp acts as an open circuit until a firing voltage of the lamp is reached(50-60V). When the circuit is switched ON, the voltage across the capacitor charges toward the final value of 100V, with a time constant of (R_1 + R_2)C. When the charge across the capacitor reaches a value between 50 to 60 volts, the firing voltage of the neon lamp is reached and the lamp fires. The capacitor, hence, discharges through the neon lamp, lighting it up. Because of the low resistance of the neon lamp, the capacitor voltage drops quickly and the lamp gets extinguished after being lighted for a brief period of time(flashing). The lamp once again becomes an open circuit and the capacitor starts recharging, providing a controlled delay time before the lamp one again fires. The rate of flashing can be varied by adjusting R_2.

The delay introduced by the R-C in circuit in Fig 7 can be used for several other useful purposes. For example, if it is required to delay the switching ON of a DC relay following the application of voltage to the relay coil, the circuit at Fig.7 can be used.

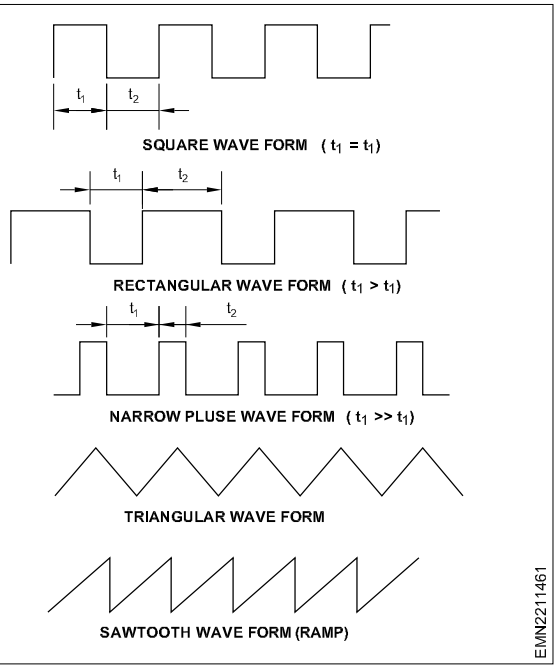
Multivibrators and Study of Circuit Diagrams

Objectives: At the end of this lesson you shall be able to
- **state the function of relaxation oscillators**
- **state the meaning of clock in the digital system**
- **explain the circuit of an astable multi-vibrator**
- **calculate the ON-time, OFF-time and PRF of astable multi-vibrators given values of R and C**
- **list a few applications of an astable multi-vibrator**
- **explain the difference among a astable multi-vibrator monostable multi-vibrator and bistable multivibrator**
- **draw the circuit of mono-shot and calculate the ON-time of the output pulse**
- **explain bistable multi-vibrator as Rs flip flop.**

NON SINUSOIDAL OSCILLATORS

A relaxation oscillator is a circuit for generating non-sinusoidal oscillations. These circuits can be used to give different types of repetitive wave-forms other than sine waves. A few types of non sinusoidal wave forms generated using relaxation oscillators are shown in Fig 1.

Fig 1

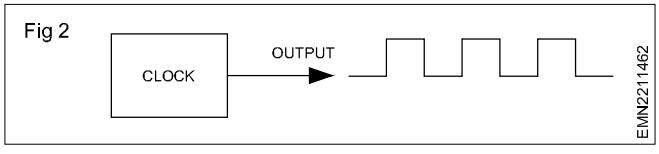


Amongst the different types of wave forms shown in Fig.1, the rectangular wave form is most frequently used for several applications. A few such applications are:

– Digital clocks, Digital computers and Digital equipments.

All digital systems need a reference frequency referred to as clock frequency to time the operation of the various sections of the system. This clock frequency is generated using a clock generator. A clock generator is nothing but a relaxation oscillator circuit which produces repetitive wave-forms, generally square wave as shown in Fig 2.

Fig 2



The output of this relaxation oscillator(clock generator) will be continuous pulses having two distinct states HIGH and LOW. A High state corresponds to a constant voltage (say 5V) and the low state corresponds to a different constant voltage(say 0V). These high and low states are repeated at definite intervals.

The clock generator or the relaxation oscillator used for generating pulse wave-forms as shown in Fig 2 is commonly known as a Multivibrator. A few applications are;

Electronic Keyboards or Pianos: In entertainment electronics, relaxation oscillators generating square wave-forms are essential for the production of electronic music. This is because, square waves are rich in harmonics.

Test and Measuring Instruments: The rectangular, square and sawtooth wave-forms generators are extensively used in Oscilloscopes(CRO's), Function generators and so on.

Timers and Industrial controls: Rectangular, square wave generators are extensively used to control the delay time in switching-on and duration of on-period and several such industrial control requirement applications.

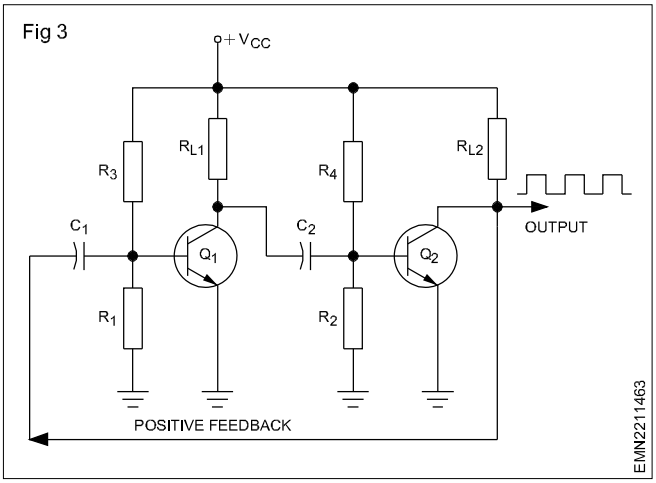
Above listed applications of non-sinusoidal waveform generators are only a few of its vast applications.

ASTABLE MULTI-VIBRATORS

A basic multi-vibrator circuit for generating square-wave is shown in Fig 3.

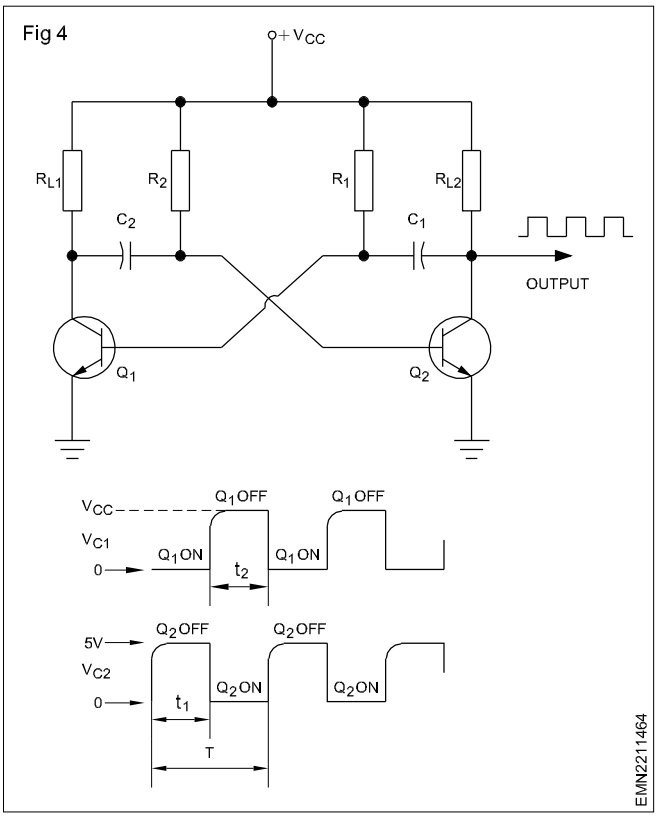
As can be seen, the multivibrator has two amplifier stages with feedback. The output of Q_1 drives the input of Q_2, and

Fig 3



the output of Q_2 is fed back to Q_1. Since each CE amplifier stage introduces a phase shift of 180 degrees to its input signal, the signal fed at the input of Q_1a under goes a total phase shift of 180+180 degrees at the output. A 360 degrees phase shift between the input and output means, they are in phase. Hence, if the output signal is fed-back to input, it results in positive feed-back, which results in oscillations.

Fig 4 is a redrawn circuit of the multivibrator circuit at Fig 3. The circuit is redrawn for the sake of easier understanding of the working and waveforms.



In Fig 4, the oscillations are produced by switching ON-OFF of transistors. When one amplifier (stage) conducts, it cuts-off the other amplifier. When the stage which was OFF, starts to conduct, this action cuts-off the stage which was ON. This circuit is referred to as a relaxation oscillator because, at any instant of time, one amplifier stage is will be resting while the other is working.

The rate at which Q_1 and Q_2 are switched ON and OFF determines the oscillator frequency. As can be seen from the output wave form of the oscillator at Fig 4, the duration for which Q_1 is OFF is called the ON time of the pulse and the duration for which Q_1 is ON is called the OFF time of the pulse. The sum of one ON time plus one OFF time is called the time-period, T, of the wave form.

$$T = t_1 + t_2$$

If $R_1 = R_2$, $R_{L1} = R_{L2}$, $C_1 = C_2$ and Q_1 & Q_2 are identical, then, the ON time and OFF time due to both Q_1 and Q_2 will be same.

For instance, if each stage is ON or OFF for 0.5 ms, then the time period T is simply given 2 x 0.5 ms = 1 ms. Then the frequency of the multi-vibrator is 1/ T = 1000 Hz.

Referring Fig 4, the period for which transistor Q_1 and Q_2 stays OFF is determined by the RC time constants of R_1 & C_1 and R_2 & C_2. It takes about 0.69 time constants(τ = RC) for the RC network to reach the base turn-on voltage. This gives the way to estimate the time that each transistor will be held in the off state.

$$t = 0.69RC.$$

If $R_1 = R_2$ and $C_1 = C_2$,

then,

$t_1 = t_2$ and T will be 2(0.69RC).

Example: If $R_1=R_2$= 47KW and $C_1=C_2$= 0.05µF, then the off-time of transistor will be,

$$t = 0.69 \times 47 \times 10^3 \times 0.05 \times 10^{-6}$$

$$= 1.62 \text{ m Sec.}$$

Since $R_1 = R_2$ and $C_1 = C_2$, $t_1 = t_2 = 2\,t$

$$T = 2 \times t = 2 \times 1.62 \text{ m Sec.}$$

$$= 3.24 \text{ m Sec.}$$

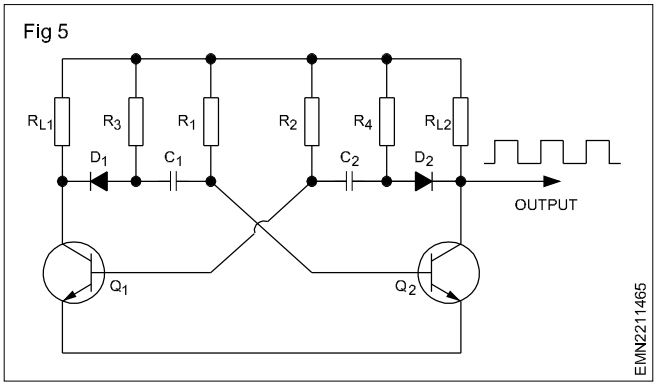
Hence, the multivibrator produces a frequency,f, or more aptly known as *Pulse Repetition Frequency(PRF)* of square wave(because $t_1 = t_2$) given by,

$$\text{PRF or } f = \frac{1}{T} = \frac{1}{3.24 \times 10^{-3}} = 309 \text{ Hz}$$

When the values of R_1, R_2 and C_1, C_2 are not equal, the off-time of the two transistors will be different. Hence the output wave-form will be non-symmetrical or will not be a square wave form.

The multivibrator circuit shown in Fig 4 is known as a **free running** multi-vibrator. This mean, the multi-vibrator oscillates by itself without the need for any external signal to change the states. This free running multi-vibrator is also known as **Astable multi-vibrator**, because the amplifiers used in the circuit is not stable in either state(ON or OFF).

As can be seen in Fig 4, the square wave output of the astable multi-vibrator is having rounded edges. Such round edges are not suitable in certain critical digital applications.These rounded edges can be eliminated(made vertical) by adding two diodes and two



resistors as shown in Fig 5.

The astable multi-vibrators shown in Fig 4 and Fig 5 are referred to as the collector-coupled multi-vibrators.

In addition to astable multi-vibrators which gives repetitive pulse wave form output, there are other types of multi-vibrators which are classified depending upon the manner in which the two stages of the multi-vibrator interchange their ON and OFF states. They are:

– Mono-stable multivibrator - having one stable state.

– Bistable multivibrator - having two stable states.

MONO-STABLE Multivibrators

Fig 6 shows a typical mono-stable multi-vibrator also known as **mono-shot** or **one-shot**.

A mono-shot has one stable state with one transistor conducting and the other off. This state can be changed only temporarily by giving an input pulse generally known as **trigger** pulse to the transistor which is off. But this changed state returns back to its original stable state after a period decided by the values of R and C.

Fig 6

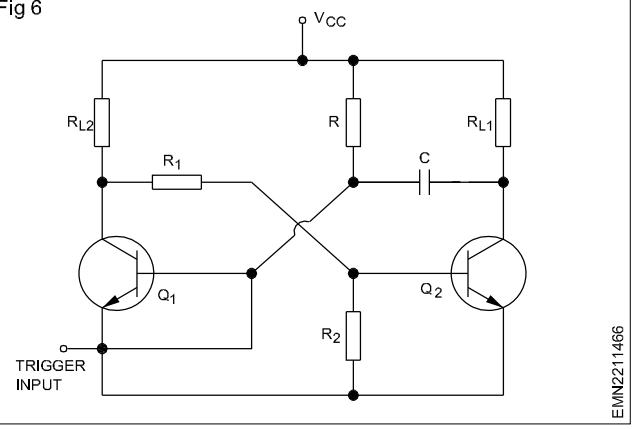


Fig 7 shows a practical mono-stable multi-vibrator with trigger input. Fig 7 also shows the wave-forms at different points of the circuit.

The period t for which Q_2 is kept off temporarily is given by,

$$t = 0.69\ RC.$$

Mono-stable multi-vibrators are extensively used as timers in electronic timing control circuits.

BISTABLE Multivibrators

An astable multi-vibrator automatically switches from one state to other (ON-to-OFF or OFF-to-ON...). Whereas, a bistable multi-vibrator will change the state(ON to OFF or OFF to ON) when triggered and remain in the new state (ON or OFF). This means, a bistable multi-vibrator has two stable states. Fig 9 shows a typical bistable multi-vibrator circuit.

The circuit at Fig 9 is completely symmetrical. The potential dividers R_1, R_2 and R_3, R_4 form identical bias network at the base of transistors. Each transistor is biased from the collector of the other transistor. Due to the slightest

Fig 7

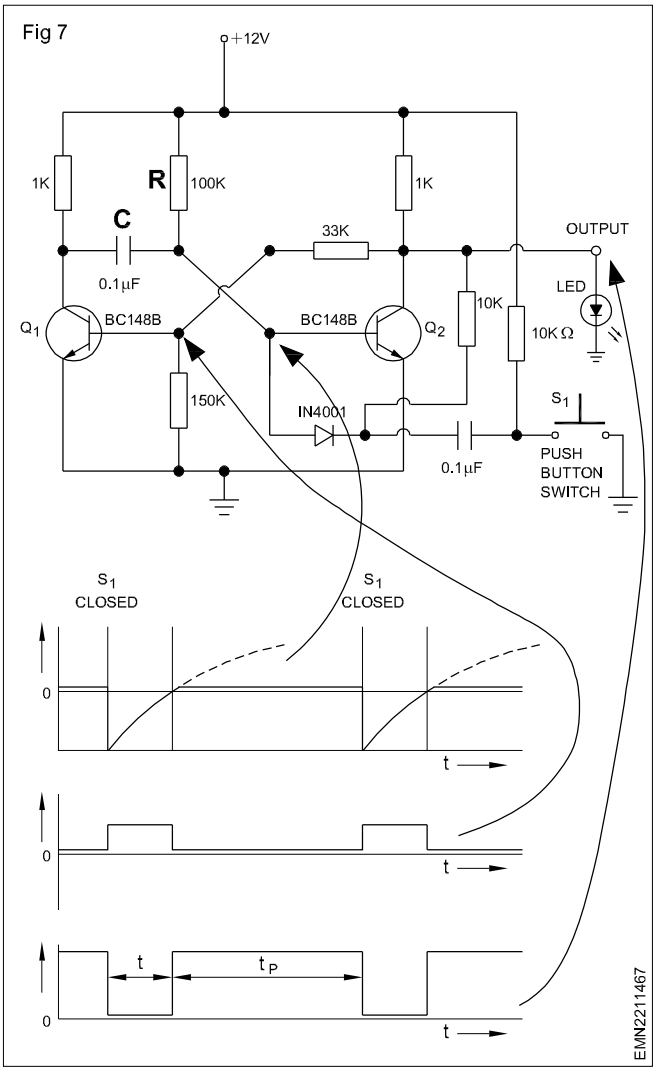
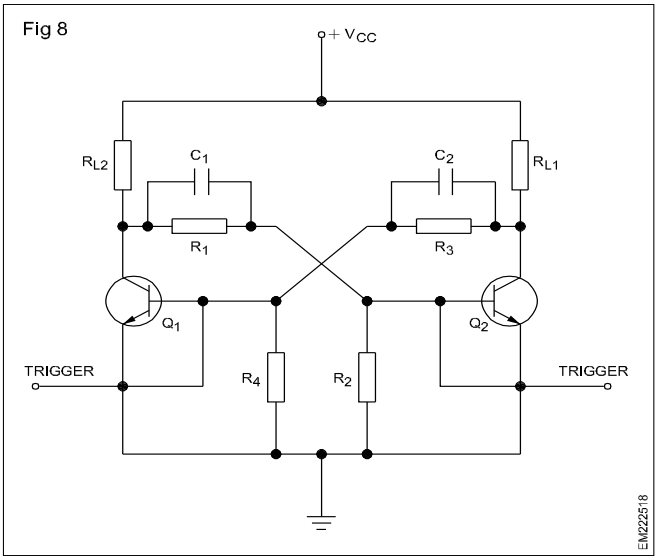


Fig 8

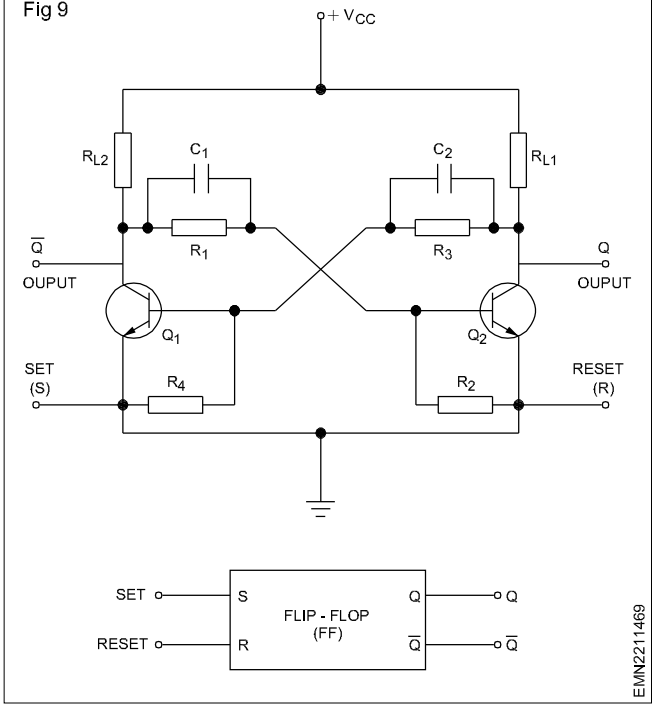


difference in parameters of the transistor, when the circuit is switched ON, any one of the two transistors will turn-ON, and the other remain in OFF condition.

In the circuit at Fig 9, the two identical CE amplifier stages are so connected that the output of one is fed to the input of the other, through resistors R_1, R_3 and shunted by capacitors C_1, C_2. The purpose of the capacitor is nothing but to speed up the switching characteristic of the circuit

to get distortion-less output wave-form. Capacitors C_1 & C_2 are also known as **commutating capacitors**.

Fig 9

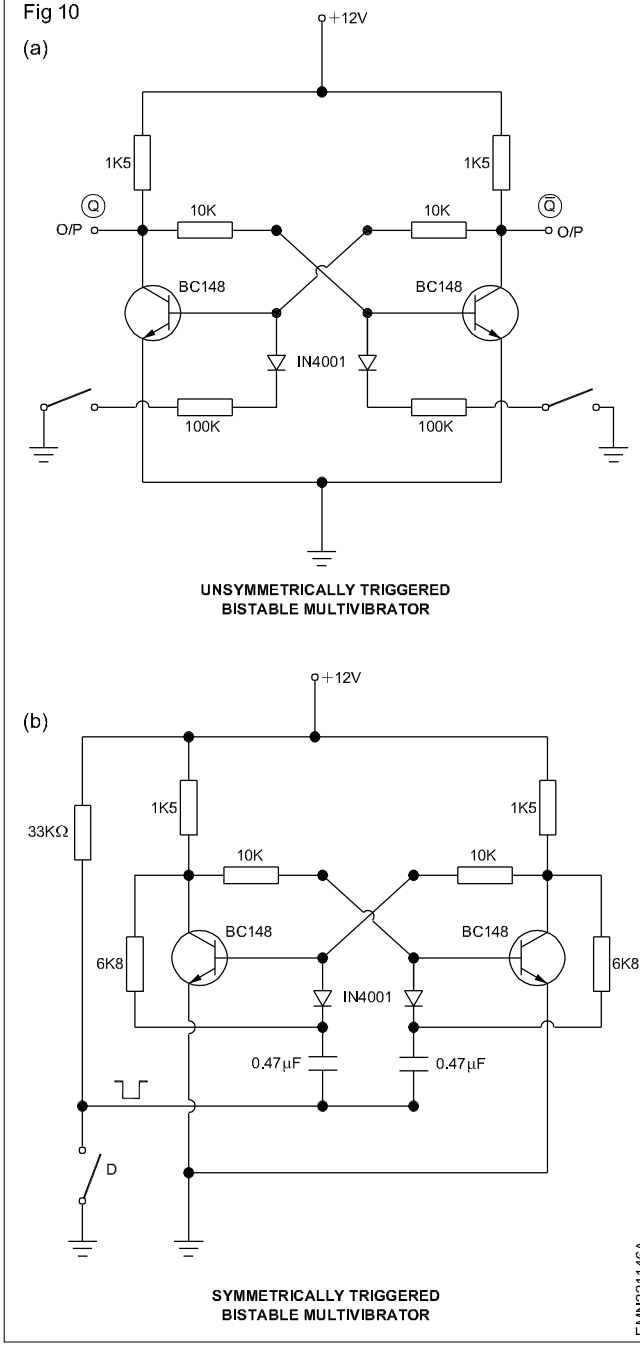


A bistable multi-vibrator is also known as a **flip-flop**. The output terminals are generally identified as Q & Q(Q-bar) as shown in Fig 10.

When Q is in high state (also known as **Logic-1** state in digital electronics), Q (Q-bar) will be in low state (also known as **Logic-0** state), and vice versa. This circuit is known as a flip-flop circuit because, if one output flips(high/logic-1) the other output automatically flops(low/logic-0). A flip-flop can be switched from one state to the other by applying a suitable triggering input. Flip-flops are used as a basic **memory cell** in digital computers for storing information. Flip-flops are used in various forms in almost all digital system as counters, frequency dividers and so on.

Practical bistable multi-vibrators with unsymmetrical and symmetrical triggering arrangement are shown in Fig 10a and 10b.

Fig 10



Schmitt Trigger

Objectives: At the end of this lesson you shall be able to
- **explain the circuit description of schmitt trigger**
- **state the meaning of UTP & LTP.**

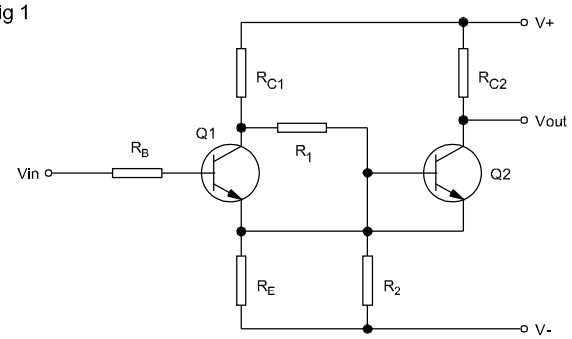
Schmitt trigger

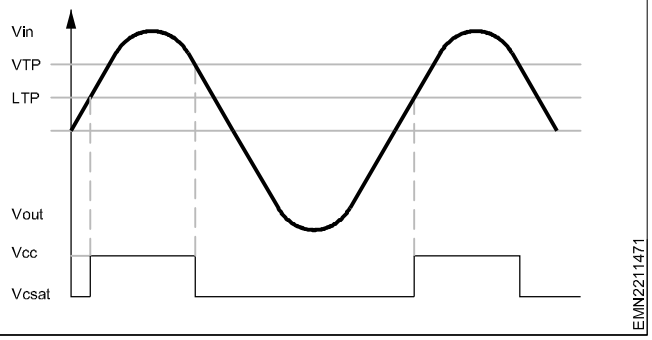
The following circuit shows the Schmitt trigger implemented by two emitter -coupled transistor stages.

Circuit Description

Schmitt trigger is a type of comparator. It measures the input to see if it is above or below a certain threshold. The threshold varies to make it less likely that the output will switch rapidly back and forth due to a noisy input near the threshold.

Fig 1





Operation

Initial state

For NPN transistors as shown above, imagine the input voltage is below the emitter voltage (high threshold) so that Q_1 base - emitter junction is reverse biased and Q_1 does not conduct. Q_2 base voltage is determined by the voltage divider RC_1, R_1, R_2 so that Q_2 is conducting and the trigger output is in the low state. The two resistors RC_2 and R_E form another voltage divider that determines the high threshold. Neglecting VBE, the high threshold value is approximately.

$$V_{HT} = \frac{R_E}{R_E + R_{C2}} V_+$$

The output voltage is low but well above the ground.

Crossing up the upper threshold (UTP)

When the input voltage (Q_1) base voltage) rises slightly above the voltage across the emitter resistor R_E (the high threshold), Q_1 begin conducting. Its collector voltage goes down and Q_2 begins going cut-off, because the voltage divider now provides lower (Q_1 base voltage. The common emitter voltage follows this change and goes down thus making Q_1 conduct more. The current begins steering from the right leg of the circuit to the left one. This process continues until Q_1 becomes completely turned on (saturated) and Q_2 turned off. The trigger is transitioned to the high state and the output (Q_2 collector) voltage is close to V_+. Now, the two resistors RC_1 and RE form a voltage divider that determines the low threshold. Its value is approximately.

$$V_{LT} = \frac{R_E}{R_E + R_{C1}} V_+$$

Crossing down the low threshold (LTP)

With the trigger now in the high state, if the input voltage lowers enough (below the low threshold), Q_1 begins cutting - off. Its collector current reduces; as a result, the shared emitter voltage lowers slightly and Q_1 collector voltage rises significantly. R_1-R_2 voltage divider conveys this change to Q_2 base voltage and it begins conducting. The voltage across R_E rises, further reducing the Q_1 base-emitter potential in the same avalanche-like manner, and Q_1 ceases to conduct. Q_2 becomes completely turned - on (saturated) and the output voltage becomes low again.

Clipper Circuit

Objectives : At the end of this lesson you shall be able to
- **define clipper circuit**
- **list the types of clippers**
- **state the functions of positive clipper with circuit**
- **state the functions of negative clipper with circuit.**

Wave shapping circuit:

A wave shapping circuit is used to change the shape of the wave form from alternating current or direct current. A clipper circuit is used to prevent the wave form voltage from exceeding the predetermined voltage without affecting the remaining part of the wave form.

Clipping circuit is a wave-shaping circuit and is used to either remove or clip a portion of the applied wave in order to control the shape of the output waveform. The portion of the voltage or the cutoff voltage may be above or below or both specified level. One of the most basic clipping circuits is the half-wave rectifier. A half-wave rectifier clips either the negative half cycle or the positive half cycle of an alternating waveform and allows to pass only one half cycle.

Classifications of clippers

According to biasing, the clippers may be classified as

- Unbiased clippers and
- Biased clippers

According to configuration used the clippers may be

- Series diode clippers
- Parallel or shunt diode clippers
- A series combination of diode, resistor and reference supply.

According to level of clipping the clippers may be

- Positive clippers
- Negative clippers
- Biased clippers
- Combination clippers

The basic components required for a clipping circuit are- an ideal diode and a resistor. In order to fix the clipping level to the desired amount, a DC battery may also be included. When the diode is forward biased, it acts as a closed switch, and when it is reverse biased, it acts as an open switch. Different levels of clipping can be obtained by varying the amount of voltage of the battery and also interchanging the positions of the diode and resistor.

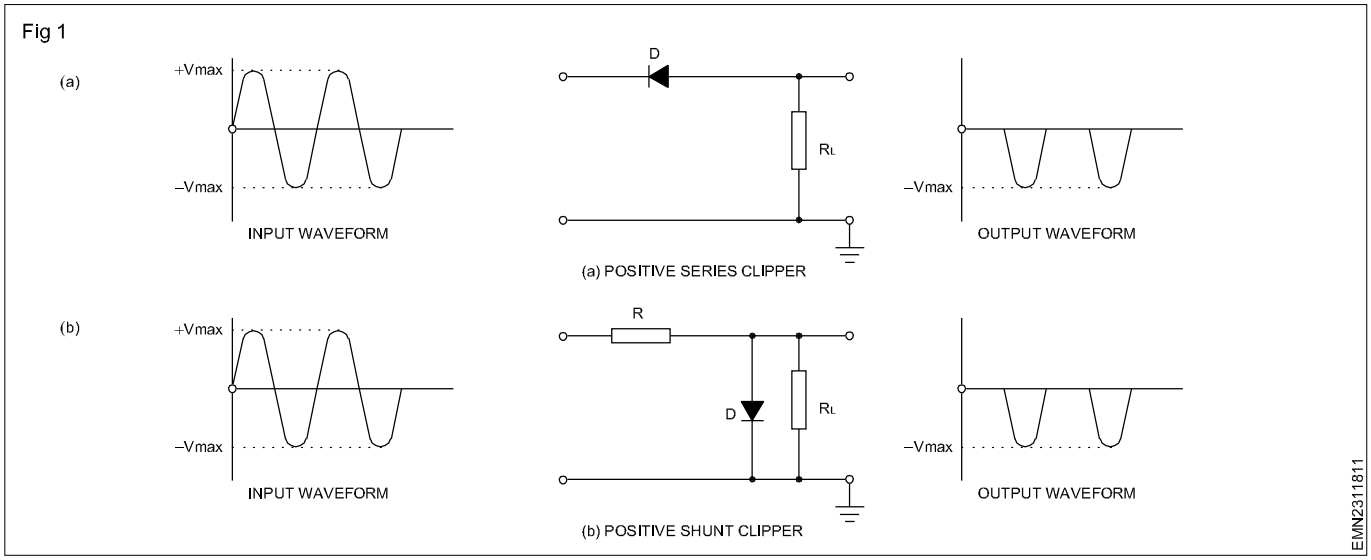
Depending on the features of the diode, the positive or negative region of the input signal is 'clipped' off and accordingly the diode clippers may be positive or negative clippers.

There are two general categories of clippers; series and parallel (or shunt). The series configuration is defined as one where diode is in series with the load, while the shunt clipper has the diode in a branch parallel to the load.

Positive Diode Clipper

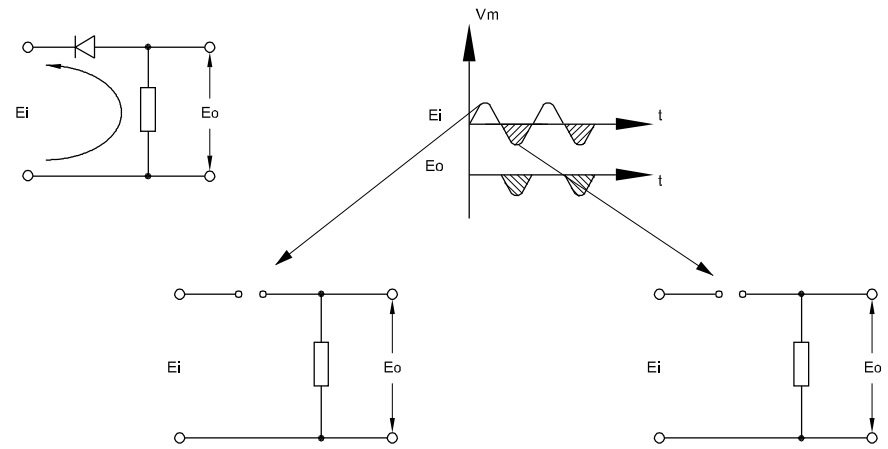
In a positive clipper, the positive half cycles of the input voltage will be removed. The circuit arrangements for a positive clipper are illustrated in the Fig. 1a and Fig. 1b given below.

Fig 1



As shown in fig. 1a, the diode is kept in series with the load. During the positive half cycle of the input waveform, the diode "D" is reverse biased, which maintains the output voltage at 0 volts. Thus causes the positive half cycle to be clipped off. During the negative half cycle of the input, the diode is forward biased and so the negative half cycle appears across the output. The above explanation will be self defined in the Fig. 2.

Fig 2



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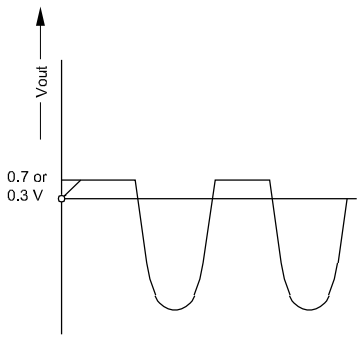
In Fig. 1(b) the diode is kept in parallel with the load. This is the diagram of a positive shunt clipper circuit. During the positive half cycle, the diode 'D' is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily. This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the positive half cycles in zero, as shown in the output waveform. During the negative half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently the entire input voltage appears across the diode or across the load resistance R_L if R is much smaller than R_L.

Actually the circuit behaves as a voltage divider with an output voltage of

$[R_L/R+R_L]\ V_{max}=-V_{max}$ when $R_L>>R$

In the above discussions, the diode is considered to be ideal one. In a practical diode, the breakdown voltage will exist (0.7V for silicon and 0.3V for Germanium). When this is taken into account, the output wave forms for positive clipper will be of the shape shown in the Fig3 below.

Fig 3



OUTPUT WAVEFORM FOR POSITIVE CLIPPER

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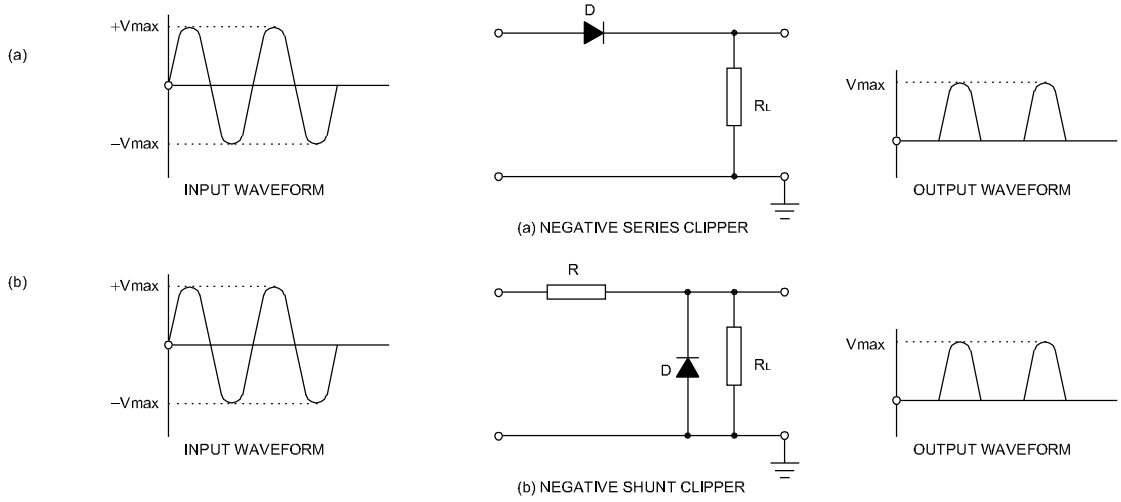
Negative diode clipper

The negative clipping circuit is almost same as the positive clipping circuit, with only one difference. If the diode in figures 1(a) and (b) is reconnected with reversed polarity, the circuits will become for a negative series and shunt clippers are shown in figures 4(a) and (b) as given below.

Fig 4



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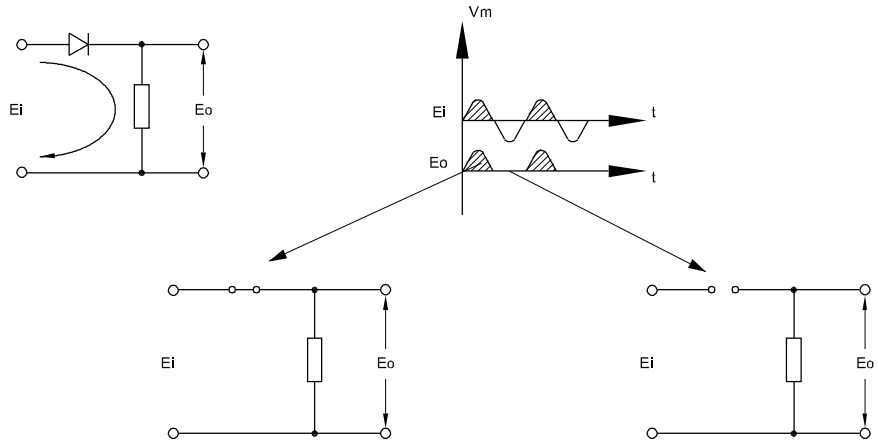
As shown in the figure 4a, the diode is kept in series with the load. During the negative half cycle of the input waveform, the diode 'D' is reverse biased, which maintains the output voltage at 0 volts. Thus causes the negative half cycle to be clipped off. During the positive half cycle of the input, the diode is forward biased and so the positive half cycle appears across the output. The above explanation will be self defined in the Fig5.

Fig 5



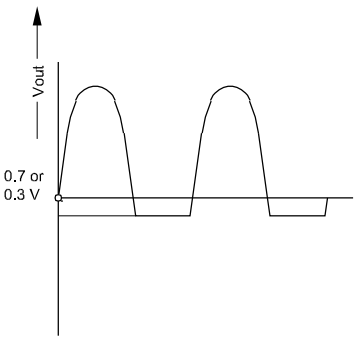
In Fig. 4(b) the diode is kept in parallel with the load. This is the diagram of a negative shunt clipper circuit. During the negative half cycle, the diode 'D' is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily. This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the negative half cycles is zero, as shown in the output waveform. During the positive half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently the entire input voltage appears across the diode or across the load resistance R_L if R is much smaller than R_L.

Actually the circuit behaves as a voltage divider with an output voltage of

$[R_L/R+R_L]\ V_{max}=V_{max}$ when $R_L>>R$

In the above discussions, the diode is considered to be ideal one. In a practical diode, the breakdown voltage will exist (0.7 for silicon and 0.3 V for Germanium). When this is taken into account, the output waveforms for negative clipper will be of the shape shown in the fig. 6 below.

Fig 6



OUTPUT WAVEFORM FOR NEGATIVE CLIPPER

Biased positive clipper and biased negative clipper

Objectives : At the end of this lesson you shall be able to

- **define biased negative and biased positive clippers**
- **state the functions of biased negative clipper with the circuit diagrams and waveforms**
- **state the functions of biased positive clipper with the circuit diagrams and waveforms.**

Biased negative clipper

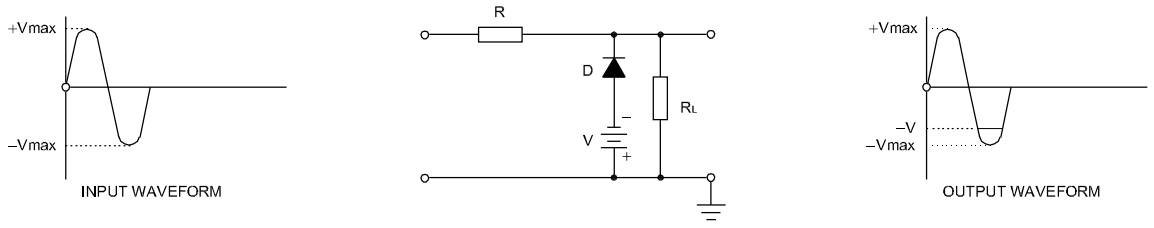
A biased clipper comes in handy when a small portion of positive or negative half cycles of the signal voltage is to be removed. When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper. The circuit diagram and waveform is shown in the figure 1.

In a biased negative clipper, when the input signal voltage is positive, the diode 'D' is reverse biased. This causes it to act as an open - switch. Thus the entire positive half cycle appears across the load, as illustrated by output waveform. When the input signal voltage is negative but does not exceed the battery voltage 'V', the diode 'D' remains reverse-biased and most of the input voltage appears across the output. When negative signal voltage becomes more than the battery voltage V the diode D is forward biased and conducts heavily. The output voltage is equal to '-V' and stays at '-V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, 'V'. Thus a biased negative clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.

Biased positive clipper

In a biased positive clipper, when the input signal voltage

Fig 1



BIASED NEGATIVE CLIPPER

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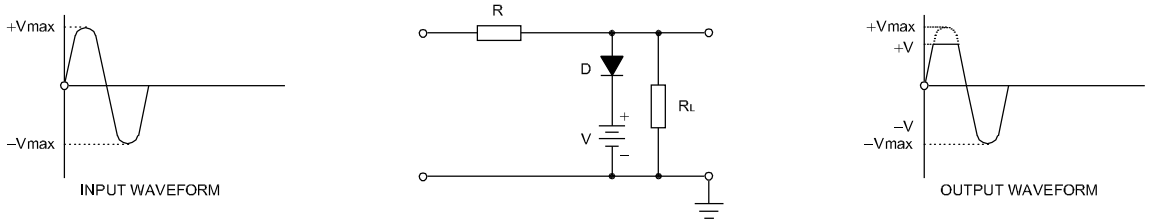
is negative, the diode 'D' is reverse biased. This causes it to act as an open - switch. Thus the entire negative half cycle appears across the load, as illustrated by output waveform . When the input signal voltage is positive but does not exceed the battery voltage 'V', the diode 'D' remains reverse-biased and most of the input voltage appears across the output. When positive signal voltage becomes more than the battery voltage V the diode D is forward biased and conducts heavily. The output voltage is equal to '-V' and stays at '-V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, 'V'. Thus a biased positive clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.

Fig 2



BIASED POSITIVE CLIPPER

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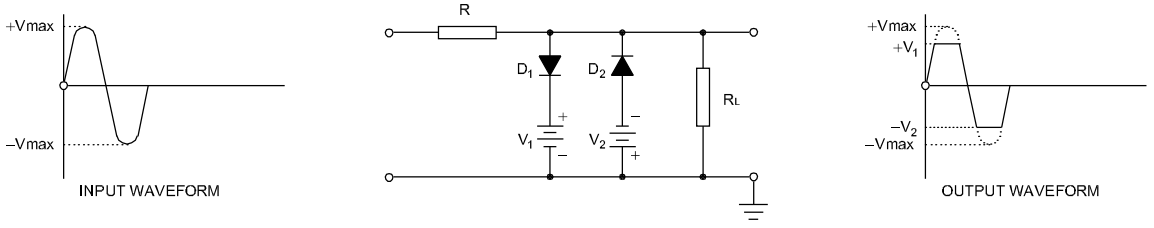
Combination clipper

Objectives : At the end of this lesson you shall be able to

- **define combination / dual clipper**
- **state the functions of combination clipper**
- **list the applications of clipper circuits.**

When a portion of both positive and negative of each half cycle of the input voltage is to be clipped (or removed), combination clipper is employed. The circuit for such a clipper is given in the Figure1.

Fig 1



COMBINATION CLIPPER

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The action of the circuit is summarized below. For positive input voltage signal when input voltage exceeds battery voltage '+V_1' diode D_1 conducts heavily while diode 'D_2' is reversed biased and so voltage '+V_1'. On the other hand for the negative input voltage signal, the diode 'D_1' remains reverse biased and diode 'D_2' conducts heavily only when input voltage exceeds battery voltage 'V_2' in magnitude. Thus during the negative half cycle the output stays at '-V_2' so long as the input signal voltage is greater than '-V_2'.

Applications

Clippers circuit has great applications in radars, digital computers and other electronic systems for removing unwanted portions of the input signal voltages above or below a specified level. Another application is in radio-receivers for communication circuits where noise pulses that rise well above the signal amplitude are clipped down to the desired level. Clipping circuits are also referred to as voltage limiters, amplitude selectors, or slicers.

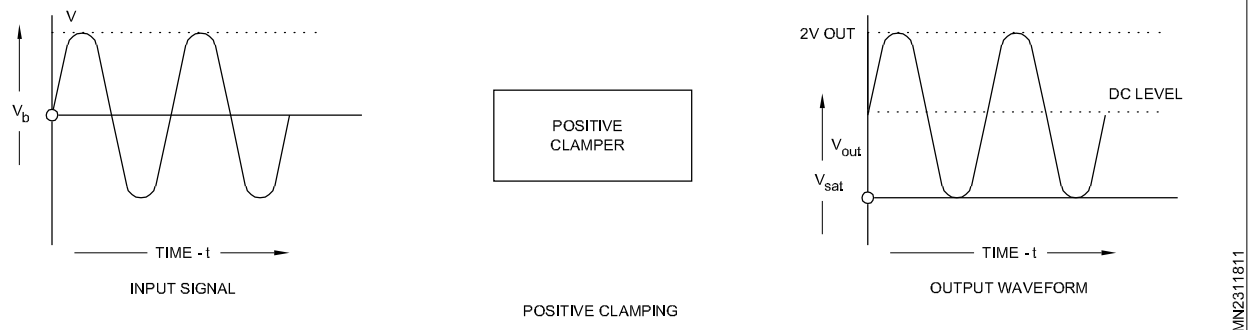
Clamper circuits

Objectives : At the end of this lesson you shall be able to
- **define clamper circuit**
- **define positive clamper**
- **define negative clamper**
- **explain the working principle of positive clamper**
- **explain the workig principle of negative clamper**
- **state the application of clamper circuit.**

A clamping circuit is used to place either the positive or negative peak of a signal at a desired level. The dc component is simply added or subtracted to/from the input signal. The clamper is also referred to as an IC restorer and ac signal level shifter.

A clamper circuit adds the positive or negative dc component to the input signal so as to push it either on the positive side, as illustrated in figure 1 or on the negative side, as illustrated in figure 2.

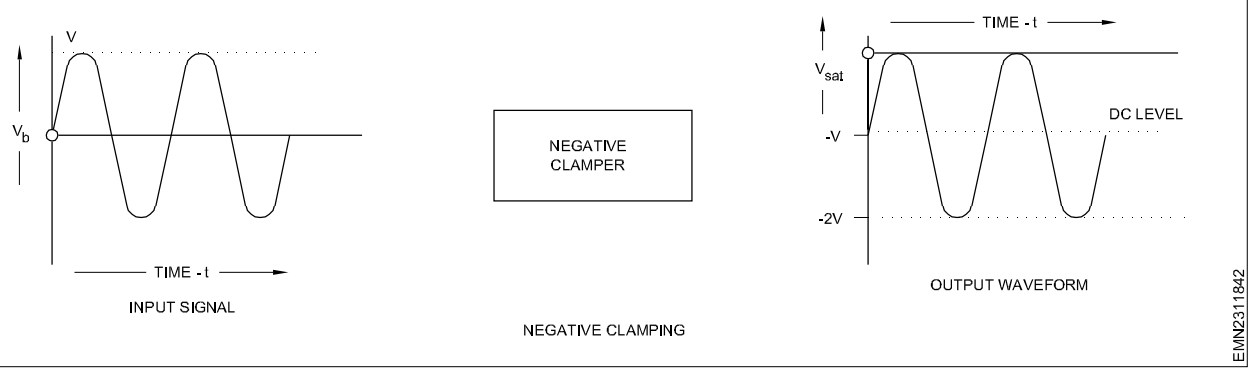
Fig 1



The circuit will be called a positive clamper , when the signal is pushed upward by the circuit. When the signal moves upward, as shown in figure (1), the negative peak of the signal coincides with the zero level.

The circuit will be called a negative clamper, when the signal is pushed downward by the circuit. When the signal is pushed on the negative side, as shown in figure (2), the positive peak of the input signal coincides with the zero level.

Fig 2



Application

In some cases, like a TV receiver, when the signal passes through the capacitive coupling network, it loses its dc component. This when the clamper circuit is used so as to re-establish the dc component into the signal input. Though the dc component that is lost in transmission is not the same as that introduced through a clamping circuit, the necessity to establish the extremity of the positive or negative signal excursion at some reference level is important. They also find applications in storage counters, analog frequency meter, capacitance meter, divider and stair-case waveform generator.

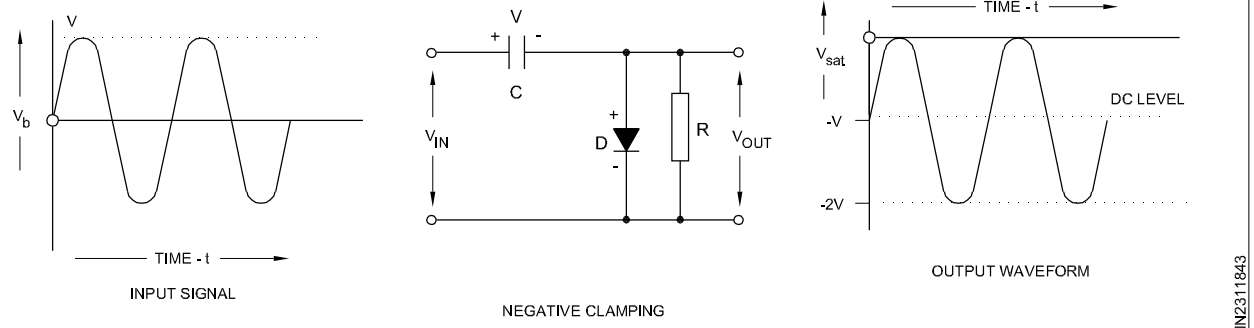
For a clamping circuit at least three components - a diode, a capacitor and a resistor are required. Sometimes an independent dc supply is also required to cause an additional shift. The important points regarding clamping circuits are:

- The shape of the waveform will be the same, but its level is shifted either upward or downward,
- There will be no change in the peak-to-peak or rms value of the waveform due to the clamping circuit. Thus, the input waveform and output waveform will have the same peak-to-peak value that is, $2V_{max}$. This

is shown in the figure above. It must also be noted that same readings will be obtained in the ac voltmeter for the input voltage and the clamped output voltage.

- There will be a change in the peak and average values of the waveform. In the figure shown above, the input waveform has a peak value of V_{max} and average value over a complete cycle is zero. The clamped output varies from 2 V_{max} and 0 (or 0 and -2V_{max}). Thus ths peak value of the clamped output is 2Vmax and average value is V_{max}.
- The values of the resistor R and capacitor C affect the waveform.
- The values for the resistor R and capacitor C should be

Fig 3



determined from the time constant equation of the circuit, t = RC. The values must be large enough to make sure that the voltage across the capacitor C does not change significantly during the time interval the diode is non-conducting. In a good clamper circuit, the circuit time constant t = RC should be at least ten times the time period of the input signal voltage.

Negative clamper

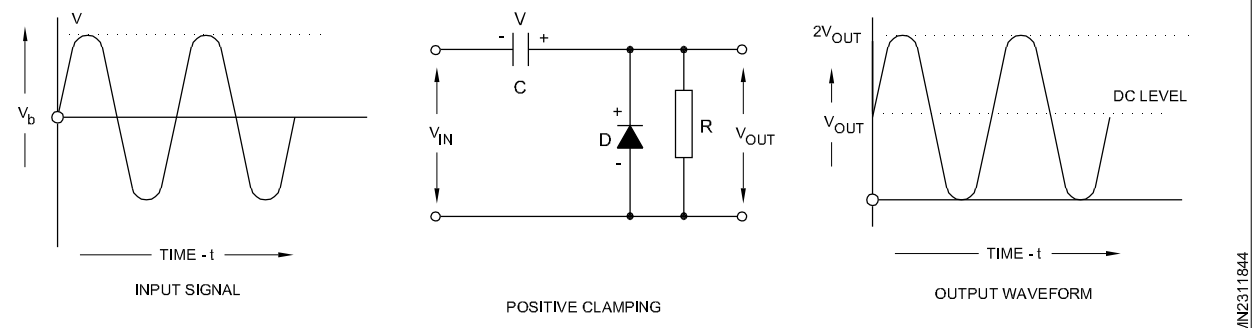
Consider a negative clamping circuit, a circuit that shifts the original signal in a vertical downward direction, as shown in the figure 3. The diode D will be forward biased and the capacitor C is charged with the polarity shown in Fig. 3, the output voltage will be equal to 0V. The capcitor is charged to V. During the negatice half cycle, the diode becomes reverse - biased and acts as an open - circuit. Thus, there will be no effect on the capacitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input voltage and the capacitor voltage and is equal to -V -V or -2V). The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to 2V.

Positive clamper

The fig 4 shown can be modified into a positive clamping circuit by reconnecting the diode with reversed polarity. The positive clamping circuit moves the original signal in a vertical upward direction. A positive clamping circuit is shown in the Fig 4 below.

It contains a diode D and a capacitor C as are contained in a negative clamper. The only difference in the circuit is

Fig 4



that the polarity of the diode is reversed. The remaining explanation regarding the working of the circuit is the same as it is explained for the negative clamper.

Consider a positive clamping circuit, a circuit that shifts the original signal in a vertical upward direction, as shown in the Fig 4. During the negative half cycle of input the diode D will be forward biased and the capacitor C is charged with the polarity shown in Fig.4, the output voltage will be equal to 0V. The capacitor is charged to V. During the positive half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus, there will be no effect on the capcitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the positive portion of the input waveform. Thus during positive input, the output voltage will be the sum of the input voltage and the capacitor voltag and is equal

to V+V or (2V). The value of the peak-peak output will be the difference of the negative and positive peak voltage levels is equal to 2V.

Zener diode clipping circuits

The use of a bias voltage means that the amount of the voltage waveform that is clipped off can be accuratelt controlled. But one of the main disadvantages of using voltage biased diode clipping circuits, is that they need an additional emf battery source whiche may not be a problem.

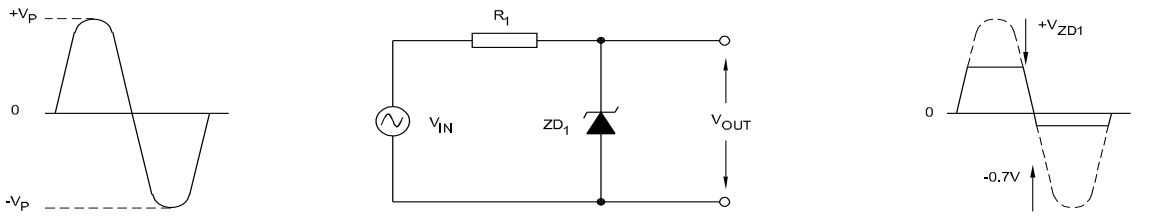
One easy way of creating biased diode clipping circuits without the need for an additional emf supply is to use Zener Diodes.

As we know, the zener diode is a another type of diode that has been breakdown region and as such as can be used voltage regulations or zener diode clipping applications. In the forward region, the zener acts just like an ordinary silicon diode with a forward voltage drop of 0.7V (700mV). When conducting, the same as above.

However, in the reverse bias region, the voltage is blocked until the zener diodes breakdown voltage is reached. At this point, the reverse current through the zener increases sharply but the zener voltage,$V_z$across the device remains constant even if the zener current, I_z varies.

Then we can put this zener action to good effect by using them for clipping a waveform as shown 5.

Fig 5



ZENER DIODE CLIPPING

EMN2311845

Zener Diode Clipping

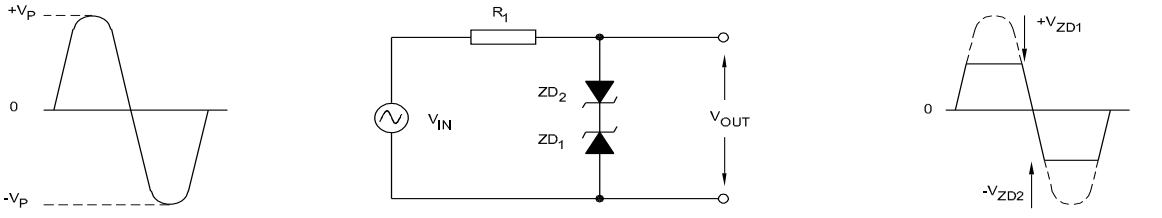
The zener diode is acting like a biased diode clipping circuit with the bias voltage being equal to the zener breakdown voltage. In this circuit during the positive half of the waveform the zener diode is reverse biased so the wavefrom is clipped at the zener voltage, $V_{ZD1.}$ During the negative half cycle the zener acts like a normal diode with its usual 0.7V junction value.

WE can develop this idea further by using the zener diodes reverse voltage characteristics to clip both halves of a wave from using serie connected back to back zener diodes in Fig 6.

The output waveform from fulll zener diode clipping circuits resembles that of the previous voltage biased diode clipping circuit. the output waveform will be clipped at the zener voltage plus the 0.7V forward volt drop of the other diode. So for exmple, the positive half cycle will be clipped at the sum of zener diode,ZD_1 plus 0.7 ZD_2 and vice vers a for the negative half cycle.

Zener diodes are manufactured with wide range of voltages and can be use to give different voltage references on each half cycle, the same as above. Zener diode are available with zener breakdown voltages, Vz ranging from 2.4 to 33 volts, with a typical tolerance of 1 or 5%.Note that once conducting in the reverse breakdown region, full current will flow through the zener diode so a suitable current limiting resistor, R1 must be chosen.

Fig 6



FULL-WAVE ZENER DIODE CLIPPING

EMN2311846

Applications

As well as being used as rectifiers, diodes can alsobe used to clip the top, or bottom, or both of a waveform at a particular dc level and pass it to the output without distortion. In or examples above we have assumed that the waveform is sinusoidal but in the theory any shaped input waveform can be used.

Diode clipping circuits are used to eliminate amplitude noise or voltage spikes, voltage regulation or to produce new waveforms from an existing signal such as squaring off the peaks of a sinusoidal waveform to obtain a rectangular waveform as seen above.

The most common application of as diode clipping is as a fly wheel or free wheeling diode connected in parallel across an inductive load to protect the switching transistor form revers voltage transients.

Field Effect Transistors

Objectives: At the end of this lesson you shall be able to
- **identify various power electronic component**
- **construction of FET & JFET**
- **difference between FET & BJT**
- **difference between JFET & BJT**
- **Heat sink and its purposes**
- **FET amplifiers in measuring device applications.**

Identification & different power electronic components

A thristor is an improved diode. Besides anode (A) and cathode (K) it has another lead which is commonly described as a gate (G), as found on picture. The same way a diode does, a thyristor conducts current when the anode is positive compared to the cathode, but only if the voltage on the gate is positive and sufficient current is flowing into the gate to turn on the device.When a thyristor starts conducting current into the gate is of on importance and thyristor can only be switched off by removing the current between anode and cathode.If S1 is closed,the thyristor will not conduct, and the globe will not light. If S2 is closed for a very short time, the globe will illuminate.To turn off the globe S1 must be opened. Thyristors are marked in some circuits as SCR, which is an acronym for silicon controlled rectifier. A triac is very similar to thyristor, with the difference that can conduct in both directions. It has three electrodes called anode 1 (A1), anode 2 (A2), and gate (G). It is used for regulation of alternating current circuits. Devices such as hand drills or globes can be controlled with a triac. Thyristor and triacs are marked alphanumerically, KT430, for example. Low power thyristors and triacs are packed in same housings as transistors, but high power devices have completely different housing. Pin-outs of some common thyristors and triacs are shown a and b. Diacs or two-way diodes as they are often referred to, are used together with thyristors and triacs. Their main property is that their resistance is very large until voltage on their ends exceeds some predefined value. When the voltage is under this value,a diac respond as a large value resistor, and when votage rises it acts as a low value resistor.

Field effect transistors (FET)

The main difference between a bi polar transistors and a field effect transistor is that,

Bi - polar transistor is a current controlled device.

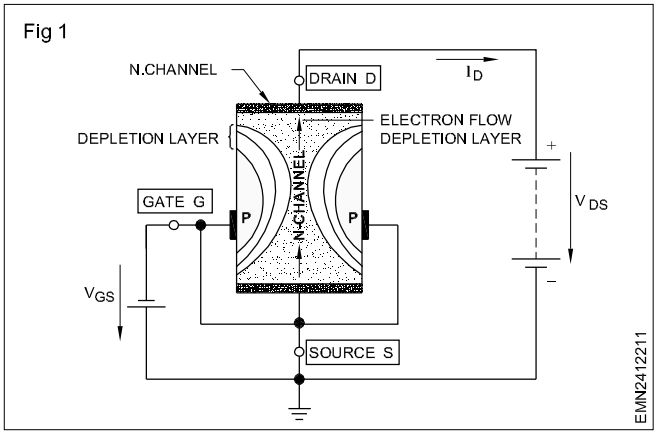
In simple terms, This means that the main current in a bipolar transistor (collector current) is controlled by the base current.

Filed effect transistor is a voltage controlled device.

This means that the voltage at the gate (similar to base of a bipolar transistor) controls the main current.

In a bi-polar transistor (NPN or PNP) the main current always flows through N-doped and P-doped semi conductor materials. whereas, in a field effect transistor the main current flows either only through the N-doped semiconductor or only through the p-doped semiconductor as shown in the Fig1.

Fig 1



If the main current flow is only through the N-doped material, then such a FET is referred as a N-channel or N type FET. The current through the N-doped material in the n-type FET is only by electrons.

If the main current flow is only through the p-doped material, then such a FET is referred as a p-channel or p-type FET. The current through the P-doped material in the p-type FET is only by holes.

Unlike in bipolar transistors in which the main current both by electrons and holes, in contrast in FET depending on the type of (P or N type) the main current in either by electrons or by holes and never both. For this reason FET are also known as uni polar transistors or uni polar device.

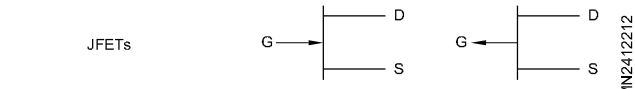
There are a wide variety of FETs. One of the fundamentals types called as junction field effect transistor (JFET) is discussed.

Junction Field effect Transistor(JFET)

It is a three terminal device and looks similar to a bi-polar transistor. The standard circuit symbols of N-channel and P-channel type FETs are shown in Fig 2.

The internal diagram of a N-channel FET is shown in Fig.3.

Fig 2

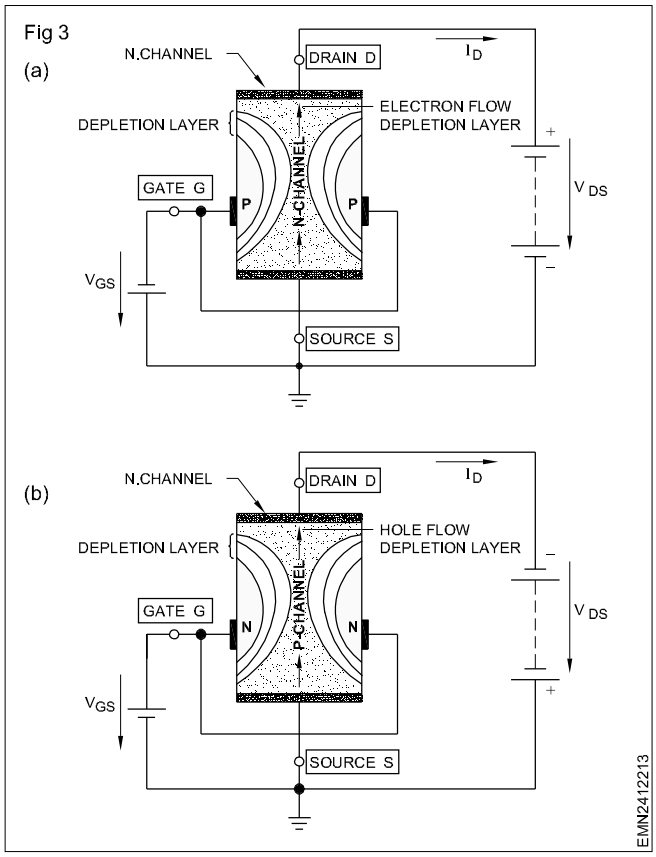


Construction

As shown in Fig 3a, a n-Channel JFET has a narrow bar of n-type. To this, two p-type junctions are diffused on opposite sides of its middle part Fig 3a. These diffused junctions form two P-N diodes or gates. The n-type semiconductor area between these junctions/gates is called channel. The diffused P regions on opposite sides of the channel are internally connected and a single lead is brought out which is called gate lead or terminal. Direct electrical connections are made at the two ends of the bar. One of which is called source terminal, S and the other drain terminal, D.

A p-channel FET will be very similar to the n-channel FET in construction except that it uses P-type bar and two N type junctions as shown in Fig 3b.

Fig 3



FET notation listed below are essential and worth memorizing,

1 Source terminal: It is the terminal through which majority carriers enter the bar(N or P bar depending upon the type of FET).

2 Drain terminal: It is the terminal through which majority carriers come out of the bar.

3 Gate terminal: These are two internally connected heavily doped regions which form two P-N junctions.

4 Channel: It is the space between the two gates through which majority carriers pass from source to drain when FET is working(on).

Working of FET

Similar to Biploar transistors, the working point of adjustment and stabilization are also required for FETs.

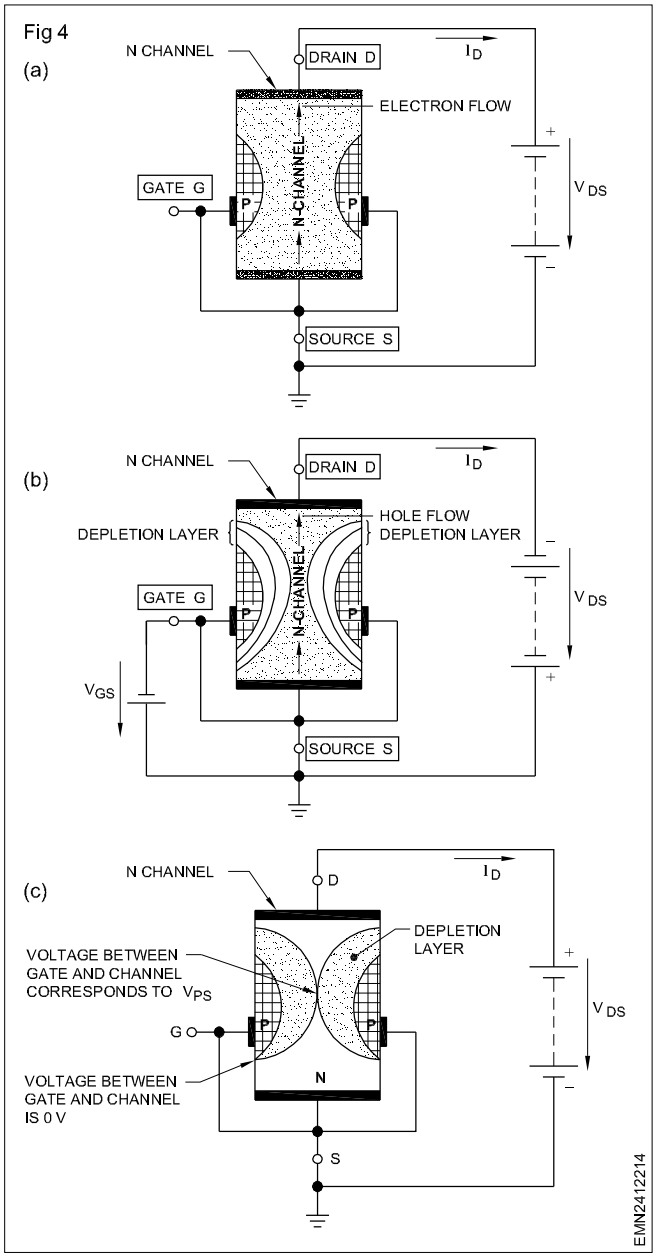
Biasing a JFET

– Gates are always reverse biased. Therefore the gate current I_G is practically zero.

– The source terminal is always connected to the end of the supply which provides the necessary charge carriers. For instance, in an N-channel JFET source terminal S is connected to the negative of the DC power supply. And, the posive of the DC power supply is connected to the drain terminal of the JFET.

Whereas in a P channel JFET, Source is connected to the positive end of the power supply and the drain is connected

Fig 4



to the negative end of the power supply.

Let us now consider an N channel JFET, the drain is made positive with respect to source by voltage V_{DS} as shown in Fig 4a. When gate to source voltage V_{GS} is zero, there is no control voltage and maximum electron current flows from source(S) - through the channel - to the drain(D). This electron current from source to drain is referred to as Drain current, I_D.

When gate is reverse biased with a negative voltage(V_{GS} negative) as shown in Fig 4b, the static field established at the gate causes depletion region to occur in the channel as shown in Fig 4b.

This depletion region decreases the width of the channel causing the drain current to decrease.

If V_{GS} is made more and more negative, the channel width decreases further resulting in further decrease in drain current. When the negative gate voltage is sufficiently high, the two depletion layers meet and block the channelcutting off the flow of drain current as shown in Fig 4c. This voltage at which this effect occurs is referred to as the Pinch off voltage, V_P.

Thus, by varying the reverse bias voltage between gate and source($-V_{GS}$), the drain current can be varied between maximum current (with $-V_{GS}=0$) and zero current(with $-V_{GS}$=pinch off voltage). So, JFET can be referred as a voltage controlled devices.

P channel JFET operates in the same way as explained above except that bias voltages are reversed and the majority carrier of channel are holes.

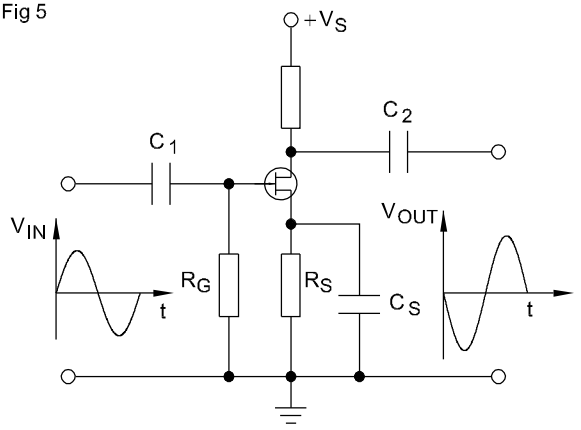
Important specifications of typical JFETs

	BF245B	BFW10
Polarity of the device (N-type/P-type)	Nj	Nj
Maximum drain-source voltage, V_{DS}	30 V	30 V
Maximum gate-source voltage, V_{GS}	30 V	30 V
Maximum drain current, I_D	25 mA	20 mA
Maximum forward gate current, I_G	10 mA	10 mA
Pinch-off Voltage (at I_D=0), V_P		8 V
Maximum power dissipation, P_{max}	300 mW	300mW
Package type	TO92	TO72
Pin Diagram (Refer 6605 data manual)	fig W141e	fig W158b

The term Nj in the specification indicates that it is a N-type junction FET.

As discussed earlier FETs also need a proper biasing arrangement for it to work. Like transistors, FETs can also be conneted in different cofiguration. Fig 5 gives a simple common source amplifier configuration.

Fig 5



COMMON - SOURCE CONFIGURATION

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Typical applications of JFET

One very important characteristic of JFET is its very high input impedence of the order of 10^9 ohms. This characteristic of FET has made it very popular at the input stage of a majority of electronic circuits.

As discrete components FETS are chiefly used in,

– DC voltage amplifiers

– AC voltage amplifiers(input stage amplifiers in HF and LF ranges)

– Constant current sources

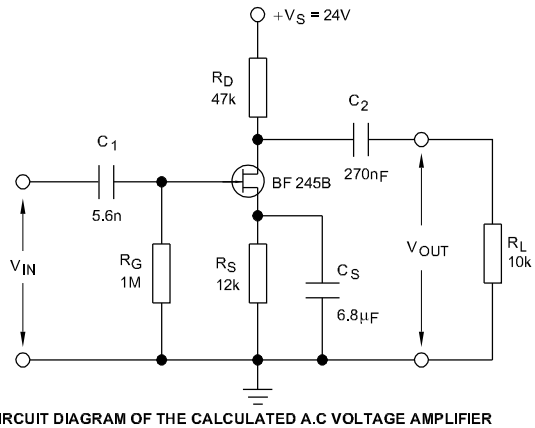
– Integrated circuits of both analog and especially in Digital technology.

One application of JFETs are illustrated below;

1 Fixed gain a.c voltage amplifier

In the circuit at Fig 6, the amplification is determined by the design. it can be varied within certain limits of the drain resistance and the source resistance are made variable. Potentiometers can be connected in series for this purpose.

Fig 6



CIRCUIT DIAGRAM OF THE CALCULATED A.C VOLTAGE AMPLIFIER

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Difference between JFET and BJJ

JFET	BJT
1 In a JFET there is only one type of carrier ie., holes in p type channel and electrons in n-type channel. For this reason it is called unipolar transistor. 2 As the input circuit of a JFET is reverse biase and therefore it as a input independence. 3 No current enters the gate & JFET. 4 JFET uses voltage on the gate terminal to the control current between drain and source. No junction in JFET so noise level is very small	1 In BJT both electrons and holes play role in conduction. It is called as bipolar transistors. 2 The input circuit of a BJT is forward based and hence has low input independence. 3 In typical BJT base current might be a few A. 4 BJT uses the current into its base to control a large current between collector and emitter.

FET Amplifiers in measuring device applications.

- Field effects transistors (FETs) are used in mixer circuits to control low inter modulations distortions.
- FETs are used in low frequency amplifiers due to its small coupling capacitors.
- It is a voltage controlled device due to this it is used in operational amplifier as voltage variable resistors.
- It is commonly used as input amplifiers in devices i.e. voltmeters, oscilloscopes, and other measuring devices, due to their high input impedance.
- It is also used in radio frequency amplifiers for FM devices.
- It is used for mixer operations of FM and TV receiver.
- It is used in large scale integration (LSI) and computer memories because of its small size.

Working principle, specifications and testing of SCR

Objectives: At the end of this lesson you shall be able to
- **explain the role of SCR in the field of industrial electronics**
- **explain the construction and working principle of SCR**
- **explain VI characteristics of SCRs**
- **list the specifications of SCRs**
- **explain the method of checking SCRs using JIG.**

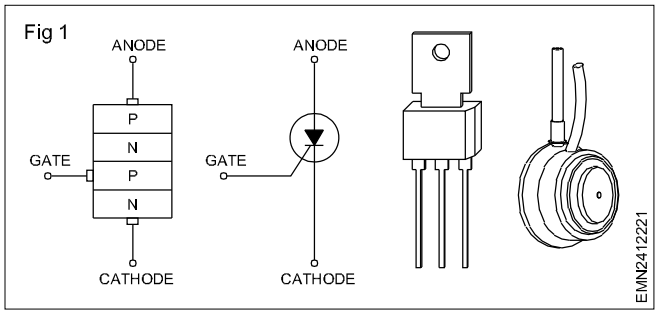
Silicon Controlled Rectifier(SCR)

Silicon Controlled Rectifier (SCR) is the first device of the thyristor family. The term thyristor is coined from the expression Thyratron-transistor. SCR is a semiconductor device. SCR does the function of controlled rectification. Unlike a rectifier diode, SCR has an additional terminal called the gate which controls the rectification(gated silicon rectifier).

The basic principle application of SCRs is to control the amount of power delivered to a load(motor, lamp, etc.,).

A rectifier diode will have one PN junction. SCRs on the other hand will have two PN junctions (P-N-P-N layers). Fig.1 shows the electrical symbol, basic construction and a typical SCR packages.

Fig 1



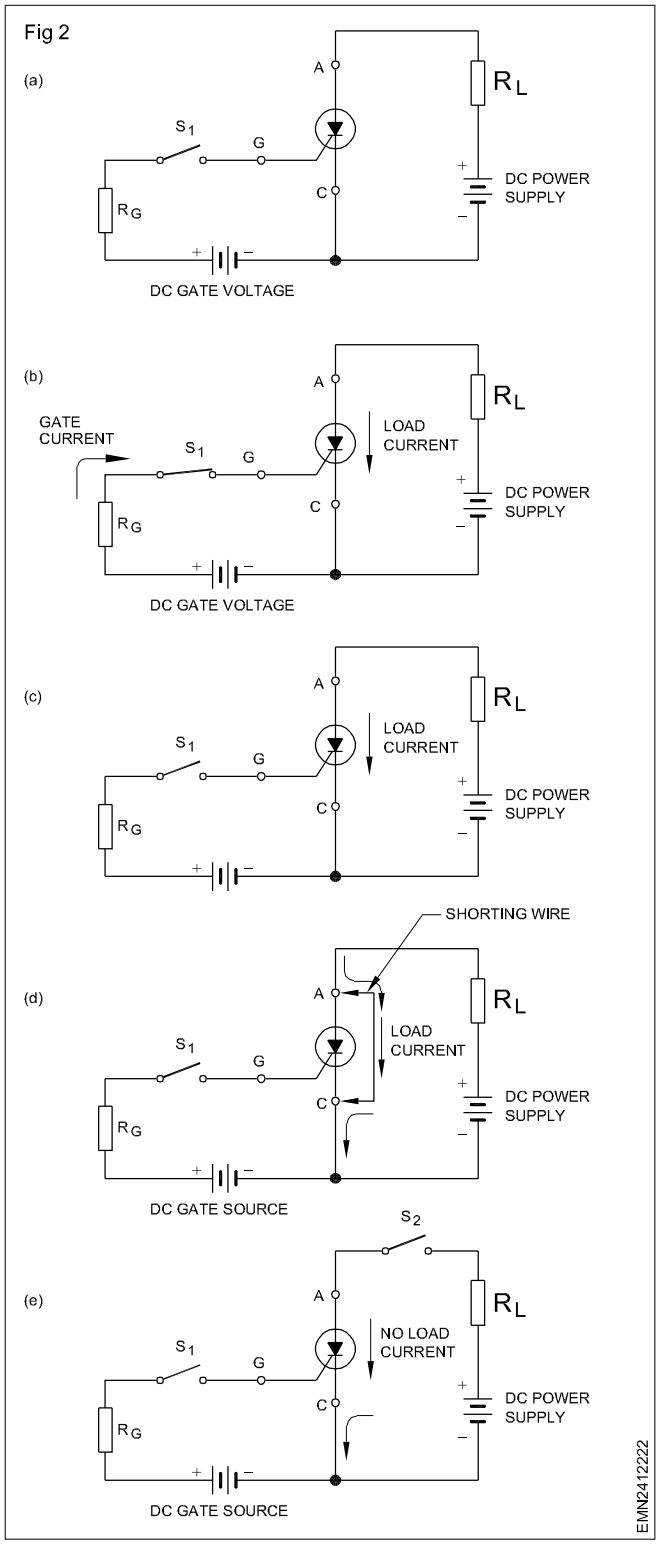
Basic operation of SCR

When a gate current is applied to the gate terminal, forward current conduction commences in the SCR(latched into conduction). When the gate current is removed, the forward current through the SCR **does not cut-off**. This means, once the SCR is latched into conduction, the gate loses control over the conduction. The current through the SCR can be turned off only by reducing the current through it(load current) below a critical value called the **Holding current.**

Fig 2 shows how an SCR can be gated into conduction or turned off.

In Fig 2a, with switched S1 open the SCR is in OFF state and no current is flowing through the load.

In Fig 2b, when S_1 is closed, a small gate current(around 1/1000 or less compared to load current) turns-ON (fires) the SCR. A heavy load current starts flowing through the SCR and load R_L.



In Fig 2c, when S_1 is opened, gate current becomes zero. This will have no effect on the current through the SCR and the heavy load current continues to flow through the SCR.

In Fig 2d, if a shorting wire is placed across the anode and the cathode terminals, the current though the SCR gets by-passed and all the current starts flowing through the shorted wire instead through the SCR. This means the current through the SCR is reduced below the rated holding current(minimum current required through SCR to keep it latched). This turns-OFF the SCR. Even when the shorting wire is removed the SCR remains to be in OFF state.

Fig 2e shows an alternative method of turning-OFF the SCR. In this instead of shorting the anode and cathode terminals of the SCR, the load current is cut-off by opening the Switch S_2. This reduced current through the SCR below the holding current and thus turns- OFF the SCR. Once the SCR is turned_OFF, the SCR does not turn-ON even if the switch S_2 is closed. To make the SCR fire again, with the switch S_2 closed, the gate current should be made to flow by closing the switch S_1.

Since the SCR does not conduct in the reverse direction, the anode of the SCR should always be positive with respect to cathode for conduction.

Important features of SCR,

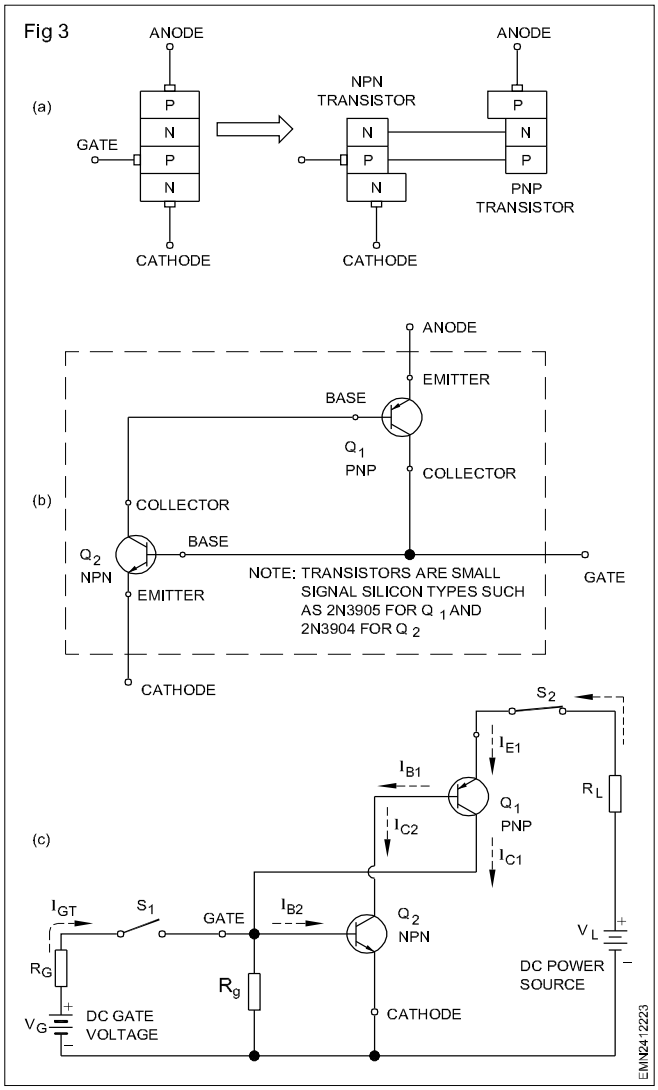
– A very small gate current will control the switching of a large load current.

Example: In 2N1597 SCR, a gate current of about 10mA will switch a load current of 1.6A(1:160).

– A gate current pulse of short duration(typically 100 msec) is sufficient to turn on the forward load current of SCR.

Understanding SCR as two interconnected transistors

For a clear understanding of how a SCR works, the four layer PNPN construction of SCR can be visualized as two



independent transistors interconnected as shown in Fig 3a and 3b.

In Fig 3c, in the initial state with S_1 open, both Q_1 and Q_2 are in cutoff and hence there is no current through the load R_L.

When S_1 is closed, the gate supply V_G causes a small base current(I_{B2}) to flow from the base of Q_2. This small base current turns on Q_2 and fairly a large collector current I_{C2} flows. At the same time, the emitter-base junction of Q_1 is forward biased and turns on Q_1. Since Q_1 collector current flows through the base of Q_2, this causes I_{C2} to increase. This increase in the base and collector currents of Q_1 and Q_2 becomes regenerative and thus takes Q_1 and Q_2 to saturation. At this time even if the base externally applied gate trigger pulse is removed, since the collector current of each transistor supplies the required base current to each other transistor, both the transistors remain to be in saturation. In this condition, the SCR acts almost like a short circuit/closed switch with a resistance as small as 0.1 ohms or less.

To bring the SCR to OFF state, since the externally applied gate has no further control of the SCR, the only way to turn-off is to reduce the collector currents of Q_1 and Q_2 to such a level that they will not sustain the regenerative action. This can be done by breaking the load current by switching off S_2 or by placing a short across the anode and cathode of the SCR. By shorting or by opening S_2, the current through the SCR(collector currents of the interconnect transistors) is reduced below the rated **holding current.**

Holding current is that minimum value of current required to sustain the regenerative action in the interconnected transistors in the absence of the gate trigger.

The resistor Rg connected across the base and emitter of Q_2 is to provide immunity from false gate triggering signals such as noise spikes etc. Recall that such a connection at the input circuit of a transistor reduces the input(gate) impedance of the transistor.

Typical VI Characteristics of SCR

SCR operation in first quadrant with DC supply

Typical Voltage-Current (VI) characteristics of a SCR is illustrated in Fig 4.

Considering that the SCR is operated with DC supply and the device is always forward biased(+ve to anode and -ve to cathode). The V-I characteristics of a typical SCR will be as shown in Fig 4. This is called as the first quadrant operation of the SCR.

When SCR is used with AC supply, then the VI characteristics in the third quadrant will also be discussed.

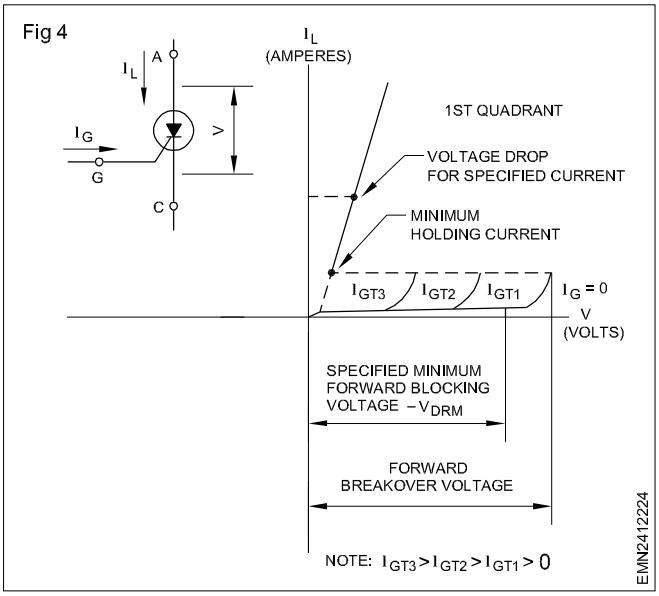
Abnormal Operation of SCR

With Gate current I_G=0,

– With a moderate Anode Cathode voltage, only a very small leakage current(can be neglected) flows through the SCR.

– If the anode cathode voltage is increased beyond a maximum forward blocking voltage(see fig 4), the SCR will break into forward condition and large current starts flowing through the SCR. This destroys the SCR breaking down the central PN junction. Therefore, the anode cathode voltage of SCR should always be less than the forward breaking voltage.

Fig 4



Break over voltage: It is that anode-cathode voltage at which the PN junctions of the SCR breaks down thus forcing the SCR into conduction.

Normal operation of SCR

With small gate trigger currents I_{G1} or I_{G2} or I_{G3}.....(Fig. 4)

– With a small gate trigger current say I_{G1}, the SCR need a lower anode cathode voltage to fire the SCR on and a large current flows through the SCR. The amount of current through the SCR is limited only by the external load connected.

– With a slightly larger gate trigger current I_{G2} (I_{G2}>I_{G1}), the SCR gets fired even at a lesser anode cathode voltage.

Thus, a lower anode-cathode voltage is required to set the SCR into conduction with higher values of gate trigger current and vice-versa.

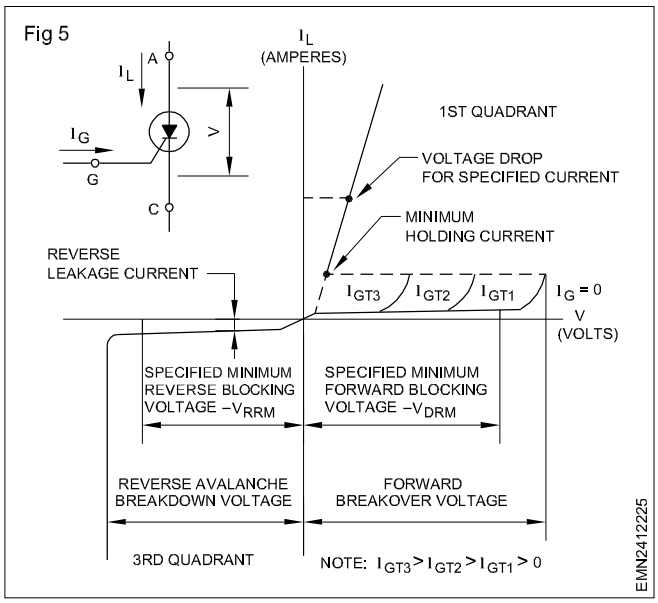
– Once the SCR is fired, it remains in conduction as long as the SCR current/load current is not allowed to drop below the "holding current value". As and when the SCR is required to stop conduction, the load current should be brought below the holding current value either by swithching-off the load circuit(load current becomes zero) or by reversing the applied voltage polarity to the anode-cathode or by other suitable means.

Fig. 5 illustrated the VI characteristics of SCR in first and third quadrant. The third quadrant operation basically illustrated the operation of the SCR when in reversed biased condition. The operation of the SCR in First and

Third quadrant occurs when the SCR is operated using AC supply.

SCR operation in third quadrant with DC supply

When the anode-cathode of SCR is reverse biased a small



reverse leakage current flows through the SCR. When the reverse bias voltage is increase slowly form zero to a higher value, beyond a particular voltage called the " Maximum Reverse blocking voltage", the PN junctions of the SCR will break down and thus SCR becomes a short and enters into conduction. This results in a large current through the SCR/ load as shown in fig 5 in the third quadrant. SCR should never be applied with a reverse voltage as high as this Maximum Reverse blocking voltage.

SCR operation with AC supply

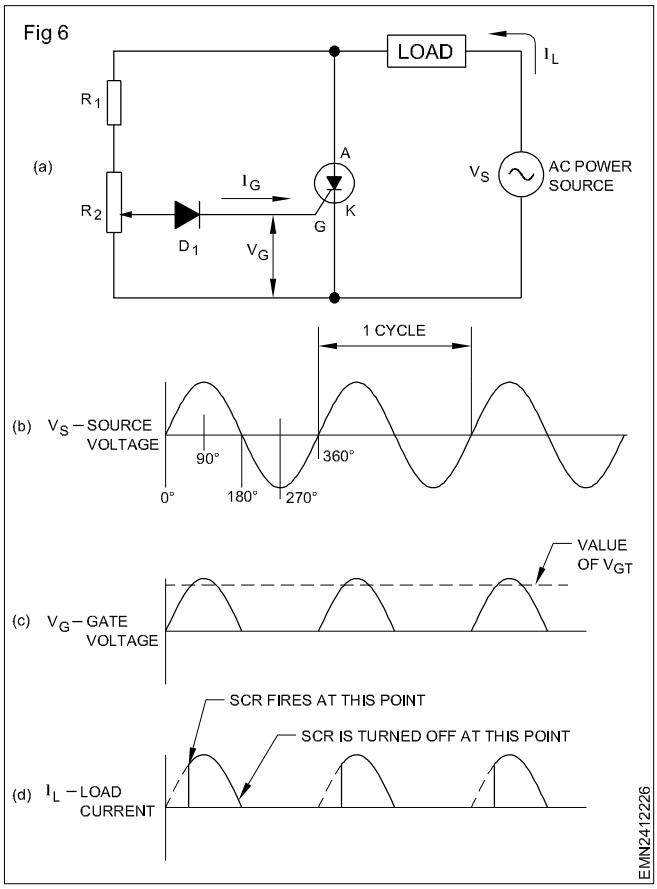
Operation of SCR with AC circuit is similar to SCR operation in the first and the third quadrant as discussed in above paragraphs. Fig 6 illustrates working of SCR in AC control circuits.

The SCR gate circuit consists of resistor R_1, potentiometer R_2 and silicon diode D_1. Resistors R_1 and R_2 act as a variable voltage divider. By adjusting the value of R_2 the gate current I_G can be suitably modified. Diode D_1 prevents negative voltage being applied to the gate when the AC supply is in the negative half cycle.

[X] During the +ve half cycle of the AC power source, as the positive half cycle voltage increases, the gate current I_G increases. When I_G reaches the trigger level, SCR fires and allows current I_L to flow through the load. From this point onwards the SCR impedance is low and current I_L continues to flow throughout the +ve half cycle even though the gate current reduces below the trigger value(recall: once SCR is fired it continues to conduct even if the gate trigger is decreased or removed).

[Y] At the end of the +ve half cycle of AC power source, the +ve voltage drops to zero and SCR ceases to conduct(recall: one method of turning off SCR is to reduce the current through the SCR to below the holding current. This can be done by either opening the load circuit or reducing the supply to zero). Thus the SCR remains in off state throughout the negative half cycle.

Cycle [X] and [Y] repeats and current through the load flows



in pulses as shown in Fig 6d.

Fig 6b,6c shows the voltage wave forms of source and gate voltage.

If the value of R_2 is varied, the point at which SCR triggers also varies changing the firing point shown in fig 6d. In the circuit shown in Fig 6a, the firing of SCR can be adjusted any where between almost 180 degrees(maximum) to 90 degrees(minimum).

This simple AC control circuit shown in Fig 6a using SCR can be used to control the current through the load during the +ve half cycle of AC. During the -ve half cycle the SCR remains turned off. Thus, SCR can be used as an excellent switching device in AC control circuits.

The circuit at Fig 6a is useful only in limited applications such as temperature control of soldering iron etc., More practical AC control circuits are discussed in further lessons.

SCR Specifications

For maximum performance, reliability and safety, each SCR should be operated within the ratings specified by the manufacturer. When you are designing a new circuit or replacing an SCR of an existing circuit, it is very essential to check the data of the SCR before using.

A typical SCR data sheet list many specifications. A few of these specifications considered as most important from the point of view of a technician are listed below;

V_{DRM}: This is referred to as the anode-cathode forward Break down voltage with no input gate current. Beyond this value, the SCR will break down into forward conduction. For typical SCRs, V_{DRM} ranges from about 30 Volts to 800 Volts.

V_{RRM}: This is referred to as the maximum anode-cathode reverse breakdown voltage. Beyond this value the SCR will break into reverse conduction. For typical SCRs, V_{RRM} also ranges from about 30 Volts to 800 Volts.

V_{GT}: This is the minimum positive gate voltage required to turn on the SCR. At temperature of 25°C typical values of V_{GT} is 0.7 to 0.8 volts. For higher temperatures of about 100 to 125°C, V_{GT} drops to approximately 0.2 volts.

I_{GT}: This is the minimum forward gate current required to turn on the SCR. Typically, low power SCRs require an I_{GT} of about 100 to 300 µA for turn-on. Medium and high power SCR needs about 5 to 150 mA for turn-on.

I_H: This is the minimum load current required to be maintained in the SCR to keep the SCR in on-state. Typical values of I_H ranges from about 6 mA for low power SCRs to 80 mA for high power SCRs.

I_T: This is the maximum allowable anode current that the SCR can withstand. This is defined by manufacturers in terms of rms forward current(I_{rms}) or average forward current (I_{avg}) for 180° of conduction. Typical values of I_{rms} for low and medium power SCRs range from about 1 to 30 Amperes.

V_{TM}: It is the maximum on state anode-cathode voltage drop across the SCR when it is conducting. Some manufacturers refer to this specification as V_F or V_{FM}. For most SCRs , V_{TM} is of the order of 1.6V.

t_{gt}: It is the time required for a specified gate current to turn on the SCR. Typical values lie in the range of 1 to 2 µSec.

t_q: It is the time required for a specified SCR to turn-off when the load circuit is made open. Typical values lie in the range of 15 to 35 µSec.

In addition to the above specifications, there are a few more specifications of SCR, some are of general nature to be considered while designing circuits using SCR and some are specific to certain SCR types. For further details refer specification sheets of SCR supplied by the manufacturers.

Specifications of a few SCRs

2N 5060

V_{RRM}	30V
V_{GT}	1.2V
I_{GT}	0.35A t_{gt}
I_H	t_q
I_T	0.8A
Package type:	TO 92

MCR 218-5

V_{DRM}	300V
V_{TM}	1.5(typ) to 1.8V(max)
V_{GT}	0.2V(min) - 2.5V(max)
I_{GT}	10mA(typ) to 25mA(max)
I_H	16mA(typ_ to 30mA(max)
$I_{T(rms)}$	8 Amps.
Package type :	TO 220

QUICK Check of SCRs

Quick check on SCRs can be carried out using a ohmmeter/ multimeter. Since SCRs are made of PNPN junction, resistance between junctions can be measured to conclude good working condition of the SCR. A good SCR shows following resistances between its terminal leads;

CHECK - 1

Between Anode - Cathode - Infinite resistance

[Irrespective of polarity]

Between Gate - Cathode

(i) Forward biased - Very low resistance (30 to 500 ohms)

(ii) Reverse biased - High resistance

Between Gate - Anode - Infinite resistance

[Irrespective of polarity]

CHECK - 2

– Set multimeter to low resistance range.

– Connect positive lead of multimeter to the anode and the negative lead to the cathode. Meter should show infinite resistance.

– Now, for moment, short anode and gate of SCR by a piece of wire. The meter should show low resistance and will continue to show low resistance even after the short between anode and gate is been removed.

It is difficult to check leaky SCRs using only a ohmmeter/multimeter.

Checking SCRs using a SCR checking JIG

A simple "SCR checking jig" is shown in Fig 7. In Fig 7, the SCR shown in dotted lines is the SCR to be checked. This could be any SCR that you want to check.

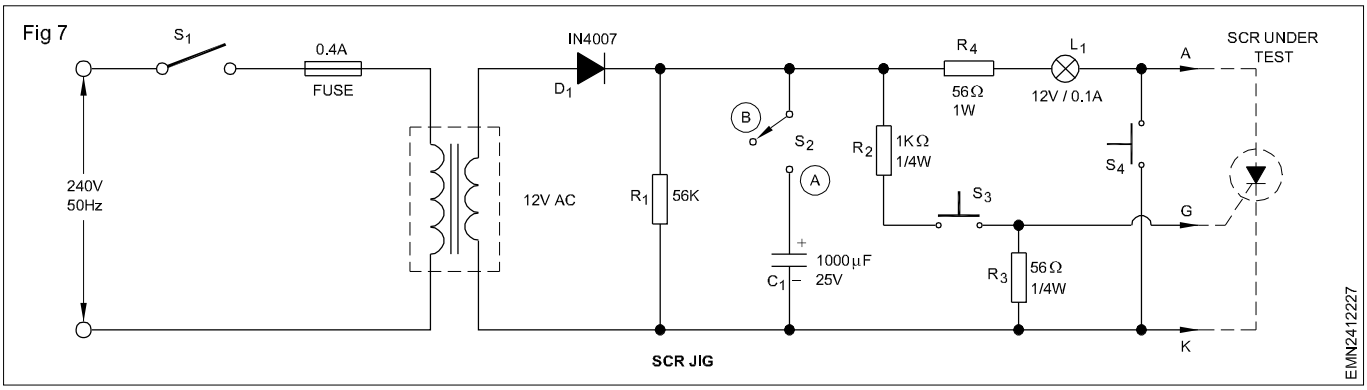
In Fig 7, the stepped down 12V AC is rectified by diode D_1 and filtered by capacitor C_1 when switch S_2 is at position A. The rectified and filtered DC is applied to the anode of SCR through lamp L_1 via a limiting resistor R_4. Resistor R_2, R_3 in series with a push button switch S_3 form a potential divider across DC. Voltage across R_3 is applied to the gate of SCR. This voltage is sufficient to turn on the SCR. Another push button Switch S_4 is connected directly across the Anode and Cathode of the SCR to be checked.

When a good SCR is placed in the test jig(in place of the SCR shown dotted) the circuit should function as given below;

1 When mains supply is on, and S_2 is at DC position, the lamp will start glowing as soon as the switch S_3 is pressed. Even on releasing S_3, the lamp should keep on glowing. Under this condittion, if switch S_4 is pressed once and released the SCR stops conducting and hence the lamp stops glowing.

2 If switch S_2 is put to AC position ie., to position B, lamp should glow only as long as switch S_3 is pressed. Switch position B corresponds to feeding AC from secondary side of transformer.

Instructor to discuss reasons for 1 & 2 above as an interactive discussion. Instructor should also discuss the outcome of above steps when a open or a shorted SCR is checked.



Solid State Relay

Objectives : At the end of this lesson you shall be able to
- **explain construction and working of solid state relay**
- **explain advantage and disadvantages over mechanical relay.**

Solid - state relay

A **solid-state relay (SSR)** is an electronic switching device that switches conduction states when a small external voltage is applied along its n-type and p-type junctions. SSRs consist of a sensor which responds to an appropriate input (control signal), a solid-state electronic switching device which switches power to the load circuitry, and a coupling mechanism to enable the control signal to activate this switch without mechanical parts. The relay may be used to switch either AC or DC to the load. It serves the same function as an electromechanical relay, but has no moving parts.

Solid-state relays are composed of semiconductor materials, including thyristors and transistors, and have current ratings that extend from a few microamps for low-power packages up to around a hundred amps for high-power packages. They have extremely fast switching speeds usually ranging between 1 to 100 nanoseconds and are not easily affected by contact wear. Solid-state relays have several shortcomings:

1. It gets easily damaged in comparison to electromechanical relays.

2. Limited switching arrangements (SPST switching); a need for finer tuning due to high "on" resistances.

Coupling

The control signal must be coupled to the controlled circuit in a way which provides galvanic isolation between the two circuits.

Many SSRs use optical coupling. The control voltage energizes an internal LED which illuminates and switches on aphoto-sensitive diode (photo-voltaic); the diode current turns on a back-to-back thyristor, SCR, or MOSFET to switch the load. The optical coupling allows the control circuit to be electrically isolated from the load.

Operation

A SSR based on a single MOSFET, or multiple MOSFETs in a paralleled array, can work well for DC loads.

MOSFETs have a built-in substrate diode that conducts in the reverse direction, so a single MOSFET cannot block current in both directions. For AC (bi-directional) operation two MOSFETs are arranged back-to-back with their source pins tied together. Their drain pins are connected to either side of the output. The substrate diodes are alternately reverse biased to block current when the relay is off. When the relay is on, the common source is always riding on the instantaneous signal level and both gates are biased positive relative to the source by the photo-diode.

It is common to provide access to the common source so that multiple MOSFETs can be wired in parallel if switching a DC load. Usually a network is provided to speed the turn-off of the MOSFET when the control input is removed.

One significant advantage of a solid-state SCR or TRIAC relay over an electromechanical device is its natural tendency to open the AC circuit only at a point of zero load current. Because SCR's and TRIAC's are thyristors, their inherent hysteresis maintains circuit continuity after

the LED is de-energized until the AC current falls below a threshold value (the holding current). In practical terms what this means is the circuit will never be interrupted in the middle of a sine wave peak. Such untimely interruptions in a circuit containing substantial inductance would normally produce large voltage spikes due to the sudden magnetic field collapse around the inductance. This will not happen in a circuit broken by an SCR or TRIAC. This feature is called zero-crossover switching.

SSRs are characterised by a number of parameters including the required activating input voltage, current, output voltage and current, whether it is AC or DC, voltage drop or resistance affecting output current, thermal resistance, and thermal and electrical parameters for safe operating area (e.g., derating according to thermal resistance when repeatedly switching large currents).

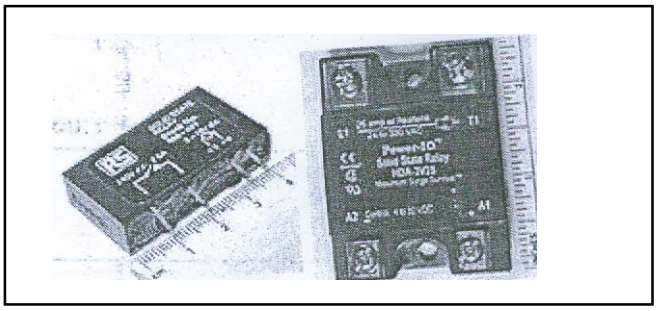
Advantages over mechanical relays

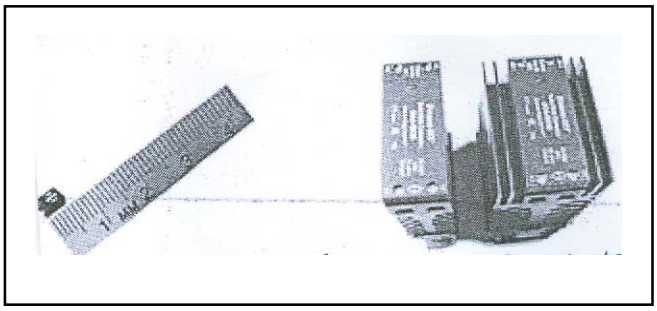
Most of the relative advantages of solid state and electromechanical relays are common to all solid-state as against electromechanical devices.

- Slimmer profile, allowing tighter packing.
- Totally silent operation
- SSRs are faster than electromechanical relays; their switching time is dependent on the time needed to power the LED on and off, of the order of microseconds to milliseconds
- Increased lifetime, even if it is activated many times, as there are no moving parts to wear and no contacts to pit or build up carbon
- Output resistance remains constant regardless of amount of use
- Clean, bounceless operation
- No sparking, allows it to be used in explosive environments, where it is critical that no spark is generated during switching
- Inherently smaller than a mechanical relay of similar specification (if desired may have the same "casing" form factor for interchangeability).
- Much less sensitive to storage and operating environment factors such as mechanical shock, vibration, humidity, and external magnetic fields.

Disadvantages

- Voltage/current characteristic of semiconductor rather than mechanical contacts:
- When closed, higher resistance (generating heat), and increased electrical noise
- When open, lower resistance, and reverse leakage current (typically μA range)
- Voltage/current characteristic is not linear (not purely resistive), distorting switched waveforms to some extent. An electromechanical relay has the low ohmic (linear) resistance of the associated mechanical switch when activated, and the exceedingly high resistance of the air gap and insulating materials when open.
- Some types have polarity-sensitive output circuits. Electromechanical relays are not affected by polarity.
- Possibility of spurious switching due to voltage transients (due to much faster switching than mechanical relay)
- Isolated bias supply required for gate charge circuit
- Higher transient reverse recovery time (Trr) due to the presence of the body diode
- Tendency to fail "shorted" on their outputs, while electromechanical relay contacts tend to fail "open".

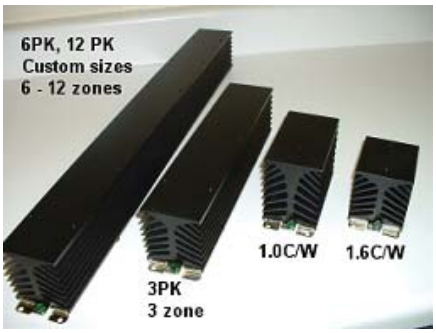




The switching device inside a modern solid state relay starts as a multi-layer structure of P and N layers grown on a silicon wafer. These become the thyristor dies that are used inside a Power-io solid state relay. The dies are available in different sizes in order to accommodate different amperage capabilities. For example, a die that is approximately 0.25 x 0.25 inches may be the size for a 50 amp application and 0.5 x 0.4 inches might be 125 amps. All solid state relays develop heat as a result of a forward voltage drop through the junction of the die at a rate of approximately 1.2°C per amp that is being switched. Beyond a point, heat will require a lowering (or derating) of the load current that can be handled by the solid state relay.

Heatsinks are used to create a method of removing heat away from the current carrying device, thus allowing higher current operation. Adequate heat sinks, including consideration of air temperature and air flow, are essential to the proper operation of a (SSR, SCR, thyristor or IGBT package). It is necessary that the user provide an

Fig 1



effective means of removing heat from the package. The importance of using a proper heat sink cannot be overstressed, since it directly affects the maximum usable load current and/or maximum allowable ambient temperature. Lack of attention to this detail can result in improper switching (lockup) or even total destruction of the solid state relay. Up to 90% of the problems with solid state relays are directly related to heat. There are several customer-specitic heat sink designs where overall size, fin geometry, fin angle / spacing, and draw-down geometry were optimized.

With loads of less than 2-4 amperes, cooling by free flowing convection or forced air currents around the unit is usually sufficient. Loads greater than 4 Amps will require heat sinks. SSR units are to be mounted to some heat sinking metal surface, material heat conductivity should be kept in mind. Heat sinks are approximately equivalent, in heat dissipation, to a sheet of aluminium 1/8" thick by the dimensions shown below:

12" X 12" = 288 square inches of exposed surface area = approximately 2.1°C per watt thermal rise (2.1 C/W)

15" X 15" = 450 square inches = approximately 1.5 degrees C per watt thermal rise (1.5 C/W)

18" X 18" = 648 square inches = approximately 1.0 degree C per watt thermal rise (1.0 C/W)

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The lower the C/W rating, the better the heat sink is at dissipating the heat, given proper ventilation and ambient temperature. For example: if a solid state relay generates 45 watts of heat, on a 2.1 C/W heat sink, that relay's internal dies will increase 94.5°C above the ambient temperature. If the ambient is 40°C, the internal die temperature may be 134.5°C.

The maximum permitted temperature for the thyristor die is typically 125°C but 115°C is often used as an additional margin of safety. If air flow is restricted to near by products, or if the ambient air in the enclosure is warmer, of if the solid state relay is not firmly attached to the heat sink, then additional amperage de-rating will be required.

Heat Sink Material

The best materials for a heat sink are: gold, silver, copper, or aluminum. For industrial applications, aluminium is the most cost effective material. Typically a black anodized finish which provides additional radiant heating dissipation is used. In comparison to aluminium, twice the amount of steel and four times the amount of stainless steel would be needed to achieve the same effect. Solid state relays should never be mounted in an enclosed area without proper air flow. Units should also never be mounted to a plastic base or to painted surfaces. The heat sink should be positioned with the fins in a vertical position with an unimpeded air flow, up and through the finned heat sink. The interface between the solid state relay and the heat sink must be a flat, clean, bare (non-painted) surface that is free of oxidation.

Precautions

Care must be taken when mounting multiple SSRs in a confined area. SSRs should be mounted on individual heatsinks whenever possible. Panel mount SSRs should never be operated without proper heat sinking or in free air as they will THERMALLY SELF DESTRUCT UNDER LOAD. A simple rule-of-thumb for monitoring temperature is to slip a thermocouple under a mounting screw. If the base temperature does not exceed 45 °C under normal operating conditions, the SSR is operating in an optimal thermal environment. If this temperature is exceeded the relay's current handling ability must either be thermally improved by the use of a heatsink, or greater air flow must be provided over the device through the use of a fan. ANY moving air in an installation, greatly improves the thermal transfer from the heatsink to the air. If the actual internal SSR device ever achieves an internal temperature of 115 to 125°C, it will be permanently destroyed. Therefore, the desired engineering requirement is to provide a slow heat-rise internal SSR, and then to provide a heat sinking capability that draws the internal heat rise away at a fast rate to ensure that the internal dies do not exceed these temperatures. Thermal problems are cumulative, irreversible, and destructive.

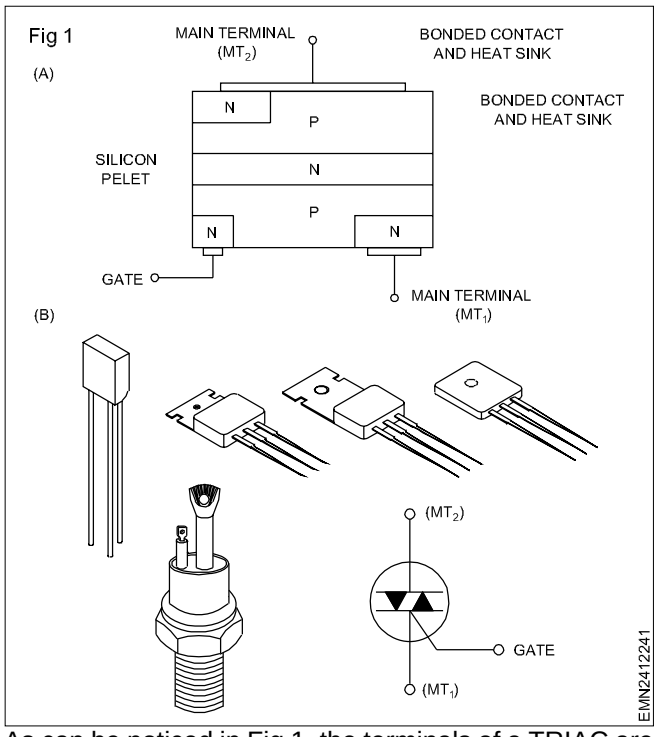
TRIAC, DIAC and their characteristics

Objectives: At the end of this lesson you shall be able to
- **explain the difference between a SCR and a TRIAC**
- **list different ways of triggering a TRIAC**
- **explain the use of TRIAC for full wave control of AC**
- **choose a Triac for a given requirement**
- **explain the method of quick testing a TRIAC**
- **explain the working and use of DIAC**
- **choose a DIAC for a given application**
- **explain the method of quick testing a DIAC.**

TRIAC

TRIAC is a three terminal gated semiconductor device for controlling AC in either direction. The term TRIAC stands for TRIode AC semiconductor. TRIAC is very similar to that of two SCR connected in reverse parallel. A Triac is able to conduct a large current in both directions, being trigged ON in one direction or the other by a gate pulse of the appropriate polarity.

Basic construction of a TRIAC, its symbol and a typical TRIAC is shown in Fig 1a,1b and 1c.



As can be noticed in Fig 1, the terminals of a TRIAC are labeled as,

Main terminal-1(MT1)

Main terminal-2(MT2)

and Gate(G).

This device operated in both directions, hence the terms anode and cathode does not apply.

TRIAC triggering

TRIAC can be triggered/turned-ON by,

1) applying a gate current,

2) exceeding the avalanche breakdown voltage V_{BO}.

3) allowing the MT1 - MT2 applied voltage to increase at a rate in excess of the maximum dv/dt.

Methods 2 and 3 mentioned above are not employed in normal TRIAC operation but they may be considered as limiting factors in circuit design. Hence all further discussion is restricted to triggering the TRIAC via the gate. Since Triac is a bi-directional device, it can be triggered into conduction by a negative or a positive gate signal. TRIACs potentials are all considered with respect to main terminal-1(MT1). This gives the following possible *operating* situations or *modes*;

– MT2 +ve with respect to MT1 —Gate signal +ve (1st quadrant+)

– MT2 +ve with respect to MT1 —Gate signal -ve (1st quadrant-)

– MT2 -ve with respect to MT1 —Gate signal +ve (3rd quadrant+)

– MT2 -ve with respect to MT1 —Gate signal -ve (3rd quadrant-)

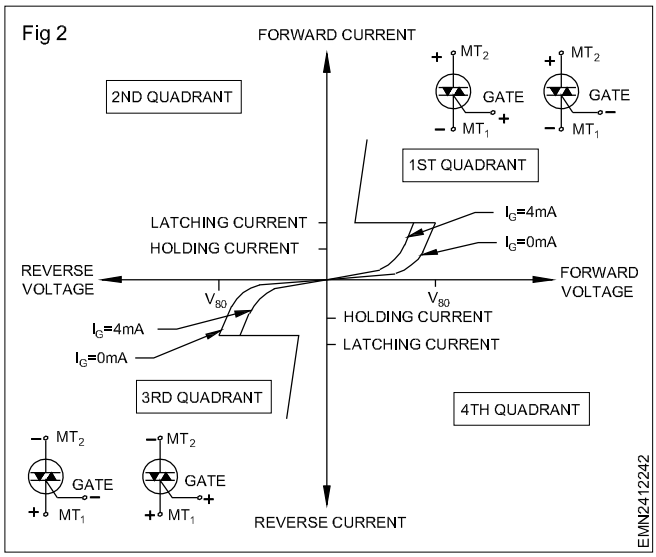
Unfortunately, TRIAC is not equally sensitive in all the above said modes. It is least sensitive in 3rd quadrant mode(MT2 negative with respect of MT1 and trigger by a +ve gate signal) so this mode is very rarely used in practice.

When a TRIAC is ON the current flowing between MT1 and MT2 is known as **Principal current**.

The TRIAC will remain ON as long as the current flowing through it is larger than the holding current as shown in the static characteristics of a Triac in Fig 2.

From the TRIAC static characteristics. When MT2 is positive with respect to MT1, the TRIAC operates in the first quadrant of its static characteristics, if it is not triggered, the small forward current increases slowly with increase in voltage until the breakdown voltage V_{BO} is reached and then the current increases rapidly. The device can be, and usually is, turned 'ON' at a smaller forward current by injecting a suitable gate current and the characteristics shows the effect of increasing the gate current from zero to 4 mA. The gate current must be maintained until the main current is at least equal to the latching current.

When terminal MT1 is positive with respect to MT2 the Triac operates in the third quadrant and the current flows in the opposite direction.



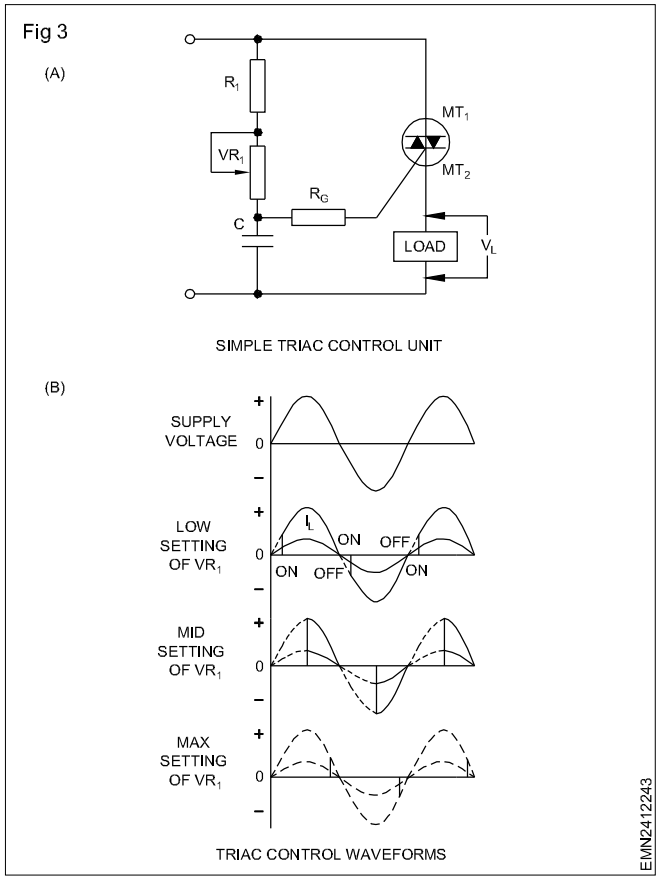
FULL WAVE control using a TRIAC

Fig 3 shows a TRIAC used for controlling the current flowing in an AC circuit. Fig shows the wave forms with different settings of POT V_{R1}.

On observing the waveforms at Fig 3, it can be seen that control is achieved by firing the TRIAC at the same point in both the positive and negative half cycle.Once triggered the device remains ON until the supply is switched OFF.

Choosing a TRIAC

Like all other components, TRIACs have maximum specified values of current and voltage that must not be exceeded. Important specifications of a TRIAC with an example is given below;



TRIAC Type code	:	BT 136	TIC 201D
I_T (rms)	:	4 Amps.	2 Amps.
V_{GT}	:	1.5 Volts.	2.5 Volts.

The value of gate current required to achieve switch on.

V_{DRM}	:	400 Volts.	400 Volts.

The maximum permitted peak voltage.

In TRIACs the terms forward and reverse do not arise since it is bidirectional.

QUICK TESTING TRIACs

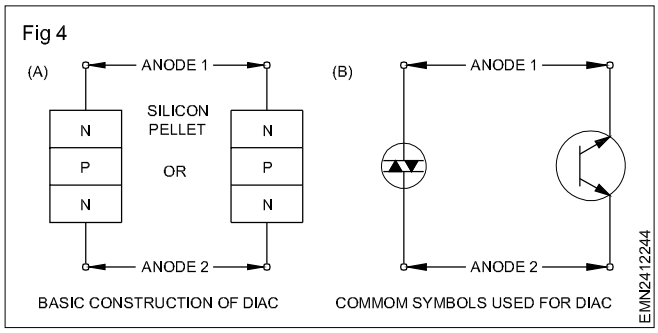
A quick test can be carried out on TRIAC using an ohmmeter. If the readings taken are comparable to the one shown in table below, the TRIAC can be considered as satisfactory and can be used in circuit;

Meter polarities		Resistance
+	-	
MT2	MT1	>1M
MT1	MT2	>1M
MT2	G	>1M
G	MT2	>1M
MT1	G	≃300Ω
G	MT1	≃300Ω

THE DIAC

Like UJTs, DIAC is a semiconductor device used extensively as a trigger device for thyristors gate circuit. In its most elementary form, DIAC is a three layer device as shown in Fig 4.

As can be seen from Fig 4, DIAC is a three layer, two terminal semiconductor device capable of conducting current in both directions.



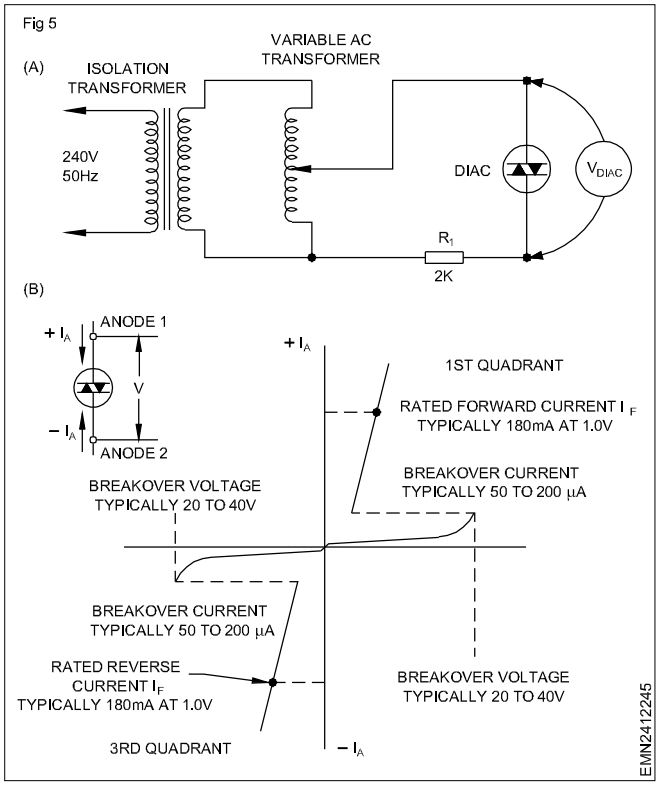
A DIAC acts in a similar manner to two diodes that are connected in reverse parallel and it therefore is able to rectify AC voltage during both half cycles. The symbol used for DIAC is shown in Fig 4b.

DIAC also resembles an NPN or PNP bipolar transistor with no base connection. Unlike bipolar transistor, the DIAC possesses uniform construction. This means, N-type and P-type doping is essentially the same at both

junctions. As shown in Fig 4, diac may be constructed as either an NPN or PNP structure.

Fig 5a shows the experimental set up for testing the DIAC. The isolation transformer is used to isolate the circuit from the supply mains. The variable transformer or variac is used to apply the variable voltage to DIAC under test. The characteristic curve a typical DIAC is shown in Fig 5b.

As shown in the experimental set-up at Fig 5a, when a small voltage of either polarity is applied across a DIAC, the current flows is very small as can be seen from its characteristics in the first and the third quadrants. If the applied voltage is steadily increased, the current will remain at a low value until the applied voltage reaches a value known as the Break over voltage of the DIAC as shown in Fig 12b. Once this point is reached the DIAC current increases rapidly and the DIAC voltage falls to a low value. At this point, the diac exhibits negative resistance characteristics(current conduction increases while the voltage across the device decreases). The DIAC will continue to conduct current as long as the current is greater than the Holding current of the device.



Choosing DIACs

Quick Testing DIACs

Since DIACs are similar to two diodes connected back to back and break down in either direction once the applied voltage reaches the breakdown voltage of the diode, while testing a DIAC using a ohmmeter, it should show high resistance (infinite resistance) when checked in either direction. This quick test only confirms that the DIAC is not shorted; however this quick test is worth carrying out before using the DIAC in a circuit.

Lamp dimmer/fan motor speed regulator using TRIAC and DIAC

Objectives: At the end of this lesson you shall be able to

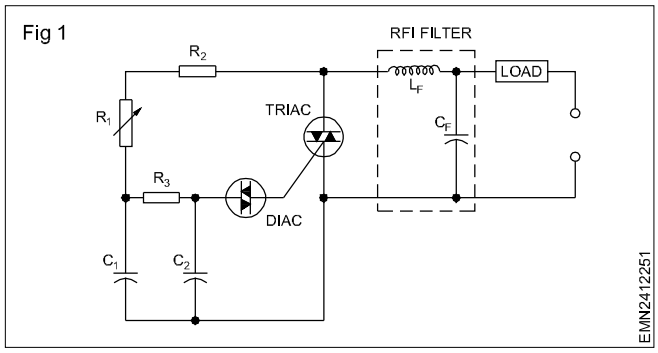
- **explain the advantage of use of TRIAC for speed control of AC motors**
- **explain the need of soft-start light dimmers**
- **draw the circuit of a simple light dimmer using a DIAC and a TRIAC**
- **explain the function of components of a typical soft-start light dimmer**
- **explain the need and working of snubber circuit in a light dimmer circuit.**

TRIAC or SCR for speed control of AC motors

Compared to SCR, TRIAC is more popular and works satisfactorily for speed control of universal motors. Although both SCR and TRIAC can be used to phase control and vary the current through the motor, TRIAC being a full-wave device, symmetrically controls the phase of both half cycles of the applied AC. The resultant full-wave current format then produces smoother motor operation that can be attained from the half-wave rectification using SCRs. This is particularly noticeable during speed control at low speeds.

The circuit at Fig 1 shows a TRIAC phase-control circuit for controlling the speed of universal motors.

The load shown in circuit at Fig 1 is a general load rather than a motor symbol because, this circuit can also be used for light dimmers and for the control of heaters.



This circuit features a double time constant phase-shift network. This reduces hysteresis in firing of the TRIAC, thereby making the manual adjustment of speed more repeatable.

The DIAC used as trigger device, adds to the reliability of

the circuit. The elemental low-pass filter comprising L_F and C_F attenuates much of the radio-frequency interference(RFI)) that gets generated and tries to get in to the power line. Such high-frequency RFI energy is generated by the extremely rapid turn-on time of the TRIAC.

LAMP DIMMERS

Lamp dimmer is a circuit which controls AC power supplied to an incandescent lamp thereby controlling the intensity of light emitted by the lamp from almost zero to full brilliance.

Conventional and soft-start dimming of incandescent lights

Old technology light dimmers used high wattage rheostats, adjustable auto-transformers, or saturable reactors, which were large, expensive,and generated considerable heat. Present day semiconductor light dimmers have over come these deficiencies and have therefore become very popular for many applications.

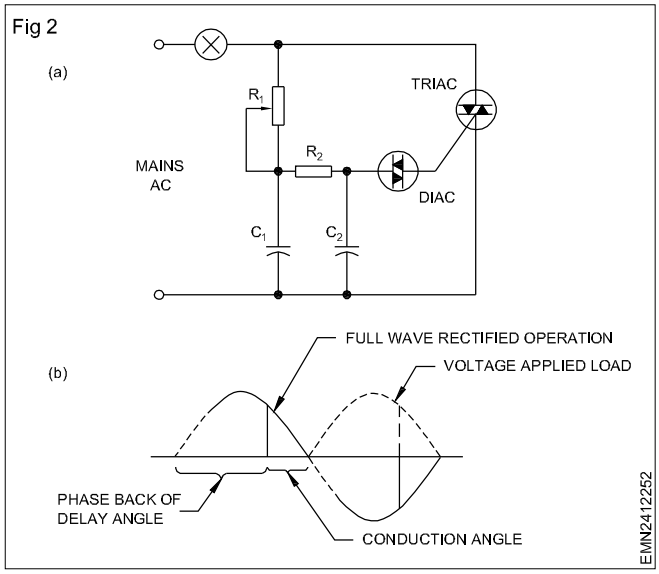
Modern thyristor dimmers are inexpensive, reliable, small, generate little heat, and are easy to control remotely. These properties have not only permitted semiconductor dimmers to supersede older types in theaters and auditoriums with excellent results, but have made dimmers practical for built-in home lighting, table and floor lamps, projection equipment and other uses.

Two light dimmers for incandescent light bulbs are discussed below. Both these dimmer circuits control light intensity by adjusting the angle of conduction of a Triac connected in series with the bulb. The first dimmer uses a very simple circuit that is ideal for highly compact applications requiring minimum cost. The second dimmer features soft starting for low inrush current and consequent long lamp life. Soft start lamp dimmers are especially useful with expensive lights with short lives, such as projection lamps and photo-graphic bulbs.

Simple light dimmer

The circuit shown in Fig 2 is a wide range light dimmer using very few parts. The circuit can be operated using any mains supply source(240V, 50 Hz) by choosing apppropriate value of circuit components. The circuit can control up to 1000 watts of power to incandescent bulbs.

Fig 2



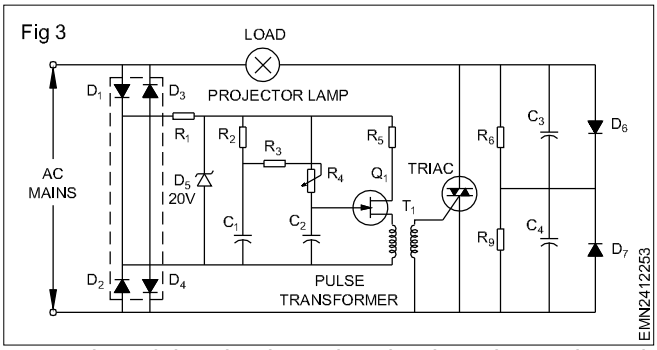
The power to the bulbs is varied by controlling the conduction angle of TRIAC. Many circuits can be used for phase control, but the single Triac circuit used is the simplest and is therefore chosen for this particular application.

The control circuit for this TRIAC must function as shown Fig 2b. The control circuit must create a delay between the time voltage is applied to the circuit and the time it is applied to the load. The TRIAC is triggered after this delay and conducts current through the load for the remaining part of each alternation. This circuit can control the conduction angle from 0° to about 170° and provides better than 97% of full-power control.

Light Dimmer with soft-start option

The circut at Fig 3 is a light dimmer with soft start option. Soft starting is desirable because of the very low resistance of a cold lamp filament compared to its hot resistance. At the time of initial switching on, the low resistance of the lamp causes very high inrush currents which leads to short filament/lamp life. Lamp failures caused by high inrush currents is eliminated by the soft start feature, which applies current to the bulb slowly enough to elliminate high surges.

Fig 3



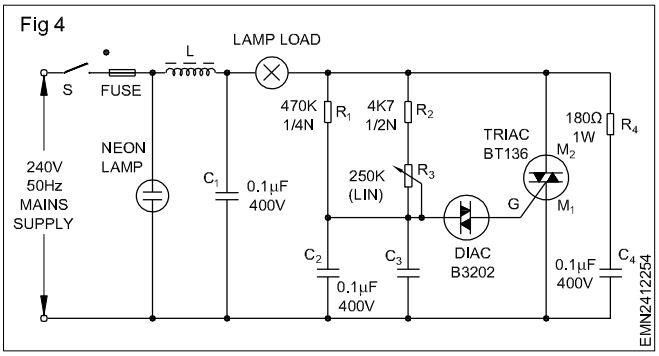
Operation of the circuit at Fig 3 begins when voltage is applied to the diode bridge consisting of D_1 through D_4. The bridge rectifies the input and applies a dc voltage to resistor R_1 and zener diode D_1. The zener provides a constant voltage of 20 volts to unijunction transistor Q_1, except at the end of each alternation when the line voltage drops to zero. Initially the voltage across capacitor C_1 is zero and capacitor C_2 cannot charge to trigger Q_1. C_1 will begin to charge, but because the voltage is low, C_2 will have adequate voltage to trigger C_1 only near the end of the half cycle. Although the lamp resistance is low at this time, the voltage applied to the lamp is low and the in rush current is small. Then the voltage on C_1 rises, allowing C_2 to trigger Q_1 earlier in the cycle. At the same time the lamp is being heated by the slowly increasing applied voltage and by the time the peak voltage applied to the lamp has reached its maximum value, the bulb has been heated sufficiently so that the peak inrush current is kept to a reasonable value. Resistor R_4 controls the charging rate of C_2 and provides the means to dim the lamp. Power to the load can be adjusted manually by varying the resistance of R_4. T_1 is a pulse transformer. In addition to supplying the trigger to Triac,

this transformer isolates the high current load circuit form the low power triggering circuit (gate isolation methods for TRIAC in discussed in further paragraphs).

A simple Lamp dimmer cum Universal motor speed controller

In the lamp dimmer cum universal speed controller circuit shown in Fig 4, a TRIAC is used as control device. Phase control techinque is used to control conduction angle of the TRIAC which inturn control the power fed to the lamp.

Fig 4



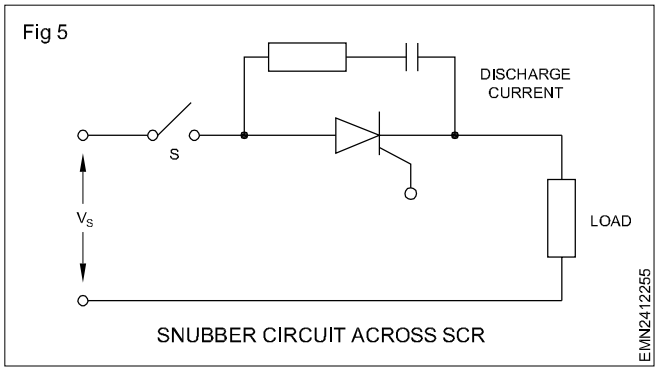
A lamp L is connected in series with AC mains supply to the TRIAC. The trigger pulses to TRIAC gate is given through DIAC. The DIAC is triggered at the same break over voltage level (30 V) during both positive and negative half cycles.

Potentiometer R_4 provides the facility for varying the intensity of light or speed of a universal motor.

Snubbers

Snubber is a small network of resister and capacitor connected across the switching circuit in power electronics as shown in Fig 5.

Fig 5

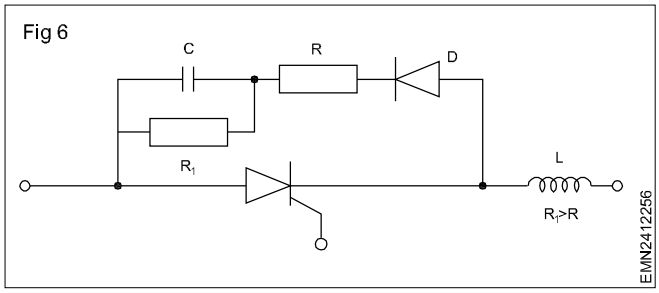


The fanction of snubber is to control the circuit reactance by absorbing the voltage spikes caused by the switching action. The purpose of snubber is to eliminate the voltage transient and ringing that occurs when the SCR opens. The snubber provides an alternate path for the current flowing through the RC circuit

Snubber circuits enhance the performance of the switch circuits by using additional comporents like diode D also shown in Fig 6 .The diode 'D' acts as a free wheeling diode to protect the SCR.

This also consists of an inductance L in series with the SCR to prevent the high di/dt that leads to damage the SCR And hence, a small value of resistance is placed in series with the capacitor to limit the high discharge current .

Fig 6



Snubber circuits are used to minimise switching losses in converters and associated high dv/dt and di/dt stress across power semi conductor devices. snubber circuits are of turn-ON and turn - OFF type and placed in series and parallel respectively.

Snubber Circuit

One problem with the TRIAC control is the sudden application of reverse voltage across the TRIAC immediately after it has stopped conduction. This is a serious problem when the load is a highly inductive as in motors. This reapplied voltage denoted by dv/dt can trigger-on (unwanted or false triggering) the device losing the phase control.

To avoid this false triggering, an R and C series network is placed across the circuit(R_4 and C_4 as shown in Fig 4). This RC network slows down the rate of rise of voltage applied across the TRIAC. This RC circuit connected across the TRIAC circuit is called Snubber circuit.

The inductance L and capacitor C_1 forms a low pass filter to substantially reduce the radio frequency interference (RFI) generated by the rapid turn-on and turn-off the TRIAC.

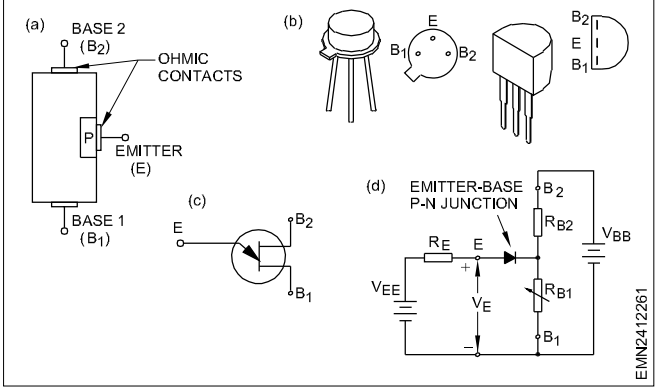
The lamp dimmer circuit at Fig 4 can be used equally well as a fan speed regulator. The only change to be made is to connect a fan in place of the lamp shown in the circuit at Fig 4. The speed can be varied from almost zero to full speed by just rotating POT R_3.

Unijunction transistor (UJT) and its applications

Objectives: At the end of this lesson you shall be able to
- **explain the construction and working principle of UJT**
- **make a quick test of UJT**
- **list the important specification of UJT**
- **list and explain the application of UJTs**

Unijunction transistor(UJT) is a three terminal semiconductor device as shown in fig 1a. In its appearance it looks like a transistor as shown in Fig 1b. As shown in Fig 1a, it consists of two layers(a P-layer and a N-layer) and therefore it has only one junction(hence its name, uni-junction).

Fig 1

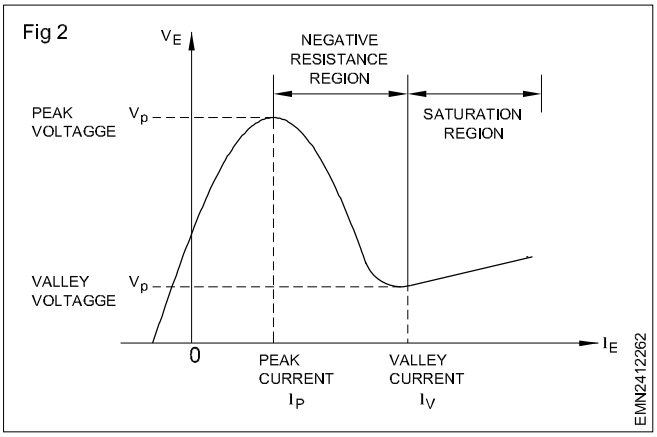


The symbol of UJT and its electrical equivalent circuit is shown in Fig 1c and 1d.

UJT is a special semiconductor device because it exhibits negative resistance characteristics as shown in Fig 2. The details of the characteristics are discussed in subsequent paragraphs.

Construction of UJT

Fig 2



2646 and 2N 2647 UJT's are available in the modified TO-18 case style as shown in Fig 1b.

Equivalent circuit of UJT

The electrical equivalent circuit of UJT is shown in fig 1d. The resistance between the B_1 and B_2 terminals is called the inter-base resistance R_{BB}. The N-type silicon bar serves as a resistance divided into two parts R_{B1} and R_{B2} by the PN junction. The total of the internal R_{B1} and R_{B2} is the interbase resistance R_{BB}. Value of R_{BB} is typically in the range of 4 to 10 Kohms. Also r_{B1} usually a little greater than r_{B2} because the emitter is a little closer to B_2.

The interbase resistance R_{BB} is measured with the emitter open.

$R_{BB} = R_{B1} + R_{B2}$ at I_E=0.

Operation of UJT

The DC supply polarities for a UJT to function is shown in Fig 3. As can be seen from fig 3, B_2 is connected to +ve and B_1 to ground. As a result current(conventional) flows from B_2 to B_1. This conduction results in a voltage gradient along the N-type silicon bar. Therefore there is a voltage in the region of the emitter junction(V_E) which is positive with respect to ground. The magnitude of this voltage is given by the simple voltage divider action between R_{B1} and R_{B2}.

$$V_E \text{ or } (V_{RB!}) = \frac{R_{B1}}{R_{B1}+R_{B2}} V_{BB} = \eta V_{BB} \quad \text{....[1]}$$

The Greek letter η (eta) is called the intrinsic stand-off ratio. This is an important data of any UJT and is invariably mentioned in all UJT data sheets. From the above equation, intrinsic stand-off ration η (eta) is given by,

$$\eta = \frac{R_{B1}}{R_{B1}+R_{B2}} \quad \text{....[2]}$$

Typical values of h Vary form about 0.5 to 0.8 for most UJTs.

The value of h is important because, knowing h and the applied voltage across the base terminals V_{BB}, voltage across R_{B1} can be calculated using equation [1].

For example, if η = 0.65 and V_{BB} = 12 Volts,

then, $V_{RB1} = \eta\ _{VBB}$ = 0.65 x 12 V = 7.8 volts.

Voltage V_{RB1} represents the reverse bias voltage at diode D.In order for an emitter current I_E to flow, the emitter voltage V_{EB1} should be above V_{RB1} by about 0.7volts(internal barrier potential for a silicon diode). This emitter voltage V_{EB1} that will cause the diode to be forward biased and conduct emitter current is usually designated as V_P.

The value of V_P can be calculated using the formula,

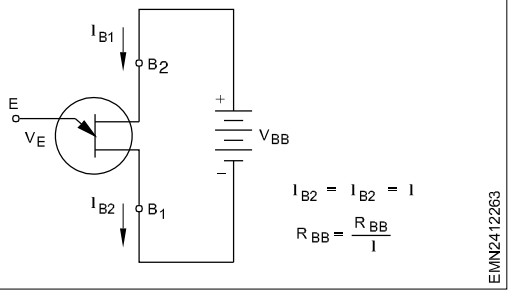
$V_P = \eta\ V_{BB}$ + 0.7 volts

In the example considered above, V_P = 7.8 V + 0.7V = 8.5 Volts.

When V_P is raised to 8.5 volts, diode D conducts. This means I_E flows through the R_E,diode D, R_{B1} to ground. This

sudden rush of current through the highly doped N-type R_{B1} reduces the resistance of R_{B1}(remember R_{B1} is not a fixed value resistor, it is the resistance of the N-type semiconductor). Because of the reduced R_{B1}(from a few thousand ohms to a value as low as 40 to 50 ohms) results in a small voltage drop across R_{B1}. Hence emitter voltage V_{EB1} drastically decreases to around 1 volt(from 8.5V before the diode conduction to around 1V when the diode starts conducting). This drop in the value of V_{EB1} is shown in Fig.3. This point is sometimes referred to as the on-state condition.

Fig 3

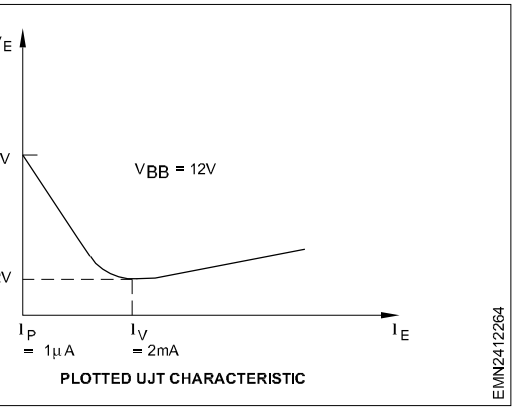


Since an increase in the emitter current results in decrease in emitter voltage(V_{EB1}), this region of the UJT characteristics is referred to as the negative resistance region.

After a certain point referred to as the 'valley point', any further increase in the emitter biasing voltage V_{EE}/emitter current I_E will start increasing and the voltage drop across the emitter and base-1. This region is called as the UJTs saturation region. This will occur when the rate of hole injection is so great as to build up a positive space charge in the region. It should be noted that after the valley point, the emitter current should not be increase beyond the rated maximum forward emitter current value(typically around 50mA) beyond which the diode D may break down.

A comparison of the UJT theoritical characteristics(as in Fig 2) and actual characteristics which can be plotted is shown in Fig 4.

Fig 4



Some of the important terms associated with UJT characteristics are given below;

Peak Point Current(I_P) - minimum amount of emitter current to place the UJT in negative resistance region.

Valley Current (I_V) - maximum allowable emitter current within the negative resistance region.

Valley voltage (V_V) - minimum voltage that can maintain the UJT in its negative resistance region.

Quick test of UJT using Ohm meter

From the construction of a UJT it can be seen that, Emitter and Base-1 with Base-2 open, behaves as a PN diode. Therefore, when tested using a ohm meter this should show low resistance when forward biased and high resistance when reverse biased.

Similarly Emitter and Base-2 with Base-1 open behaves as a PN diode and hence the same forward and reverse bias test using a ohm meter can be carried out to confirm its good condition.

To carry out a quick test of a given UJT, check forward and reverse bias conditions of the two diodes of UJT as given in above two paragraphs.

Typical UJT Specifications

UJT specification as can be seen in any data manual is given below. 2N 2646 UJT is taken only as a sample for understanding the specifications. Specifications for other UJT will almost be in the same format. However the manufacturers data sheets given more details than what is listed below;

Type	Device	I_P	I_V	R_{BBO}	Eta(η)
2N 2646	UJT-P	5µA	4mA	15Kohms	0.60

Application of UJTs

UJTs are employed in a wide variety of circuits involving electronic switching and voltage or current sensing applications. These include,

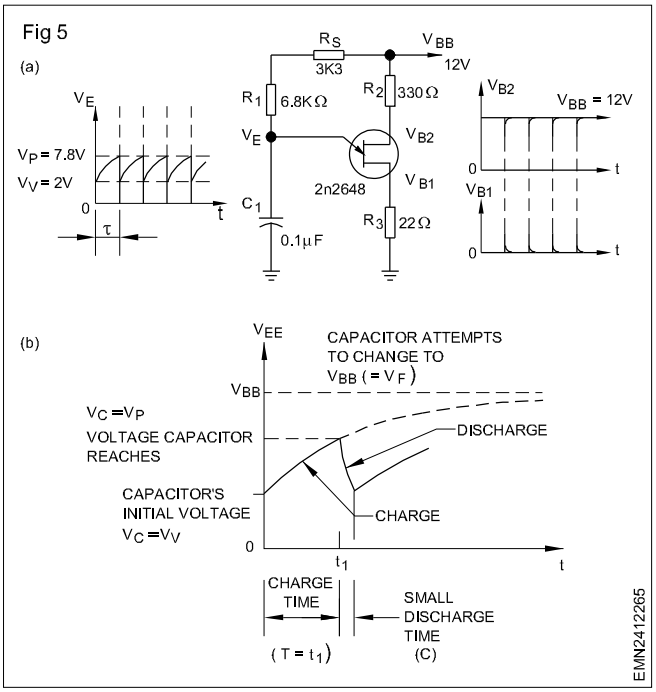
– Triggers for thyristers
– As oscillators
– As pulse and Saw tooth generators
– Timing circuits
– Regulated Power supplies
– Bistable circuits

and so..on.

The most common and popular application of UJT is the Relaxation oscillator. Fig 5a shows a practical relaxation oscillator using 2N 2646 UJT.

As the voltage V_{BB} is supplied, capacitor C is charged via Resistors R_s and R_1. If the voltage V_C across the capacitor cross the peak point voltage(V_P) of UJT, the UJT goes into conduction.

The sooner UJT goes into conduction, the charged capacitor C discharges rapidly as shown in Fig 5b via the low inner base resistance R_{B1} and R_3. This conduction of UJT and the discharge of C through the emitter-Base1 of UJT results in a sudden rush of current through R_3 and hence the voltage



across R_3 increases sharply as shown in Fig 5.

By discharging the voltage across it, the voltage across the capacitor becomes smaller than the valley point voltage V_V. Because of this, UJT cuts-off once again. Because the UJT is cut-off, there is no current through R_3 and hence the voltage across it (output voltage) becomes zero as shown in Fig 5.

Once the UJT is cut-off, capacitor C starts charging again through R_S and R_1. When the charged voltage again crosses the value of V_P, UJT turns-on again and the cycle repeats resulting in continuous pulse wave form at the output(across R_3).

The frequency of oscillation of the UJT oscillator depends on,

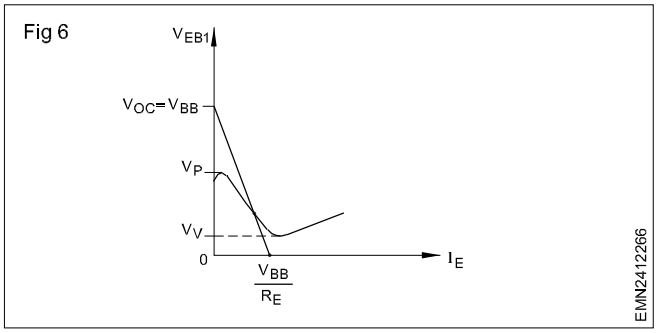
[1] Time constant tau(τ) given by tau(τ) = R_E x C

and [2] Value of intrinsic standoff ratio eta(η) of the UJT.

The frequency of oscillation(f_o) of the UJT relaxation oscillator is given by the formula,

$$f_o = \frac{1}{T} \approx \frac{1}{R_E C_1 l_n \left[\frac{1}{(1-\eta)}\right]}$$

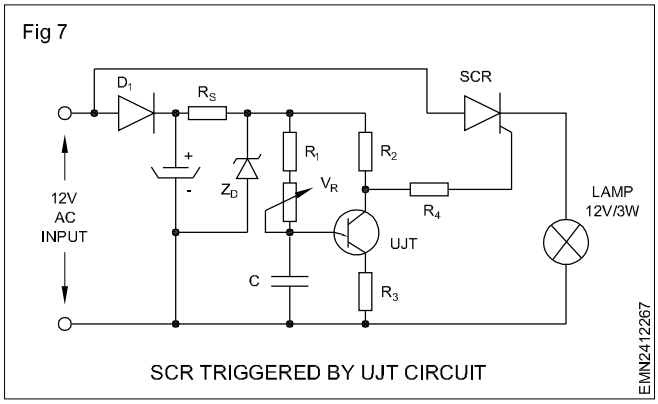
For a UJT to function properly in an oscillator, its DC load line must cross the negative resistance region of its emitter characteristics as shown in Fig 6.



An important thumb rule while designing an relaxation oscillator using UJT is given below;

Minimum and Maximum values of R_E to ensure oscillations,

UJT Triggered SCR circuit is one of the application of UJT in the UJT relaxation oscillator, that is used to trigger the SCR to control its load current as shown in Fig7.



In this circuit, the gate triggerring pulses are shaped by the values of variable resisteor V_R and decides the timing of trigger pulse produced by the UJT. This in turn controls the brightness of the lamp load current supplied by the SCR's triggering pattern.

MOSFET

Objectives : At the end of this lesson you shall be able to
- **state the principle of operation of MOSFET and its types**
- **list the special type of MOSFETs**
- **explain the features of MOSFETs.**

In MOSFETs, control is via an insulating layer instead of a junction (as in JFETS). This insulating layer is generally made of silicon dioxide, from which the very name MOSFET is derived(Metal Oxide Semiconductor). Some times the MOSFETs are also referred to as Insulated-gate FET, for which the abbreviation used are IFET or IGFET.

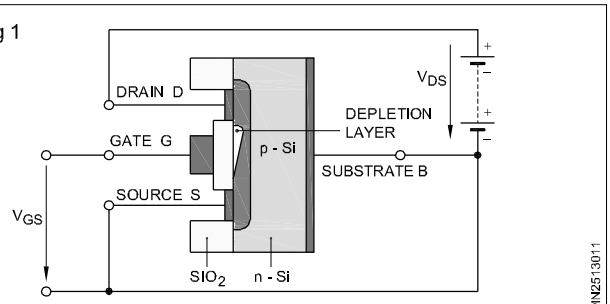
Types of MOSFETs

Depletion-type MOSFETs

Construction and mode of operation

Fig 1 shows the construction of a depletion MOSFET of the n-channel type.

Fig 1



Here, two highly doped n-zones are diffused into a p-doped silicon plate, which is referred to as the substrate, and are provided with junction-free drain and source connections. Between the two zones there is a thin weakly n-doped channel, which produces an electrical connection between the source and drain without an external field-action. This channel is covered by an insulting layer of silicon dioxide (SiO_2), to which a metal electrode is applied as the gate connection.

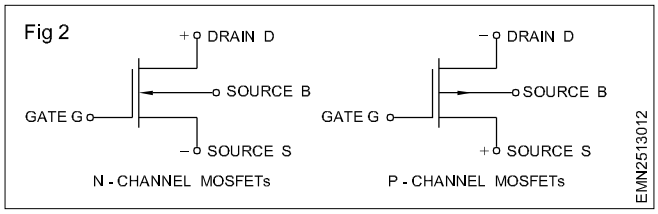
If a voltage U_{DS} is applied between source and drain, at U_{GS} = 0V an electron current flows from the source electrode via the n-channel to the drain electrode. If, however, a negative voltage is applied to control electrode G, the electrons present in the n-channel are forced out of the vicinity of the gate electrode, so that a zone depleted of charge carriers is produced there. This causes a constriction of the n-channel and consequently also a reduction of its conductivity. If the gate voltage becomes more negative, the conductivity of the channel is reduced, as is consequently also the drain current I_D. Another peculiarity of depletion-type MOSFETs is that they can also be controlled with a positive gate-voltage. Charge carriers are then drawn out of the p-doped substrate into the n-channel and its conductivity is increased even further, compared with the conductivity at U_{GS} = 0V.

Designations and circuit symbols

The same designations are used for the connections of MOSFETs as they are for JFETs, i.e source, drain and gate. MOSFETs, however, have another electrode, which is referred to as the substrate connection. Together with the semiconductor material of the channel, this substrate forms a p-n junction, which can be used as a second control-electrode. It is then led out of the casing, like the other electrodes. In a number of versions, however, the substrate electrode is connected directly to the source connection in the casing, which rules out the additional control possibility.

Fig 2 shows the circuit symbols for depletion-type n-channel MOSFETs and p-channel MOSFETs. For the n-channel type, the arrow points towards the line representing the channel; in the case of the p-channel type, on the other hand, it points away from the line representing the channel. The continuous line representing the channel indicates that it is a depletion-type MOSFET.

Fig 2



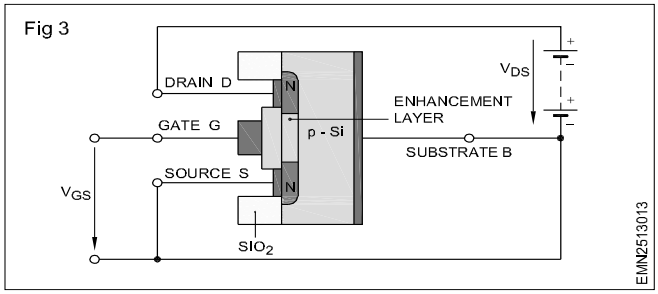
N-channel MOSFETs are operated with a positive drain-source voltage. They have a considerably greater practical significance than p-channel MOSFETs, which require a negative drain-source voltage for their operation.

Enhancement-type MOSFETs

Construction and mode of operation

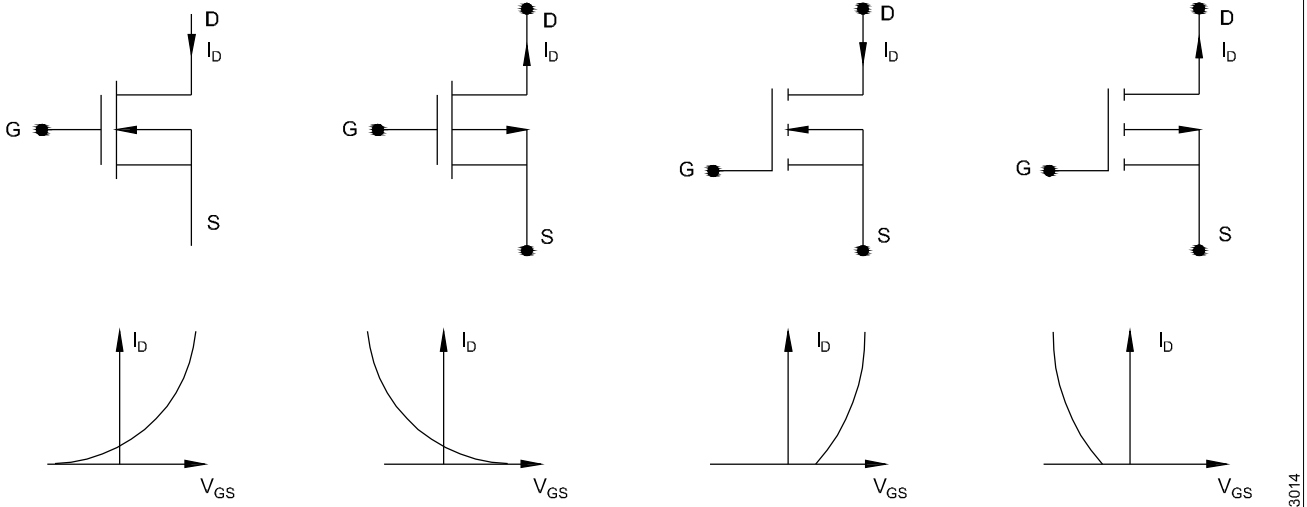
Enhancement-type MOSFETs have a similar technological construction to the depletion types. Without the external action of a field, however, no conducting channel exists between the drain connection and the source connection, so that at U_{GS} = 0V, no drain current can flow. Fig. 3 shows the construction of an enhancement-type n-channel MOSFET.

Fig 3



The same circuit designations are used for the four electrodes of the enhancement-type MOSFET as they are for the depletion types: drain, source, gate and substrate. The circuit symbols used are different. The line representing the channel in the circuit symbol is discontinuous for an enhancement - type MOSFET. This indicates that no drain current I_D flows at U_{GS}=0V. The circuit symbols for the two types of enhancement MOSFET are given in Fig. 4.

Fig 4



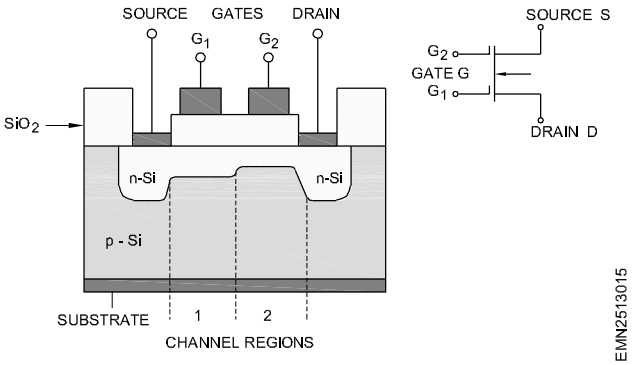
Enhancement-type MOSFETs are only rarely produced as individual transistors. Their construction and working principle are, however, widely used in integrated MOS switching circuits.

Special types of MOSFET

Dual-gate MOSFET

The dual-gate MOSFET is a special type of depletion MOSFET. It has two series-connected channel regions as the current path. The conductivity of each of these two channel regions can be independently controlled via its own gate. The construction and circuit symbol of a depletion-type dual-gate MOSFET of the n-channel type are reproduced in Fig.5. Because of the four connections, this special type is also referred to as a “MOSFET tetrode”.

Fig 5

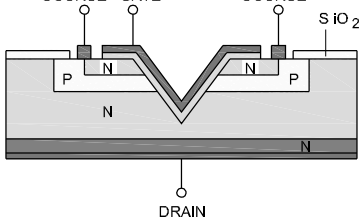


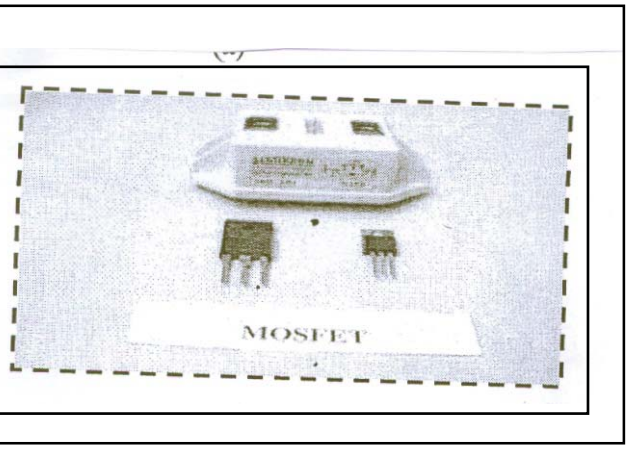
VMOSFET

The field-effect transistors dealt with so far, can handle only relatively small powers during amplification or switching. The reason for this is the relatively long channel of approximately 5 µm with a forward resistance of approximately 1kΩ to 10kΩ. With present-day manufacturing techniques, it is possible to produce a vertical structure for field-effect transistors, instead of the customary horizontal sequence of layers. consequently, higher allowable currents and voltages are obtained, so that considerably greater powers can be amplified or switched.

Fig. 6 shows the construction of an enhancement-type n-channel VMOSFET and the associated circuit symbol.

Fig 6





From above Fig. 7 it can be concluded that depletion type MOSFETs are normally ON type switches i.e, with the gate terminal open a nonzero drain current can flow in these devices. This is not convenient in many power electronic applications. Therefore, the enhancement type MOSFETs (particularly of the n-channel variety) is more popular for power electronics applications. This is the type of MOSFET which will be discussed in this lesson. Fig. 6(b) shows the photograph of some commercially available n-channel enhancement type power MOSFETs.

Operating principle of a MOSFET

At first glance it would appear that there is no path for any current to flow between the source and the drain terminals since at least one of the **p n** junctions (source - body and body-drain) will be reverse biased for either polarity of the applied voltage between the source and the drain. There is no possibility of current injection from the gate terminal either since the gate oxide is a very good insulator. However, application of a positive voltage at the gate terminal with respect to the source will convert the silicon surface beneath the gate oxide into an n type layer or "channel", thus connecting the source to the drain as explained next.

The gate region of a MOSFET which is composed of the gate metallization, the get (silicon) oxide layer and the p-body silicon forms a high quality capacitor. When a small voltage is application to this capacitor structure with gate terminal positive with respect to the source (note that body and source are shorted) a depletion region forms at the interface between the SiO_2 and the silicon as shown in the fig. 8(a)

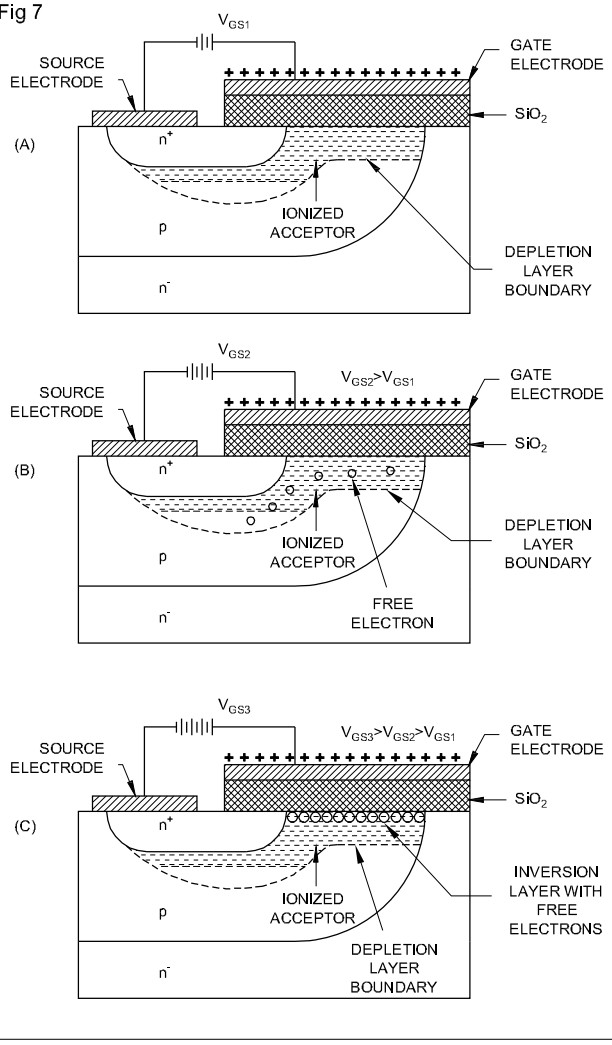
The positive charge induced on the gate metallization repels the majority hole carriers from the interface region between the gate oxide and the P type body. This exposes the negatively charged acceptors and a depletion region is created.

Further increase in V_{GS} causes the depletion layer to grow in thickness. At the same time the electric field at the oxide -silicon interface gets larger and begins to attract free electrons as shown in fig. 8b. The immediate source of electron is electron-hole generation by thermal ionization. The holes are repelled into the semiconductor bulk ahead of the depletion region. The extra holes are neutralized by electrons from the source.

As V_{GS} increases further the density of free electrons at the interface becomes equal to the free hole density in the bulk of the body region beyond the depletion layer. The layer of free electrons at the interface is called the inversion layer and is shown in Fig. 8(c). The inversion layer has all the properties of an n type semiconductor and is a conductive path or "channel" between the drain and the source which permits flow of current between the drain and the source. Since current conduction in this device takes place through an n-type "channel" created by the electric field due to gate source voltage it is called "enhancement type n-channel MOSFET".

The value of V_{GS} at which the inversion layer is considered

Fig 7



to have formed is called the "gate-source threshold voltage $V_{GS}(th)$". As V_{GS} is increased beyond $V_{GS}(th)$ the inversion layer gets somewhat thicker and more conductive, since the density of free electrons increase further with increase in V_{GS}. The inversion layer screens the depletion layer adjacent to it from increasing V_{GS}. The inversion layer screens the depletion layer adjacent to it from increasing V_{GS}. The depletion layer thickness now remains constant.

FET Vs MOSFET

The transistor, a semiconductor device, is the device that made all our modern technology possible. It is used to control the current and even to amplify it based on an input on an input voltage or current. There are two major types of transistors, the BJT and the FET. Under each major category, there are many subtypes. This is the most significant difference between FET and MOSFET. FET stands for field effect transistor and is a family of very different transistors that collectively rely on an electric field created by the voltage on the gate in order to control the current flow between the drain and the source. One of the many types of FET is the Metal - Oxide Semiconductor field effect transistor or MOSFET. The Metal - Oxide Semiconductor (i.e) silicon di oxide is used as an insulating layer between the gate and the substrate of the transistor.

The silicon dioxide is basically a capacitor is basically a

capacitor that holds charge whenever voltage is applied to the gate. This charge then creates a field by pulling oppositely charged particles or repelling particles with the same charge and allows or restricts the flow of the current between the drain and source.

CMOS (complementary Metal -Oxide Semiconductor) basically uses a p-type and n-type MOSFETs in pairs to complement each other. In this configuration, MOSFETS only have significant power consumption during switching and not while it holds its state. This is very desirable, especially in modern computing equipment where power and thermal limits are pushed to the edge. Other types of FET cannot replicate this capability or are too expensive to manufacture.

Advancements in MOSFETs are constantly evolving, both in size as companies keep going into smaller architectures. But also in design like the 3D MOSFETs that show a lot of promise. MOSFETs are the transistor of choice for today as researchers try to find other types of transistors that can be a suitable replacement for it.

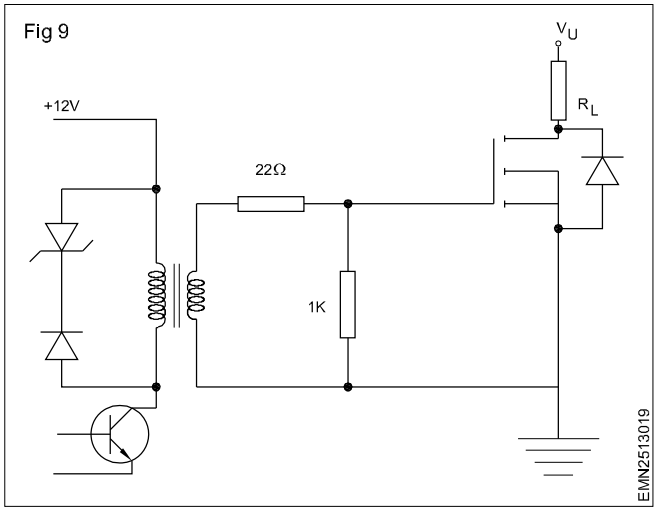
Advantages of MOSFET

1. Low gate signal power requirement.
2. Fast switching speed. No storage time effect as in transistors.
3. Power MOSFETs are not subjected to forward or reverse bias secondary breakdowns.

Drive circuit for MOSFETs

There are several circuits for turning a power MOSFET ON or OFF. The type of circuit depends on application. As a thumb rule, the higher the gate current at turn-on and turn-off, the lower will be switching losses. A sample drive

Fig 9



circuit for a MOSFET is shown in the figure below.

A common method of coupling the drive circuitry is to use a pulse transformer. PTs are used to isolate logic circuitary from MOSFETs operating at high voltages.

Insulated Gate Bipolar Transistor (IGBT)

Objectives : At the end of this lesson you shall be able to
- **explain the characteristics of IGBT**
- **differentiate the FET and MOSFET**
- **list the advantages and disadvantages of IGBT**
- **differentiate between BJT and IGBT.**

Introduction to IGBT

The insulated gate bipolar transistor or IGBT is a three-terminal power semiconductor device, noted for high efficiency and fast switching.

It has high input impedance and large bipolar current - carrying capability.

It switches electric power in many modern appliances: electric cars, variable speed refrigerators, air-conditioners, and even stereo systems with switching amplifiers. Since it is designed to rapidly turn on and off, amplifiers that use it often synthesize complex waveforms with pulse width modulation and low-pass filters. The IGBT combines the simple gate-drive characteristics of the MOSFETs with the high-current and low-saturation-voltage capability of bipolar transistors by combining an isolated gate FET for the control input, and a bipolar power transistor as a switch, in single device. The IGBT is used in medium - to high-power applications such as switched mode power supply, traction motor control and induction heating. Large IGBT modules typically consist of many devices in parallel and can have very high current handling capabilities in the order of hundreds of amperes with blocking voltages of 6,000V.

The IGBT is suitable for many applications in power electronics, especially in Pulse Width Modulated (PWM) servo and three-phase drives requiring high dynamic range control and low noise. It also can be used in Uninterruptible Power Supplies (UPS), Switched-Mode Power Supplies (SMPS), and other power circuits requiring high switch repetition rates. IGBT improves dynamic performance and efficiency and reduced the level of audible noise. It is equally suitable in resonant-mode converter circuits.

The main advantages of IGBT over a Power MOSFET and a BJT are:

1 It has a very low on-state voltage drop due to conductivity modulation and has superior on-state current density. So smaller chip size is possible and the cost can be reduced.

2 Low driving power and a simple drive circuit due to the input MOS gate structure. It canbe easily controlled as compared to current controlled devices (thyristor, BJT) in high voltage and high current applications.

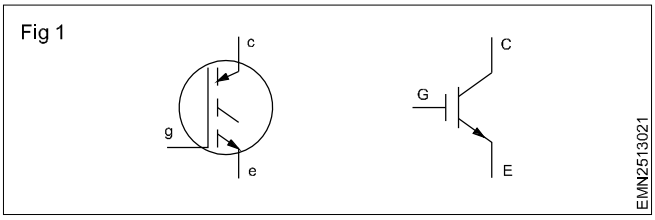
3 It has superior current conduction capability compared with the bipolar transistor. It also has excellent forward and reverse blocking capabilities.

The main drawbacks are:

1 Switching speed is inferior to that of a Power MOSFET and superior to that of a BJT. The collector current tailing due to the minority carrier causes the turnoff speed to be slow.

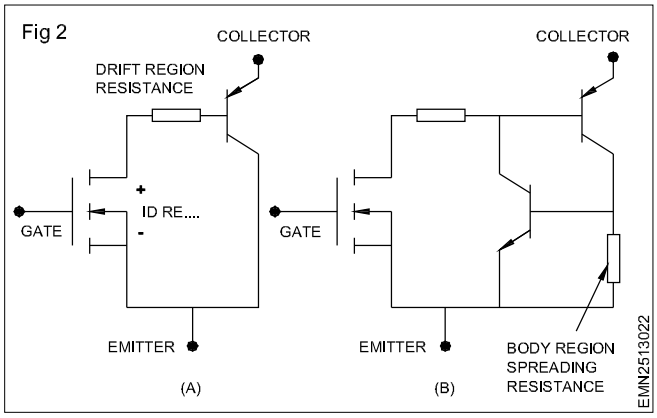
2 There is a possibility of latchup due to the internal PNPN thyristor structure.

Fig 1



The IGBT is a semiconductor device with four alternating layers (P-N-P-N) that are controlled by a metal-oxide semiconductor (MOS) gate structure without regenerative action.

Fig 2



Difference betweeen BJT and IGBT

1 BJT is a current driven device, whereas IGBT is driven by the gate voltage.

2 Terminals of IGBT are known as emitter, collector and gate, whereas BJT is made of emitter, collector and base.

Light Emitting Diodes (LEDs)

Objectives: At the end of this lesson you shall be able to
- **state the advantages of LEDs over-conventional bulbs**
- **state how light is radiated from LEDs**
- **list popular types of LEDs & Infra red LEDs**
- **explain why LEDs cannot be confidently tested using ohmmeter**
- **calculate the resistor value to be used with LED for a given application**
- **state how to protect LEDs from high reverse voltage**
- **explain the working principle of LDR, photoresister and Laser diode**
- **optical sensor and its types and application**
- **optocoupler and its types and applications**
- **opto-Isolator and its types and application.**

Light Emitting Diodes

In recent years, the use of filament lamps/bulbs which consume quite an amount of power, has less life and delicate to handle are becoming obsolete as output indicators of electric systems. With the advancement in the field of optical electronics several devices have been developed as a substitute for filament lamps. One of the most common and popular of these new devices is the **Light Emitting Diode** abbreviated as **LED**. These LEDs are now used as indicators in almost all electrical and electronic circuits and equipments.

The advantages of LEDs over incandescent bulbs are listed below;

1 LEDs have no filaments to heat and so require less current to glow.

2 LEDs require lower voltage level (typically 1.2 to 2.5 V) than the conventional bulbs.

3 LEDs last much longer - upto several years.

4 Because there is no filament to heat up, LEDs are always cool.

5 LEDs can be switched ON and OFF at a much faster rate compared with conventional lamps.

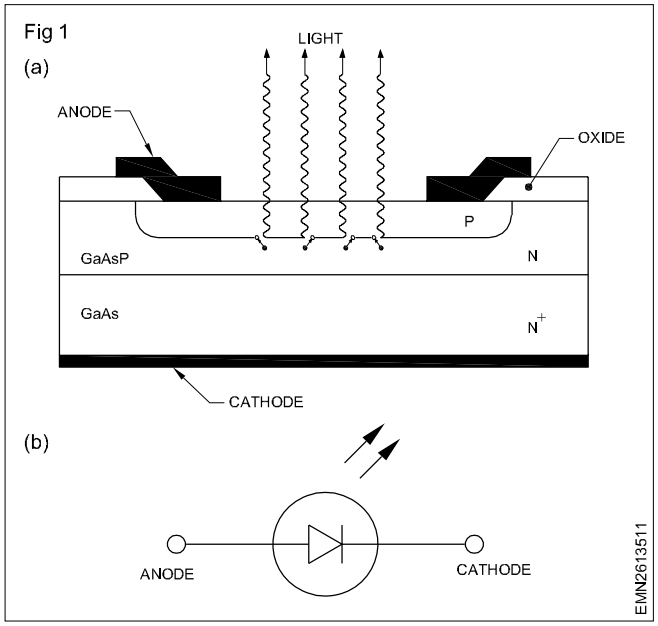
Principle of working of LEDs

LED is nothing but a type of diode. LEDs also posses the unique unidirectional property like general purpose diodes. But, the materials used in making LEDs are different; hence, their characteristics are different too. Therefore, it is very important to note that although LED is also a type of diode, it cannot and should not be used for the purpose of rectifying AC to DC.

Recall that a general purpose diode or a rectifier diode conducts when energy is supplied to the electrons (Si=0.7V, Ge=0.3V) to cross the barrier junction. Each electron, after acquiring the supplied extra energy, crosses the junction and falls into the hole on the P side of the junction while the electron recombines with a hole, the electron gives up the extra energy by it. This extra energy is dissipated in the form of heat and light. In general purpose diodes because the silicon material is not transparent(opaque), the light produced by the electrons does not escape to the outer environment. Hence, it is not visible. But LEDs are made using semi-transparent materials instead of silicon. Because the material used in making LEDs is semi-transparent, some of the light produced by the electrons escapes to the surface of the diode, and, hence, is visible as shown in Fig 1a.

LEDs are typically doped with gallium arsenic, gallium phosphate or gallium arseno-phosphate. Different dopes cause the LED to emit light of different colours(wavelengths) such as red, yellow, green, amber, or even invisible infrared light.

Fig 1



The schematic symbol of LED is shown in Fig 1b. The arrows are used to indicate that light is radiated from the device.

Types of LEDs

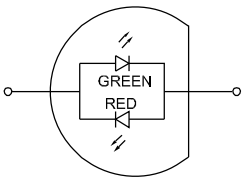
Single colour LEDs: Most of the commercially available and commonly used LEDs are single colour LEDs. These LEDs radiate one of the colours such as red, green, yellow or orange. Different coloured LEDs will have different forward voltages as given in the table below:

Colour of LED	Red	Orange	Yellow	Green
Typical Forward voltage drop	1.8V	2V	2.1V	2.2V

These typical forward voltage drops are at a typical LED forward current I_f = 20 mA

Two colour LEDs: These LEDs can give two colours. Actually, these are two LEDs put in a single package and connected as shown in Fig 2.

Fig 2

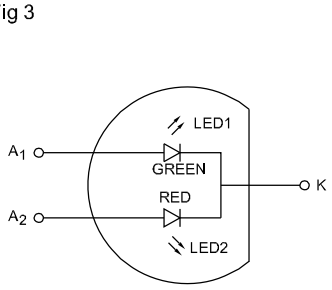


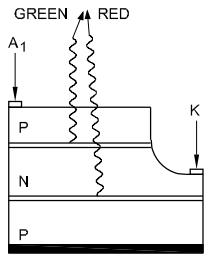
EMN2613512

In a two-colour LED, two LEDs are connected in inverse parallel, so that one of the colour is emitted when the LED is biased in one direction and the other colour is emitted when the LED is biased in the other direction. These LEDs are more expensive than the single colour LEDs. These LEDs are useful to indicate +ve, –ve polarities, GO-NOGO indication, null detection etc.

Multicolour LEDs: These are special types of LEDs which can emit more than two colours. These LEDs comprises of a green and a red LED mounted in a three-pin common cathode package as shown in Fig 3.

Fig 3





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This LED will emit green or red colour by turning ON only one LED at a time. This LED will emit orange or yellow by turning on the two LEDs with different current ratios as shown in the table given below:

Output colour	Red	Orange	Yellow	Green
LED-1 current	0	5mA	10mA	15mA
LED-2 current	15mA	3mA	2mA	0

Sizes and shapes of LEDs

LEDs are available commercially in different shapes and sizes to suit varied commercial applications. Fig 4 shows some of the most popular shapes and sizes of LEDs.

The light output of LED may be guided as point-source or diffused. The point-source LED provides a small point of light while the diffused type has a lens which diffuses the light into a wide angle viewing area.

Terminals of LEDs

Since LEDs are basically diodes, they have anode and cathode terminals/leads as in any general purpose diode. Fig 5 shows the methods to identify the terminals of a LED.

Mounting kits for LEDs

Special mounting kits, as shown in Fig 6, are available for fixing the LEDs on to the printed circuit boards and monitoring panels. These kits not only extend the life of the LED by way of protecting it from mechanical stress but also make the output of the LED clearly visible.

Fig 4

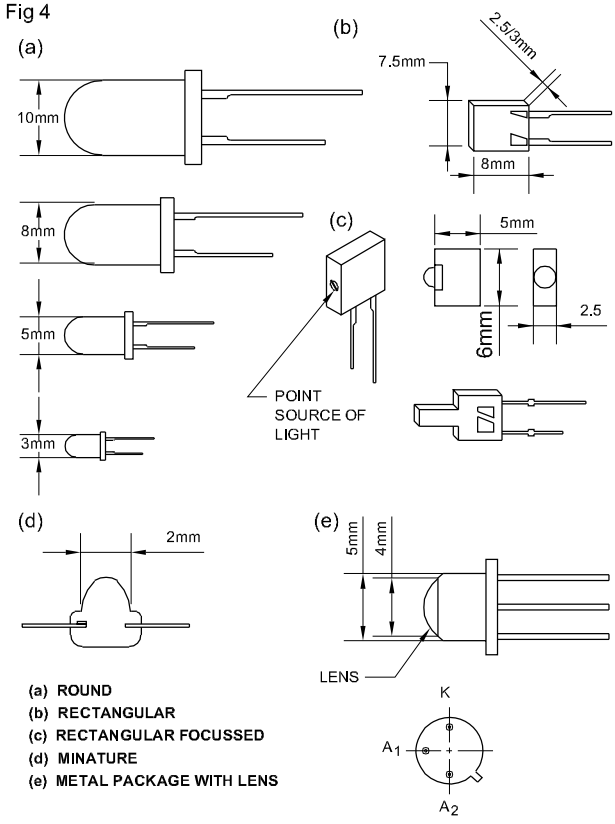

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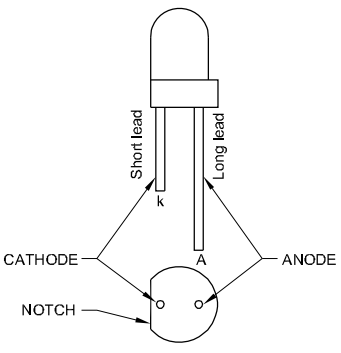
Fig 5



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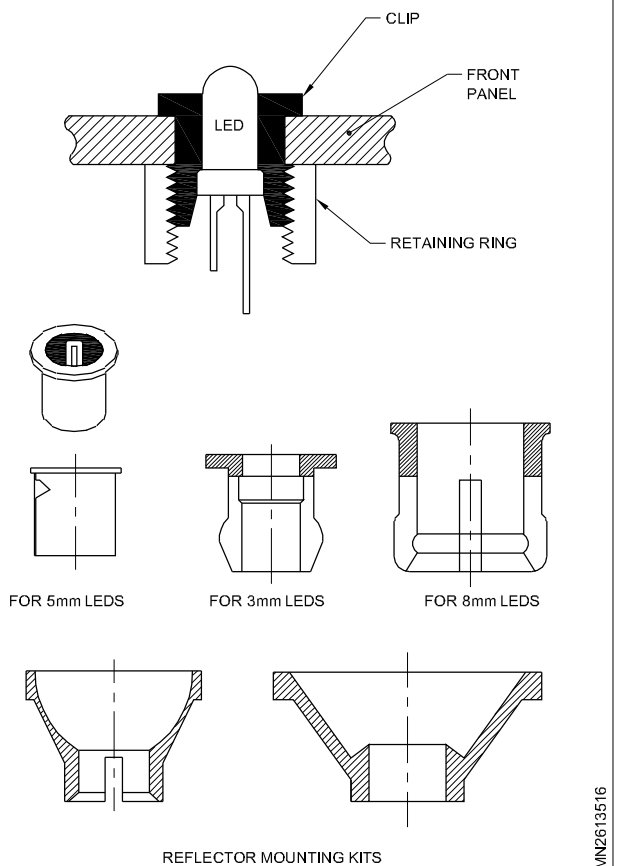
Testing LEDs using Ohmmeter

The anode and cathode terminals of a general purpose diode can be checked easily using an ohmmeter. But, in the case of LEDs, unlike general purpose diodes, the forward voltage of LED ranges from 1.5 to 3 volts (in some cases it is higher than 3 V), and a typical forward current ranges from 10 mA to more than 50mA. Because of this large forward voltage and current requirement of

the LEDs, it is not always possible to test the LEDs using an ohmmeter. The reason is, most of the portable type ohmmeters/multimeters use internal battery of not more than 3V for the operation of the meter. This voltage would have got reduced with constant use of the meter. Hence, when an LED is tested using an ohmmeter, the glow of the LED may be very dim or the LED may not glow at all depending on the condition of the battery inside the meter. Hence, the condition of an LED cannot be

Fig 6



confidently confirmed using a meter. However, since meter testing is the quickest, this can be used while purchasing an LED from the vendor where other equipments may not be available for testing.

Specifications of LEDs

Specifications sheet of a typical LED is given in the table below;

A Typical LED-specification sheet

(For: FairChild, FLV117 Red LED)

Characteristics	Min.	Typical	Max.
Forward current, I_f		20 mA	50 mA
Forward voltage, V_f		1.7V	3V
Reverse voltage, V_R		8V	
Axial luminous intensity	0.8 mcd	2 mcd	
Angle of half intensity		±20°	
Peak wave-length		665 nm	

From the specifications of a typical LED given above, the following important points are to be noted;

– The forward voltage drop of the LED is much higher (1.7V to 3V) than that of general purpose diodes.

– The reverse voltage that can be applied to the LED is much lower than in general purpose diodes.

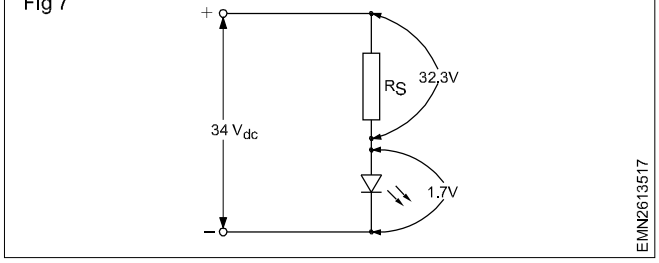
The above two important points confirm that, LEDs do not have the same characteristics as general purpose diodes.

In the typical LED specification, for instance, if 8 V or more is applied across the LED in the reverse biased polarity, the LED will be destroyed.

Example: What value of R_S is required, if a red colour LED is to be used in a circuit with a source of 34V dc.

Using the specifications of the red LED given in the table, it is clear beyond doubt that the LED cannot be connected across 34 volts supply directly (maximum Vf = 3V). Hence, as shown in Fig 7, a resistor is to be used in series with the LED which must drop to 32.3 volts if the voltage across LED should be 1.7 V.

Fig 7

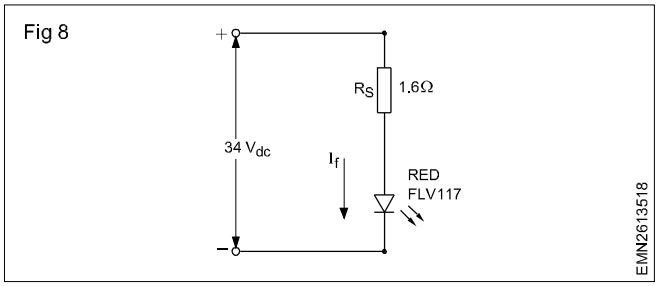


For the LED to give reasonably good light, the current through the LED has to be 20 mA, as indicated in the specifications sheet. So, the value of R_S must be,

$$R_S = \frac{V}{I} = \frac{32.3\ V}{0.02\ A} = 1615\ \Omega$$

Since the maximum permissible current through the LED is given as 50 mA, it is possible to use a standard 1.6KΩ resistor. This will make a current of 20.2 mA to flow through the LED which is well within the permitted maximum current rating. The LED can now be safely connected across a source voltage of 34 V as shown in Fig 8.

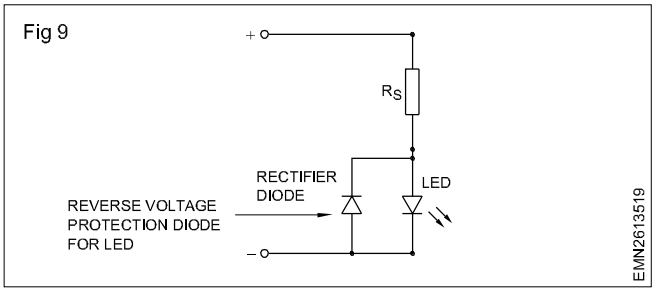
Fig 8



Note that, the maximum reverse voltage that can be applied for the chosen LED is only 8 volts. If accidentally a reverse voltage greater than 8 volts is applied, the LED will get damaged permanently. One way to protect the LED is by connecting a rectifier diode in parallel to the LED as shown in Fig 9.

In Fig 9, when a reverse voltage across the LED becomes

Fig 9



more than 0.7 V, the rectifier diode conducts with a forward voltage of 0.7 V. Thus the reverse voltage across the LED is restricted to 0.7 V which is much less than the maximum reverse voltage of 8 V of the LED, and hence the LED is safe.

IR LED

An infrared light-emitting diode (IRLED) is a special-purpose LED is shown in fig 10 that emits infrared signals. Specifically, it is a semiconductor device that releases infrared rays when exposed to electrical current.

Unlike LEDs that project parts of the visible light spectrum, IRLEDs are not used to provide lighting. They are, instead, most commonly used in various signal transfer systems, such as in remote controls for televisions, night-vision cameras and other devices. An IRLED beams light with data signals to control the device. IRLEDs are also used in security installations, cameras and other kinds of technologies. They are useful because of their low energy consumption and low heat generation.

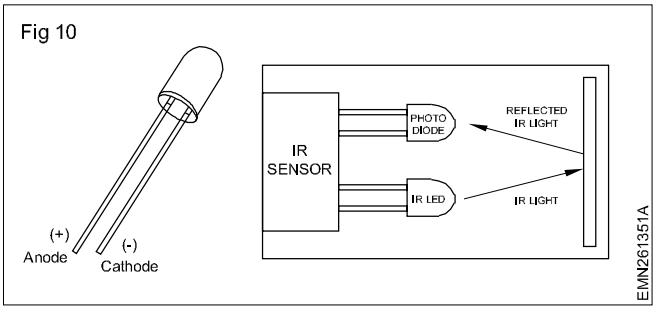
Infrared Sensor. An Infrared light emitting diode (**IR LED**) is a special purpose LED emitting **infrared** rays ranging 700 nm to 1 mm wavelength.

Different IR LEDs may produce infrared light of differing wavelengths, just like different LEDs produce light of different colors. IR LEDs are usually made of gallium arsenide or aluminum gallium arsenide. In complement with IR receivers, these are commonly used as sensors.

The appearance of IR LED is same as a common LED. Since the human eye cannot see the infrared radiations, it is not possible for a person to identify if an IR LED is working. A camera on a cell phone camera solves this problem. The IR rays from the IR LED in the circuit are shown in the camera.

Pin Diagram of IR LED

Fig 10



An IR LED is a type of diode or simple semiconductor. Electric current is allowed to flow in only one direction in diodes. As the current flows, electrons fall from one part of the diode into holes on another part. In order to fall into these holes, the electrons must shed energy in the form of photons, which produce light. It is necessary to modulate the emission from IR diode to use it in electronic application to prevent spurious triggering. Modulation makes the signal from IR LED stand out above the noise. Infrared diodes have a package that is opaque to visible light but transparent to infrared.

IR sensor An IR sensor is a device that detects IR radiation falling on it. Proximity sensors (used in touchscreen phones and edge avoiding robots), contrast sensors (used in line following robots) and obstruction counters/sensors (used for counting goods and in burglar alarms) are some applications involving IR sensors.

IR Sensor Principle of Working

An IR sensor consists of two parts, the emitter circuit and the receiver circuit. This is collectively known as a photo-coupler or an optocoupler.

The emitter is an IR LED and the detector is an IR photodiode. The IR phototdiode is sensitive to the IR light emitted by an IR LED. The photo-diode's resistance and output voltage change in proportion to the IR light received. This is the underlying working principle of the IR sensor.

The type of incidence can be direct incidence or indirect incidence. In direct incidence, the IR LED is placed in front of a photodiode with no obstacle in between. In indirect incidence, both the diodes are placed side by side with an opaque object in front of the sensor. The light from the IR LED hits the opaque surface and reflects back to the photodiode.

Proximity Sensors Proximity sensors employ reflective indirect incidence principle. The photodiode receives the radiation emitted by the IR LED once reflected back by the object. Closer the object, higher will be the intensity of the incident radiation on the photodiode. This intensity is converted to voltage to determine the distance. Proximity sensors find use in touchscreen phones, among other devices. The display is disabled during calls, so that even if the cheek makes contact with the touchscreen, there is no effect.

Line Follower Robots In line following robots, IR sensors detect the color of the surface underneath it and send a signal to the microcontroller or the main circuit which then takes decisions according to the algorithm set by the creator of the bot. Line followers employ reflective or non-reflective indirect incidence. The IR is reflected back to the module from the white surface around the black line. But IR radiation is absorbed completely by black color. There is no reflection of the IR radiation going back to the sensor module in black color.

Item Counter Item counter is implemented on the basis of direct incidence of radiation on the photodiode. Whenever an item obstructs the invisible line of IR radiation, the value of a stored variable in a computer/microcontroller is incremented. This is indicated by LEDs, seven segment displays and LCDs. Monitoring systems of large factories

use these counters for counting products on conveyor belts.

Burglar Alarm Direct incidence of radiation on the photodiode is applicable in burglar alarm circuit. The IR LED is fit on one side of the door frame and the photodiode on the other. The IR radiation emitted by the IR LED falls on the photodiode directly under normal circumstances. As soon as a person obstructs the IR path, the alarm goes off. This mechanism is used extensively in security systems and is replicated on a smaller scale for smaller objects, such as exhibits in an exhibition.

Laser diode

Like LEDs laser diodes are typical PN junction devices used under a forward-bias. The word LASER is an acronym for light amplification by stimulated emission of radiation. The use of laser is (becoming increasing common) in medical equipment used in surgery and in consumer products like compact disk (CD) players, laser printers, hologram scanners etc.

(a) Construction

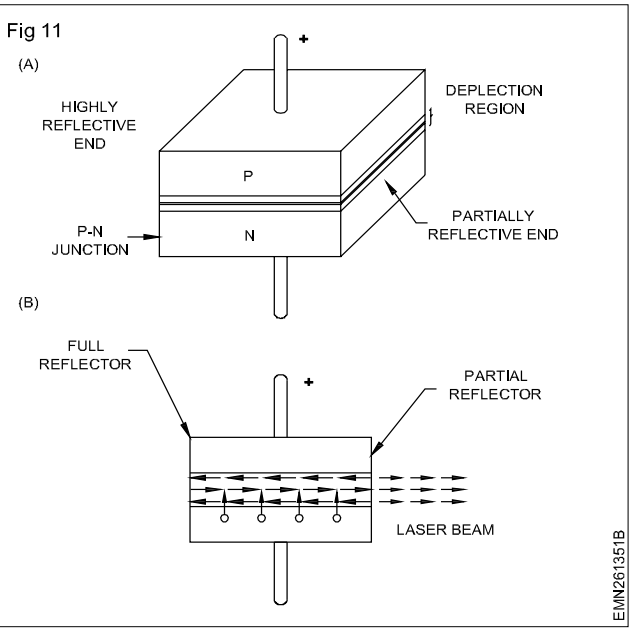
Broadly speaking, the laser diode structure can be divided into two categories:

1 **Surface-emitting laser diodes:** These laser diodes emit light in a direction perpendicular to the PN junction plane.

2 **Edge-emitting laser diodes:** These laser diodes emit light in a direction parallel to the PN junction plane.

Fig.11a shows the structure of an edge-emitting laser diode. This type of structure is called Fabry-Perot type laser. As seen from the figure, a P-N junction is formed by two layers of doped gallium arsenide (GaAs). The length of the PN junction bears a precise relationship with the wave length of the light to be emitted. As seen, there is a highly reflective surface at one end of the junction and a partially reflective surface at the other end. External leads provide the anode and cathode connections.

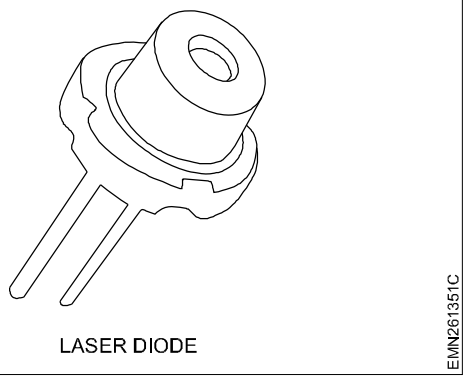
Fig 11



(b) Theory

When the PN junction is forward biased by an external voltage source, electrons move across the junction and usual recombination occurs in the depletion region which results in the production of photons. As forward current is increased, more photons are produced which drift at random in the depletion region. Some of these photons strike the reflective surface perpendicularly. These reflected photons enter the depletion region, strike other atoms and release more photons. All these photons move back and forth between the two reflective surfaces. Fig.10b. The photon activity becomes so intense that at some point, a strong beam of laser light comes out of the partially reflective surface of the diode.

Fig 12



(c) Unique characteristics of laser light

The beam of laser light produced by the diode has the following unique characteristics

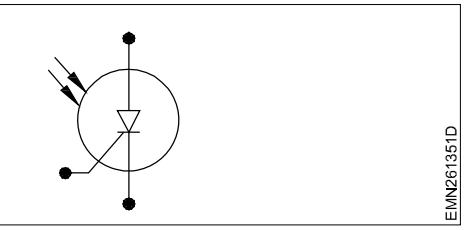
1 It is coherent i.e there is no path difference between the waves comprising the beam;

2 It is monochromatic i.e. it consists of one wavelength and hence one colour only.

3 It is collimated i.e emitted light waves travel parallel to each other.

Laser diodes have a threshold level of current above which the laser action occurs but below which the laser diode behaves like a LED emitting incoherent light. The schematic symbol of a laser diode is similar to that of LED. Incidentally, a filter or lens is necessary to view the laser beam.

Fig 13



d) Applications

Laser diodes are used in variety of applications ranging from medical equipment used in surgery to consumer products like optical disk equipment, laser printers, hologram scanners etc. Laser diodes emitting visible light are used as pointers. Those emitting visible and infrared light are used to measure range (or distance). The laser diodes are also widely used in parallel processing of

information and in parallel interconnections between computers. Some of these applications are discussed in the following articles.

Printers using laser diodes

There are two types of optical sources usually used in printers; (1) laser diodes and (2) LED arrays. The printers using laser diodes are called laser beam printers (or simply laser printers). These are one of the most attractive type of equipment in office automation in today's world. Words and figures can be printed rapidly and clearly more easily by a laser printer than by other types of printers.

Hologram scanners

An infrared light -emitting diode (LED) is a type of electronic device that emits infrared light not visible to the marked eye. An infrared (IR) LED operates like a regular LED, but may use different materials to produce infrared light. This infrared light may be used for a remote control, to transfer data between devices, to provide illumination for night vision equipment, or for a variety of other purposes.

An infrared LED is like all LEDs a type of diode, or simple semiconductor. Diodes are designed so that electric current can only flow in one direction. As the current flows, electrons fall from one part of the diode into holes on another part. In order to fall into these holes, the electrons must shed energy in the form of photons, which produce light.

Infrared emitting diode infrared light working principle and characteristics

TV monitoring systems engineering in the past rarely used infrared light, but because of today's society not only increase the crime rate, infrared light surveillance in a more prominent role, not only the treasury, oil depots, armories, books library, the cultural relics department, prison and other important departments, but also in the general monitoring system have been adopted. Even residential area television monitoring project has also applied the IR IP camera. This shows that people on television monitoring system engineering requirements increasingly standardized, higher and higher. On the important places are increasingly demanding to do 24 hours of continuous monitoring.

Infrared light into its mechanism of semiconductor infrared radiation emitting solid (infrared emitting diode) infrared light and infrared light two kinds of thermal radiation, most of the infrared infrared IP camera are used as a light-emitting diode LED IR infrared security surveillance camera's main material.

Infrared emitting diode infrared light, the principle and characteristics are as follows: the matrix of infrared light - emitting diode light. Infrared emission diode by the infrared radiation efficiency of the material commonly gallium arsenide GaAs) made of a PN junction, applied to the PN junction forward bias injection current excitation infrared light. Spectral power distribution center wavelength 830~950nm, half-peak bandwidth of about 40nm or so, it is the narrow distribution as ordinary CCD monochrome camera can be a range of feelings. Its biggest advantage is that you can completely red storm, (using 940~950nm wavelength infrared tube) or only weak red storm (red storm is a visible red light) and long life.

Infrared light - emitting diodes transmit power with irradiance $\mu W/m^2$ representation. In general, the infrared radiation power and forward current is proportional to but near the maximum forward current rating, the temperature of the device due to the current heat consumption rises, the light emission power down. Infrared diode current is too small, it will affect the radiation power of the play, but the work current is too general affect their life and even the infrared diode burned. Industry's popular in video surveillance camera inside the built-in cooling system that allows the camera steady work longer.

Light Dependant Resistor (LDR)

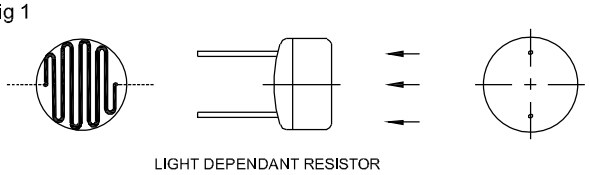
Objectives : At the end of this lesson you shall be able to
- **explain the working principle of LDR.**

Light Dependant Resistor

The name itself tells us what the component does. "photo" is for light "resistor" is to resist the flow of current.

Photoresistors, also known as light dependent resistor (LDR), Cadmium Sulfide cells (CDS cells), photoconductor and sometimes simply photocells are a type of transducer which converts energy from one form to another where one of the known forms is electrical energy. To keep things simple, we will refer to it as photoresistor. Resistance in a photoresistor inversely varies with the amount of light it is exposed to. Bright light=Less resistance and low light=more resistance. These sensors are used to make light sensitive devices and are more often found in street lights, cheap toys, outdoor clocks etc., if you have ever wondered how a street light turns on in the night and switches off in the

Fig 1

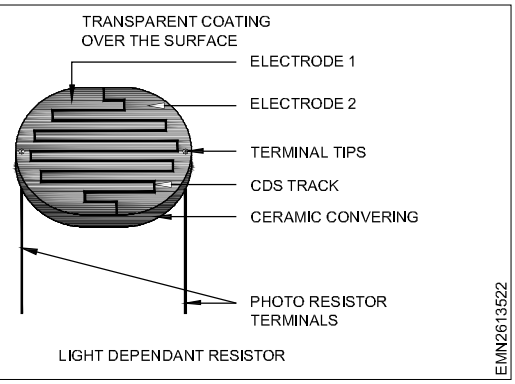


day, you will be surprised to find a cheap photoresistor circuitry inside it.

Phototransistors/photodiodes/photovoltaic cells are altogether different and do not confuse that with these photoresistors.

Cadmium sulfide is often used to make these components due to its low cost. Other materials such as Lead sulfide, Indium antimonide and Lead Selenide are also used for high end requirements.

Fig 2



LIGHT DEPENDANT RESISTOR

How do they work?

Working principle of a photoresistor is relatively simple. If you have already read electricity basics, you know that electricity is nothing but movement of electrons within a material. Conductors have low resistance and insulators have high resistance. The third category is the semiconductors which stand between a conductor and an insulator. Photoresistor is made of one such semiconductor with very high resistance with only a few free electrons. When light falls on this material, photons from light is absorbed by these materials and energy is transferred to electrons which break up resulting in lower resistance and higher conductivity. The resistance in low light to bright light it results in only a few hundred ohms. When exposed to low light, the resistance in a photoresistor can be several mega-ohms (5-20M** dependent on the type & size) and in bright light it results in only a few hundred ohms. Also photoresistors are non-polarized, meaning it can be connected either way in a circuit.

You can easily connect the leads with a multimeter on resistance mode and check resistance of your photoresistor. Face it towards bright light and check the resistance. Now place your hand or cover it up with a black tape and check the resistance again. You see that the resistance drastically increases once you cover the photoresistor.

Advantages

1 Cheap and will not make a hole in your pocket if you spoil few

2 Commonly found in most robot hobby shops

3 Available in different sizes with different specification

4 Easy to design and implement them in a circuitry.

Drawbacks

1 Highly inaccurate. Each one behaves differently than the other. If the first one has a resistance of 150Ω in bright light, second one can have 500Ω of resistance in the same light.

2 They cannot be used to determine precise light levels.

3 Very slow for sensitive applications. If you put a LDR in a speeding robot and tell it to stop at an obstacle, you end up seeing your robot crash.

Photoresistor applications

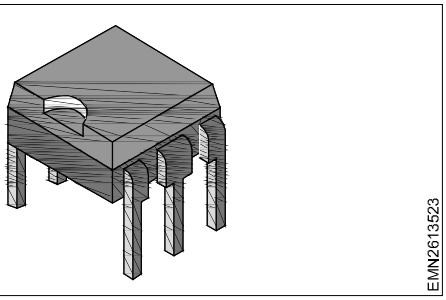
The photoresistor or light dependent resistor is attractive in many electronic circuit designs because of its low cost, simple structure and rugged features. While it may not have some of the features of the photo -resistor is widely used in circuits such as photographic meters, flame or smoke detectors, burglar, card readers, controls for street lighting and many others.

The properties of photoresistors can vary quite widely dependent upon the type of material used. Some have very long time constants, for example it is therefore necessary to carefully choose the type of photoresistor for any given circuit or application.

Generally transformers not only provide higher or lower voltage differences between their primary and secondary windings, but they also provide "electrical isolation" between the higher voltages on the primary side and the lower voltage on the secondary side.

Thus transformers isolate the primary input voltage from the secondary output voltage using electromagnetic coupling by means of a magnetic flux, circulating within the iron laminated core. But we can also provide electrical isolation between an input source and an output load using just light by using a very common and valuable electronic component called an Optocoupler.

Fig 3



An Optocoupler, also known as an Opto-isolator or Photo-coupler, is an electronic components that interconnects two separate electrical circuits by means of a light sensitive optical interface.

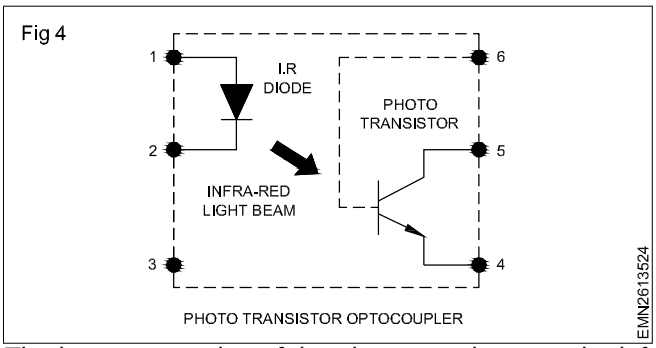
The basic design of an Optocoupler consists of an LED that produces infra-red light and a semiconductor photo-sensitive device that is used to detect the emitted infra-red beam. Both the LED and photo sensitive device are enclosed in a light - tight body or package with metal legs for the electrical connections as shown.

An optocoupler or opto-isolator consists of a light emitter, the LED and a light sensitive receiver which can be a single photo-diode, photo-transistor, photo-resistor, photo-SCR or a photo TRIAC and the basic operation of an optocoupler is very simple to understand.

Assume a photo-transistor device as shown. Current from the source signal passes through the input LED which emits an infra-red light whose intensity is proportional to the electrical signal.

This emitted light falls upon the base of the photo-transistor,

causing it to switch-ON and conduct in a similar way to a normal bipolar transistor.



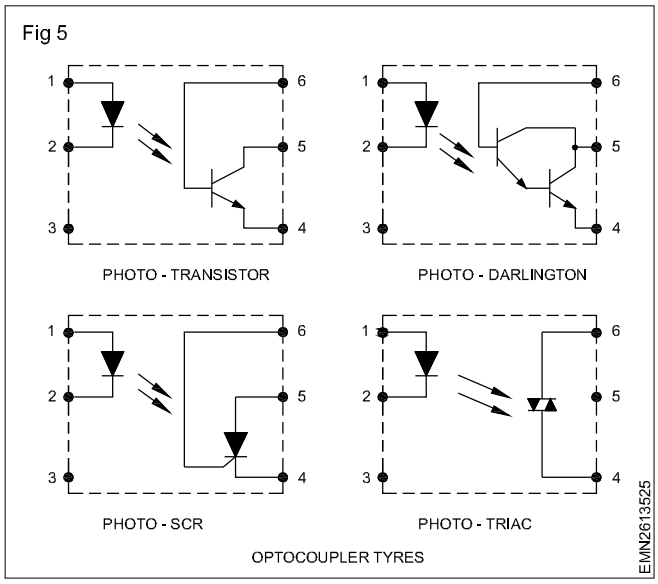
The base connection of the photo-transistor can be left open for maximum sensitivity or connected to ground via a suitable external resistor to control the switching sensitivity making it more stable.

When the current flowing through the LED is interrupted, the infra-red emitted light is cut-off causing the photo transistor to cases conducting. The photo-transistor can be used to switch current in the output circuit. The spectral response of the LED and the photo-sensitive device are closely matched being separated by a transparent medium such as glass, plastic or air. Since there is no direct electrical connection between the input and output of an optocoupler, electrical isolation upto 10kV is achieved.

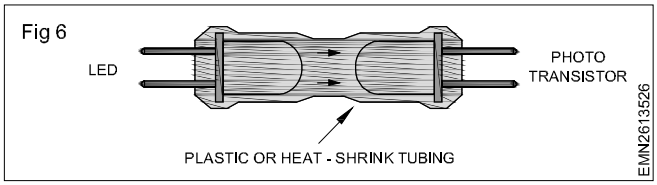
Optocouplers are available in four general types, each one having an infra-red LED source but with different photo-sensitive devices. The four optocouplers are classed the photo transistor, photo-darlington, photo-SCr and photot-Triac as shown in below.

Optocoupler types

The photo-transistor and photo-darlington devices are mainly for use in DC circuits while the photo-SCR and photo-Triac allow AC powered circuits to be controlled. There are many other kinds of source - sensor combinations, such as LED - photodiode, LED-LASER, lamp photoresistor pairs, reflective and slotted optocouplers.



Simple homemade optocouplers can be constructed by using individual components. An LED and a photo-transistor are inserted into a rigid plastic tube or encased in heat-shrinkable tubing as shown. The advantage of this home-made optocoupler is that tubing can be cut to any length you want and even bent around corners. Obviously, tubing with a reflective inner would be more efficient than dark black tubing.



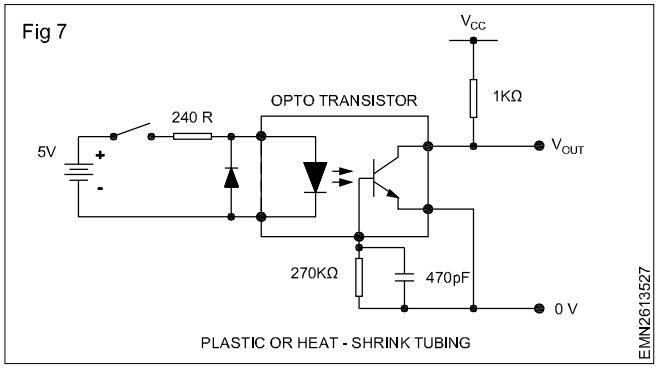
Home-made optocoupler

Optocoupler applications

Optocouplers and opto-isolators can be used on their own, or to switch a range of other larger electronic devices such as transistors and TRIACs providing the required electrical isolation between a lower voltage control signal and the higher voltage or current output signal. Common applications for optocouplers include microprocessor input/output switching, DC and AC power control, PC communications, signal isolation and power supply regulation which suffer from current ground loops, etc. The electrical signal being transmitted can be either analogue (linear) or digital (pulses).

In this application, the optocoupler is used to detect the operation of the switch or another type of digital input signal. This is useful if the switch or signal being detected is within an electrically noisy environment. The output can be used to operate an external circuit, light or as an input to a PC or microprocessor.

An optotransistor DC Switch



As well as detecting DC signals and data, Opto-Triac isolators are also available which allow AC powered equipment and mains lamps to be controlled. Opto - coupled Triacs such as the MOC 3020, have voltage ratings of about 400 volts making them ideal for direct mains connection and a maximum current of about 100mA. For higher powered loads, the opto-Triac may be used to provide the gate pulse to another larger triac via a current limiting resistor as shown.

Triac optocoupler application

This type of optocoupler configuration forms the basis of

a very simple solid state relay application which can be used to control any AC mains powered load such as lamps and motors. Also unlike a thyristor (SCR), a Triac is capable of conducting in both halves of the mains AC cycle with zero-crossing detection.

Optocouplers and Opto-isolators are great electronic devices that allow devices such as power transistors and Triacs to be controlled from a PCs output port, switch or low voltage data signal. Their main advantages is the high electrical isolation between the input and output allowing relatively small signals to control much large voltages and currents.

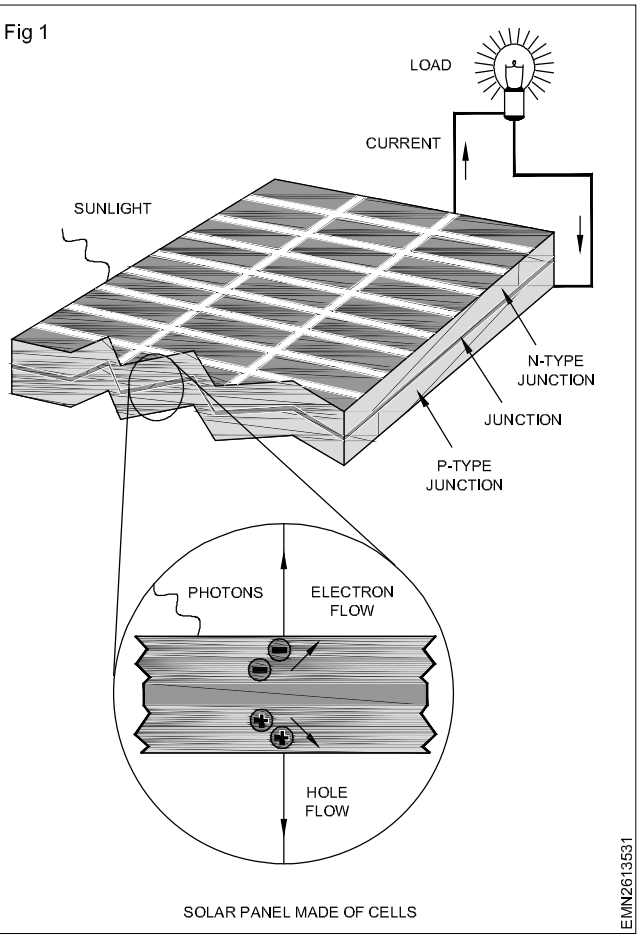
An optocoupler can be used with both DC and AC signals with optocouplers utilizing a SCR (thyristor) or Triac as the photo-detecting device are primarily designed for AC power control applications. The main advantage of photo-SCRs and photo-Triacs is the complete isolation from any noise or voltage spikes present on the AC power supply line as well as zero crossing detection of the sinusoidal waveform which reduces switching and inrush currents protecting any power semiconductors used from thermal stress and shock.

Photovoltaic Cell

Objectives : At the end of this lesson you shall be able to
- **explain the working principle of solar cells / photovoltaic cell.**

How a solar cell makes electricity?

Fig 1



A **solar cell** is also called as **photovoltaic cell**

Under the sun, a **solar cell** or **p**hoto **v**oltaic cell (PV cell) acts as a photosensitive diode that instantaneously converts light - but not heat - into electricity. Some PV cells can also convert infrared (IR) or ultraviolet (UV) radiation into DC electricity.

Cell Layers

A top, phosphorus - diffused silicon layer carries free electrons with negative charges. A thicker, boron doped bottom layer contains holes, or absences of electrons, that also can move freely.

Sun Activation

1 Photons bombard and penetrate the cell

2 They activate electrons, knocking them loose in both silicon layers.

3 Some electrons in the bottom layer sling -shot to the top of the cell.

4 These electrons flow into metal contacts as electricity, moving into a circuit throughout a 60cell module.

5 Electrons flow back into the cell via a solid contact layer at the bottom creating a closed loop or circuit and the bulb glows.

Powering homes and businesses with solar

Current leaving a module, or array of modules, passes through a wire conduit leading to an inverter. This device, about the shape of a waffle iron, inverts direct current, which flows with a fixed current and voltage, into alternating current, which flows with oscillating current and voltage. Appliances worldwide operate on AC. Fromthe inverter, the solar generated power feeds into circuitry of a household, business or power plant and onto the region's electrical grid. A remote, or independent, power system also can form a self-contained circuit without connecting to the grid. The off-grid system, however, requires batteries to store power for times, such as night, when modules do not capture enough light energy from the sun.

Large sets of PV cells can be connected together to form solar modules, arrays, or panels.

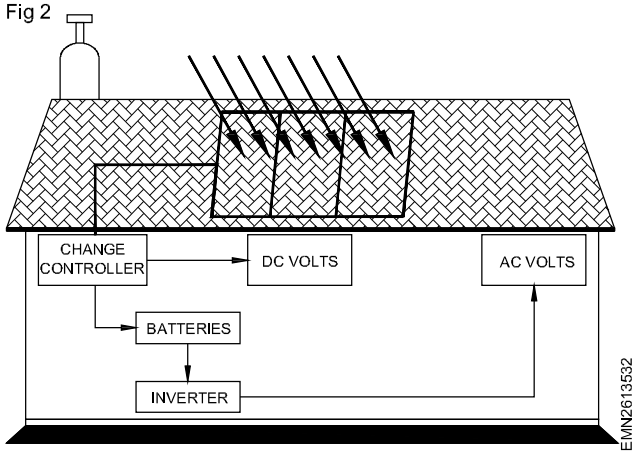
A solar panel turns the sun's light into electricity! We see electricity at work every day. For instance, when you turn on a lamp, electrons move through the cord and light up the bulb. That flow of electrons is called electricity.

One solar panel is made up of many small cells. Each of these cells uses light to make electrons move. The cell is made up of two different layers that are attached together.

The first layer is loaded with electrons, so the electrons are ready to jump from this layer to the second layer. That second layer has had some electrons taken away, so it is ready to take in more electrons.

When the light hits an electron in the first layer, the electron jumps to the second layer. That electron makes another electron move, which makes another electron move, and so on. It was the sunlight that started the flow of electrons, or electricity.

Fig 2



Photodiodes and Phototransistors

Objectives: At the end of this lesson you shall be able to

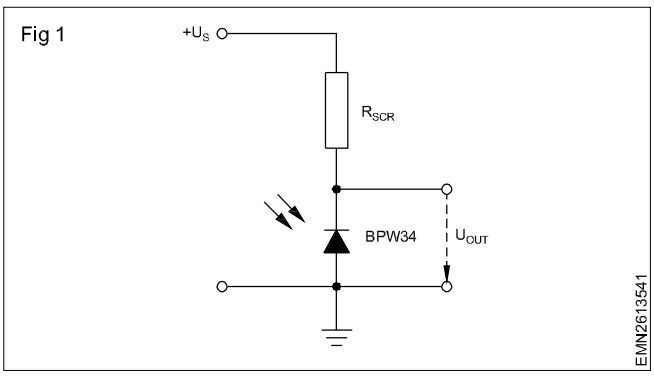
- **explain working of photodiode**
- **explain the advantages of PIN photodiode**
- **list the application of photodiodes**
- **explain working of photodiode**
- **explain the working of a light controlled switch using photo transistor.**

PHOTODIODES

P-N Photo diodes

Photodiodes are produced by silicon techniques. Photodiodes are operated in the reverse direction. A supply voltage and a series resistor are therefore required to operate photodiodes. The basic circuit for the operation of photodiodes is shown in Fig.1

Fig 1



When no light is incident on the photodiode, a reverse current flows through the p-n junction, as it does in any normal semiconductor diode, but in photodiodes it is usually referred to as the "dark current" I_{Ro}.

When light strikes the p-n junction, crystal bonds are broken as a result of the supply of energy. Mobile charge-carrier pairs are produced, which immediately migrate as a result of the electric field present. The holes travel towards the p-layer and the electrons towards the n-layer. As a result of illumination, an additional photocurrent I'_{photo} occurs, which increases linearly with the illuminance. This photocurrent is superimposed as a reverse current on the relatively small dark current, so that for the total photocurrent occurring with illumination, the following applies:

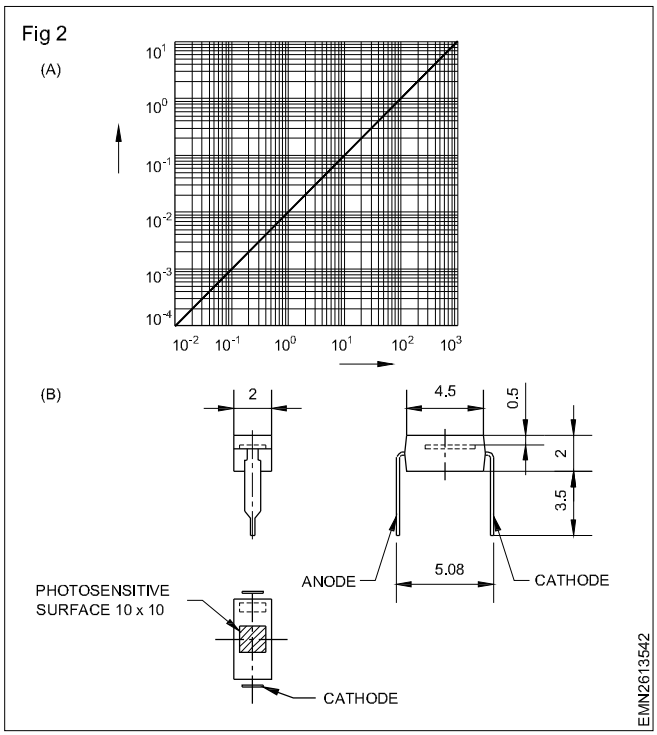
$I_{photo} = I_{Ro} + I'_{photo}$

Since I_{Ro} is far smaller than I'_{photo} then:

$I_{photo} = I'_{photo}$

The rise in I_{photo} is almost linear. Photodiodes are therefore particularly suitable for the accurate measurement of illuminance. Physical appearance and dimensions of a typical photodiode BPW 32 is shown in Fig 2.

Fig 2



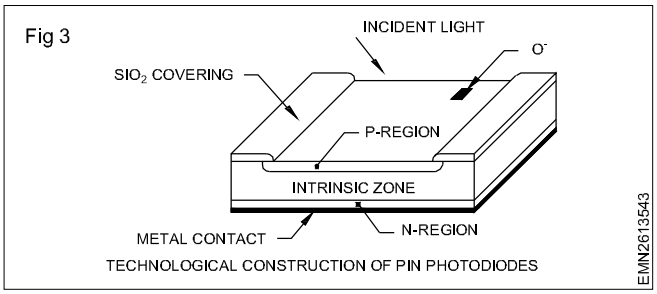
PIN Photo diodes

PIN photodiodes were developed to overcome the drawbacks of p-n photodiodes. The letters PIN indicate the zone

sequence as given below;

P-layer/Intrinsic-layer/N-layer

A typical internal construction of a PIN photodiode is shown in Fig 3.



The advantages of PIN photodiodes are;

– high sensitivity in the infrared range

– short switching times,

because of which, they are extensively used in remote control using modulated infrared light.

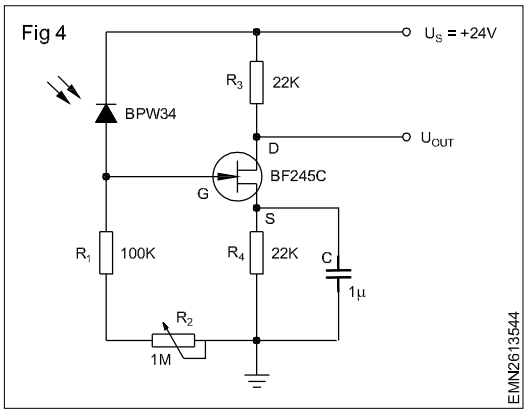
In operation they are similar to p-n photo diodes as shown in Fig 1.

Typical application of Photodiodes

Because of the very small photocurrent, photodiodes are generally used with an amplifier as shown in Fig 4. Amplifier stages with FET(Field Effect Transistor) are usually used with photodiodes because of the high input resistance of FET.

NOTE: Field Effect Transistors well known as FET is another type of transistor. Details of FET is discussed in lessons to follow.

Circuit diagram of a simple Light controlled amplifier is shown in Fig 5. This circuit uses a single FET for amplifying the output of the photodiode connected in series with a resistor.



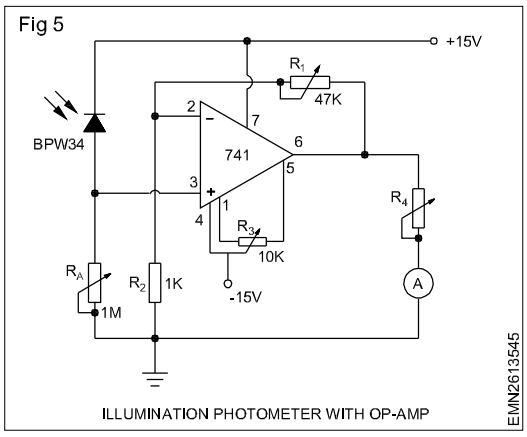
The working point of the FET can be adjusted with trimmer R_2. As the illumination on the photo diode increases, the negative gate is reduced and therefore V_{out} reduces. The same value of R_3 and R_4 are chosen to ensure linear relationship between I_{photo} and V_{out} over a wide range. Thus this photoamplifer works satisfactorily not only for very slow changes in illumination but also with alternating light.

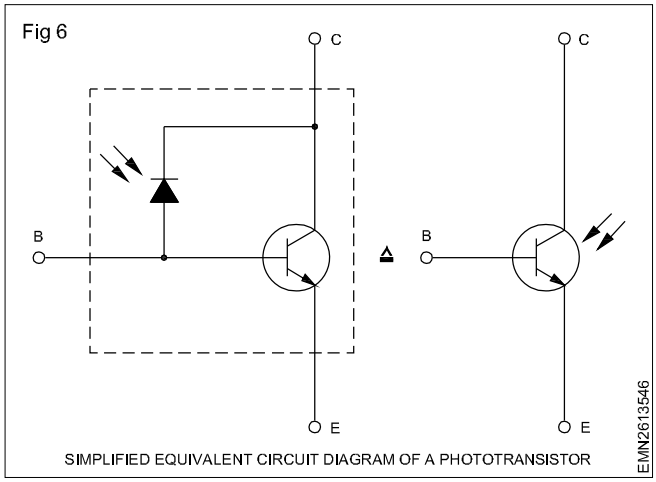
Illumination Photometer using photodiode and Opamp

An illumination Photometer with an op-amp as an amplifier is shown in Fig 5. The output of the photo sensor follows the illuminance linearly, which may be in the range between 0.05 lx and 5000 lx, with a sensitivity of 5µA/lx. The sensor has the type designation TFA 1001W and is intended for use in video cameras and optical instruments.

PHOTOTRANSISTOR

Both in the construction and in their mode of operation, phototransistor's can be thought of as a combination of a photodiode and a normal bipolar transistor. The simplified equivalent circuit diagram of a phototransistor is shown in Fig 6.





Without illumination, only a very small dark current I_{Ro} flows through the photodiode. This dark current, at the same time is the base current of the transistor. The following is then obtained for the dark current I_{Co} of the transistor,

$I_{Co} = B \times (I_{CBo} + I_{Ro})$,

Where,

I_{CBo}, is the reverse current of the collector/base diode and B is the current gain of the transistor.

When the photodiode is illuminated, a photocurrent I_{photo} flows, which is amplified by the current gain B and is superimposed on the dark current.

Therefore, the collector current of the phototransistor is,

$I_C = I_{Co} + B \times I_{photo}$

Since the dark current I_{Co} is much less than $B \times I_{photo}$, I_{Co} can generally be neglected, so in practice,

I_C approximately = $B \times I_{photo}$

Advantage of Phototransistors over Photodiodes

Advantages of phototransistors over photodiodes are,

– their considerably greater sensitivity and

– the illuminance-dependent collector current IC, which is increased by a factor B.

Type and availability

Phototransistors are produced with and without external base terminals. If no base terminal exists, the collector current is exclusively controlled by the change in the illuminance. It is then no longer possible to specify a working point. Such phototransistors are therefore usually used only as light-sensitive switches.

Example of phototransistors without an external base terminal;

Type number BPX81

Limiting data for BPX81:

U_{CEmax} = 32V i_{Cmax} = 50 mA

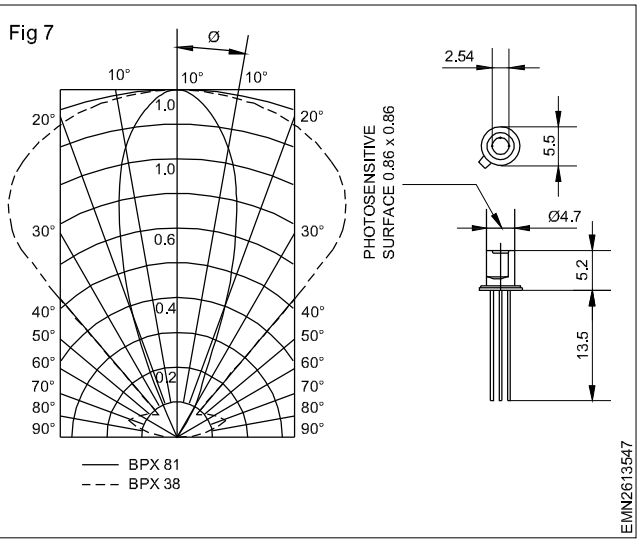
V_{Jmax} = 90°C P_{tot} = 100mW

R_{thJA} = 750 K/W

BPX 81 is used both for visible and infrared light because of its wide spectral sensitivity. Fig 7 shows the BPX81 phototransistor with component dimensions.

BPX 38 phototransistor belongs to the group of phototransistors with external base terminal. The aperture angle of BPX 38 is larger than BPX 81. Therefore BPX 81 has better directional characteristics compared to BPC 38. Fig 7 shows the typical construction of BPX 38 phototransistor.

Fig 7



BPX 38 is available in four sensitivity groups. The data is given in the table below;

Group	II	III	IV	V
Photocurrent I_{photo} at E_e=0.5mW/cm^2	0.2 to 0.4 mA	0.32 to 0.63mA	0.5 to 1.0mA	0.8 to 1.6mA
B	150	240	350	-

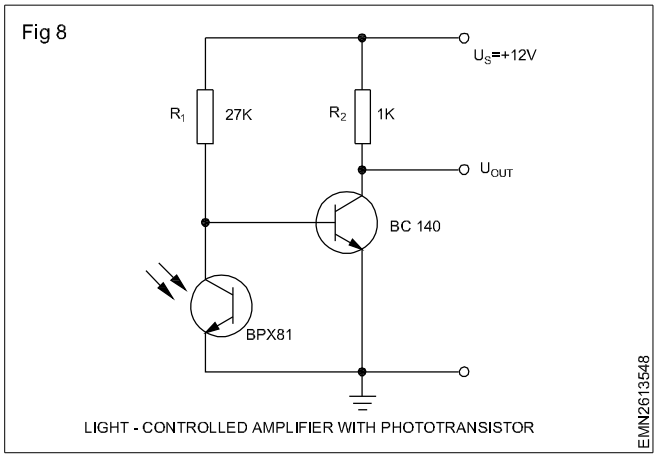
Typical applications

Of the numerous possible applications of light-sensitive phototransistors, two very simple circuits applications are given below;

Light controlled amplifier with phototransistor

Together with the phototransistor, resistor R1 again forms a light-sensitive voltage divider. The phototransistor is thus operated like a photodiode with a greater sensitivity and heavier photocurrent. It is therefore possible to drive a low-power transistor,such as BC140 directly by the collector of the phototransistor as shown in Fig 8.

Fig 8

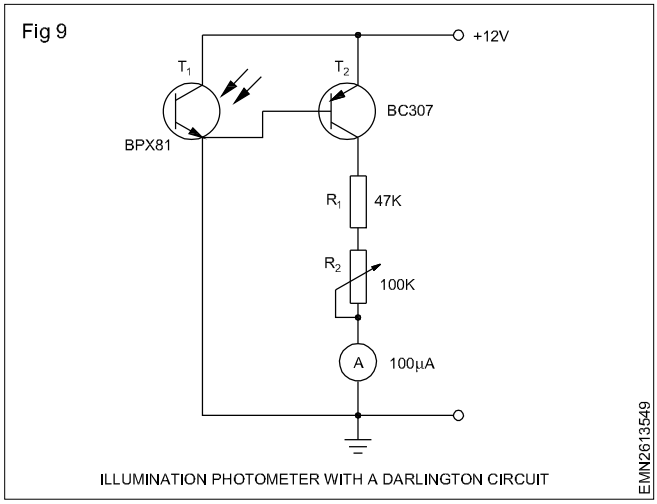


LIGHT - CONTROLLED AMPLIFIER WITH PHOTOTRANSISTOR

Illumination Photometer

Fig 9 shows a circuit with a roughly linear characteristic $I_e = f(E_e)$ as an illumination photometer for measuring illuminance. It works with a Darlington circuit, consisting of an npn phototransistor BPX81 and a pnp transistor BC307.

Fig 9



ILLUMINATION PHOTOMETER WITH A DARLINGTON CIRCUIT

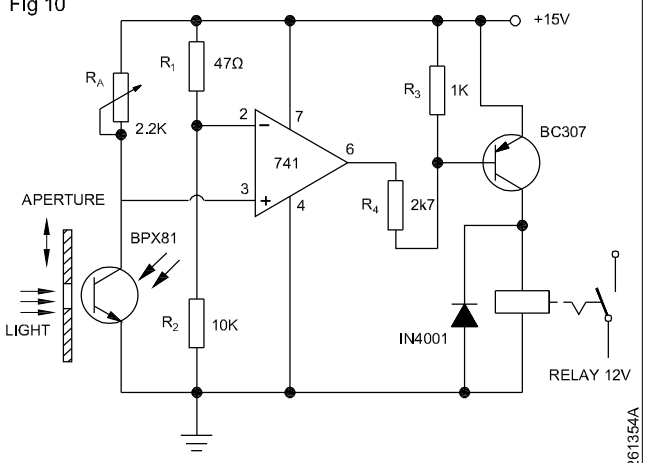
Light controlled switch using phototransistor

Fig 10 shows a circuit which evaluates the states;

"Phototransistor illuminated" or "Phototransistor not illuminated"

The Opam in the circuit works as a comparator. It is used as a signal comparator cum signal amplifier. When the phototransistor gets illuminated, the voltage at the -ve input of the opamp is higher than that at the +ve input and the output V_{out} is at 0 volts because of the operation with only one supply voltage. When the phototransistor is not illuminated, the conditions at the inputs of the opamp are reversed and the output voltage V_{out} is approximately 24 volts.

Fig 10



LIGHT-CONTROLLED SWITCHING AMPLIFIER

Application of opto electronic devices

Objectives : At the end of this lesson you shall be able to

- **explain the meaning and application of optoelectronics**
- **explain the working of a basic optical receiver**
- **explain the working of a optocoupler**
- **explain the working of a LASCR**
- **explain the principle of Optical fibres**
- **explain the working principles of opto- isolator.**

Optoelectronics is the integration of electronics, optics and light to more effectively and economically control an electromechanical operation, transfer information or make measurements.

The term light means both visible and invisible. Visible light is seen by the human eye whereas, infrared light is below the range of human perception. Optoelectronic devices include light emitters, photodetectors or sensors, optic fibers, visual displays and a variety of fittings to link computers, telephones and televisions.

Optoelectronic components have proved superior to mechanical sensing and switching as they cost less, they are smaller, light in weight, they are faster and have longer life.

Optocomponents

Optocomponents fall into two general categories-light emitters and light sensors. Light emitters and sensors can be further divided into devices that operate in the visible light range and those that operate in the infrared region.

A further differentiation in the various devices involves their physical structure. Different-sized holders have been designed for different devices.

Light sensors are divided according to their speed of operation, frequency of operation and ability to provide amplification. A further division relates to whether the light emitter and sensor are an integral part of one holder such as in the optocoupler or optoisolator.

The specific application will determine whether a photodiode, phototransistor, photo-Darlington or Schmitt trigger device is necessary. In digital applications, for example high-speed devices are generally required.

Optoisolators and optocouplers are finding wide application in power control devices, where they are used in place of relays.

Photoresistor

The photoresistor is the basic light sensing component. It is generally made of either cadmium Sulfide (CdS) or cadmium selenide (CdSe). The devices are made by the deposition of a layer of the semiconductor material on a substrate of ceramic or silicon. A clear coating of glass or plastic, to form a lens can be used to focus the light. The semiconductor material in a dark state has few free electrons however when light (photons) irradiates the cell's surface, the electron flow increases and resistivity decreases. A dark cell may have a resistance of 30 to 50 MΩ, where as an illuminated cell's resistance may drop to under 5 kΩ. Dark-to-light resistance ratios of 10,000/1 are quite common. Accompanying the resistance change is also a change in response time. Photoresistors does not respond instantaneously to the influx of light.

Photoresistors are sensitive to different wave lenghts. The CdS photoresistor peaks in the region of 0.60μm (6000 A). CdSe photoresistors peaks in the region of 0.7 to 0.75 μm. Both peaks above the visible light response.

Photoresistors are also manufactured from selenium, germanium and silicon. The material that is used determines the sentivity and response time of the sensor.

Geometric patterns in the semiconductor layer can also affect the sensitivity of photoresistors. Zigzag or interleaved

patterns provide greater surface areas but a lower operating voltage. The photoresistor can be used as a potentiometer for the biasing of oscillators or amplifiers.

Photovoltaic cell

It is PN junction diode. The P material is often made of selenium or silicon and the N material is cadmium or silicon.

Light irradiating the solar cell (junction area) reduces its energy band and causes electrons to move toward the N-type material while the holes move toward the P material. Externally, a dc potential can be measured that is in the range of 0.6 to 0.7V, with the P-material terminal being positive and the N material being negative.

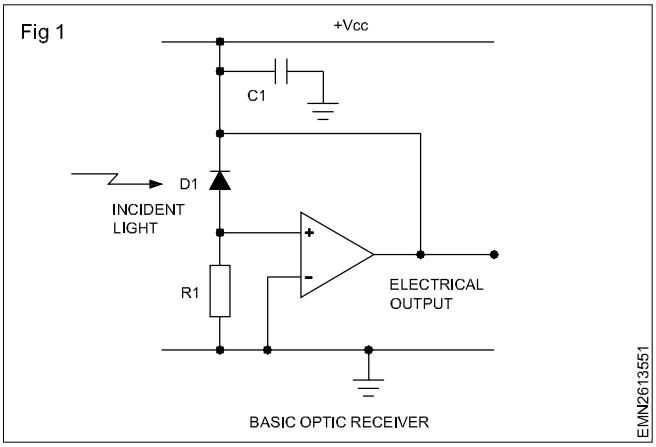
The surface area determines the current supply capability. Cells can be connected in series to increase the total voltage or in parallel to increase the total current.

The photovoltaic cell has its peak response in the range of 0.5 μm. Cells made from indium antimonide operate in the near-infrared region. Most solar cells are very active in the visible light spectrum.

Optical receivers

An optical receiver shown in Fig 1 consists of a photo-diode, pin or avalanche which converts the incident light into photo-current and a low-noise amplifier which amplifies the photo-current. The performance, i.e. bandwidth, dynamic range and noise figure of the receiver is mainly determined by the low-noise amplifier. The amplifier may employ silicon bipolar or field-effect transistors. A number of optical receiver packages are produced by various manufacturers, one such is the National Semiconductors LH0082.

Fig 1



Optocouplers

The optocoupler also called an optoisolator, is a completely sealed IRED exciter and a photodetector. The exciter and detector are two completely isolated circuits; yet signals can be readily transferred between them. A low-voltage source can be made to control a high-voltage output circuit with complete isolation and without the high potential danger often encountered.

The optocoupler may contain an IRED emitter with a photodiode, phototransistor, Darlington or laser sensor. To use these devices effectively, their characteristics must be known. Although many of their characteristics are similar to those for circuits using discrete components, there is a difference in the degree of isolation between the input and output circuits. The isolation features can be divided into three types: isolation resistance, isolation capacitance and dielectric breakdown ability. The isolation resistance is in the order of $1 \times 10^{11}\Omega$. The circuit resistance, external to the coupler, may be much lower in value. The capacitive isolation ranges from less than 1 pF to less than 3 pF and is the capacitance of the dielectric materials. Again, the circuit board layout may have a higher capacity than the coupler. Both the resistance and capacitive values are affected by the distance and medium between the source and detector. A piece of glass which is often used, affects the isolation characteristics.

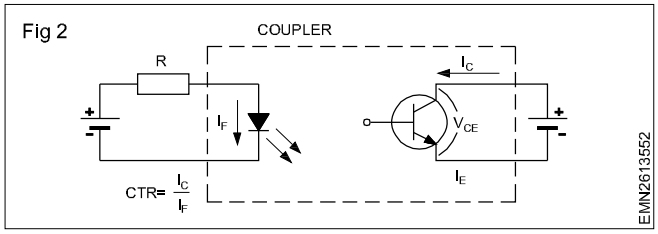
The dielectric resistance breakdown, rated in volts, defines the maximum voltage that can be applied. Other factors such as waveshape, temperature and altitude also affect the dielectric breakdown rating. Although a coupler may withstand 1000 V DC. It may only withstand 500 V AC. Couplers that have been previously subjected to high-surge voltages may exhibit a higher leakage resistance and/or short circuits between elements.

Input-output characteristics of an optocoupler, are similar to those for circuits that use discrete components. The input of the coupler is usually an IRED and the output is one of several type of sensors. In some couplers, additional reflective surfaces may be added, or components such as an R or C may be needed in order to meet specific applications. The choice of IRED emitter with a photodiode, phototransistor or Darlington will depend on the specific application.

An important consideration in the use of the optocoupler or optoisolator is the current-transfer ratio. This parameter measures how much current is transferred from the IRED to the sensor in the presence of complete electrical isolation. The CTR used with any LED-sensor combination, describes the current gain (or loss) from input to output. Essentially, the CTR is similar to comparing the I_C to I_B in a transistor circuit. Fig 2 shows the emitter-sensor circuits of a coupler.

The CTR in a coupler is defined as the ratio of I_C to I_F and from the practical point of view, the combined circuit acts as a CE amplifier except for the fact that there is no common tie between the input-output circuits. Depending on the type of sensor, the CTR can range from a loss to a gain of more than 1000.

Fig 2



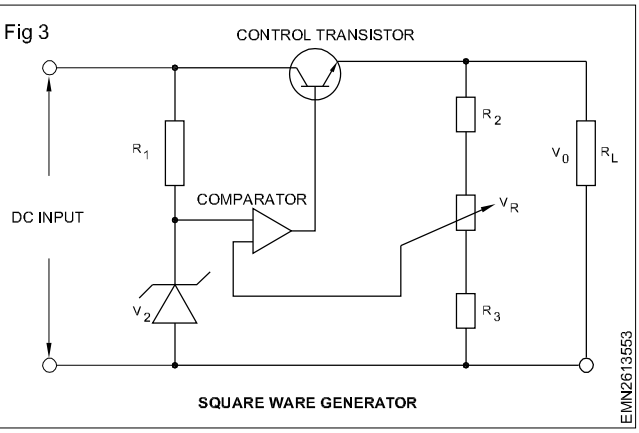
LASCR Sensors and Triac couplers

The LASCR (Light Activated SCR) uses radiant light to

activate its gate. The assembly consists of two transistos- a high voltage PNP and a gate-controlled NPN transistor. Fig 3 shows how the circuit is arranged.

When the PN junction (diode) is light-activated, a current I_P flows into the NPN transistor and biases it on; this, in turn, activates the base of the PNP transistor, turning it on. The NPN transistor is required to be a high-gain amplifier circuit, since the light-sensitive photodiode produces a very small amount of current. Because of this high sensitivity, the LASCR is also sensitive to temperature and the applied line voltage. Most LASCR circuits are low-current-rated and so are used as controllers for higher-power SCR equipment.

Fig 3



The triac like the SCR, is a power controller. The triac, however is controllable from almost zero to full power. It is ideally suited to variable-power drives, such as electric drills, heaters, light dimmers and numerous appliances.

The high-power triac, in discrete-component form, requires a smaller-powered triac to control it. This low-power two-terminal unit is referred to as a diac. In the optical coupler field, this device is called a triac driver or bilateral switch. One such triac drivers, commercially available is the motorola MOC3010.

Optical fibres

Principle

The suggestion that information could be carried on light and sent over long distances in thin fibres of very pure (optical) glass was first made in 1966. Eleven years later, the world's first fibre optic telephone link was made to work in Britain. It is expected that eventually all cables at homes and offices will change over from copper to glass cables.

Light, like radio waves is electromagnetic radiation but because of its much higher frequency (typically 10^{14} Hz = 10^5 GHz), it has a considerably greater information-carrying capacity because of its wide bandwidth. When light is modulated and guided by glass fibre cables installed in cable ducts, it escapes the severe attenuation it would suffer from rain and fog if sent through the air. It is also free from 'noise' due to electrical interference and hence distances of atleast 30 km can be used without regenerators/repeaters.

Compared with copper cables, optical fibre cables are lighter, smaller and easier to handle.

Lasers

The 'light' used in optical fibres is infrared radiation in the region just beyond the red end of the visible spectrum. Optical fibres employ 1300 or 1500 nm waves since, the longer the wavelength, the less is the atenuation of the radiation by the glass. This is why infrared is preferred to 'visible' light in optical fibres.

The infrared is generated by a tiny semiconductor laser made from gallium, aluminium and arsenic. A laser (standing for light amplification by the stimulated emission of radiation) produces a very narrow coherent beam of electromagnetic radiation of one particular frequency. Coherent light, in contrast to light from other sources (e.g a lamp) consists of waves vibrating in phase with each other, rather like the radiation, at much lower frequencies, from a radio transmitter. The detector at the receiving end is a photodiode which converts the optical signal into an electrical one.

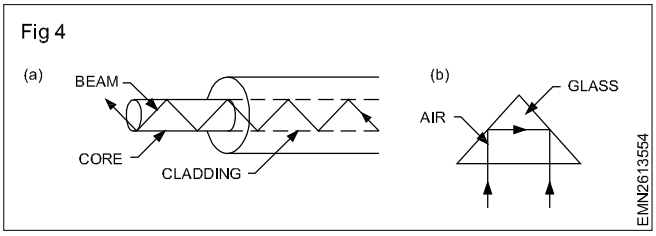
Modulation

The infrared is pulse code modulated by the speech or other data to be transmitted. Digital signals are sent in the form of pulses of radiation, being on for a '1' and off for a '0'.

Optics

The optical fibres, which are about 0.1mm in diameter have a glass core of higher refractive index than the glass cladding around it. As a result, the infrared beam is trapped in the core by total internal reflection at the core-cladding boundary as shown in Fig 4a. This is just as light is in the prisms as shown in Fig 4b of binoculars when it strikes the back surface of the prism where the refractive index is high in the glass but low in the air. The glass in optical fibres is so pure that a 2 km length absorbs less 'light' than a sheet of window glass.

Fig 4



Capacity

The information carrying capacity of an optical fibre system is about the same as the best coaxial cables. It is typically around 140M bit/sec. A 140M bit/s system can carry about 2000 telephone channels or 250 music channels or 2 colour TV channels or a mixture of these. 140 M bit/s is a very high rate of information transfer being equivalent to delivering 8 average length books every second!

Optoisolator (optical coupler or optocoupler)

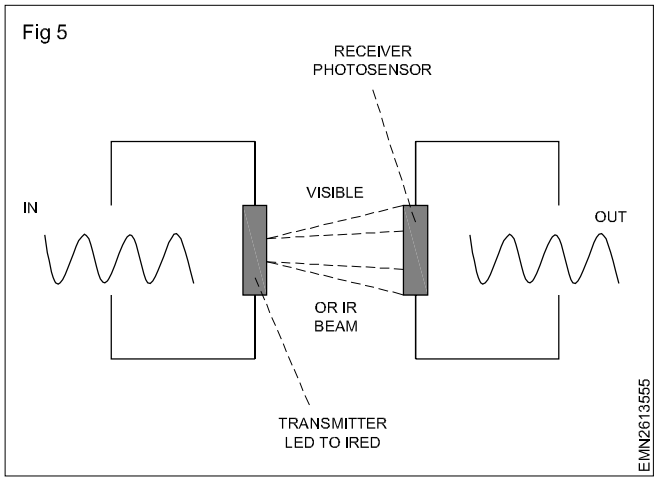
An optoisolator (also known as optical coupler, optocoupler and opto-isolator) is a semiconductor device that uses a

short optical transmission path to transfer an electrical signal between circuits or elements of a circuit, while keeping them electrically isolated from each other. These components are used in a wide variety of communications, control and monitoring systems that use light to prevent electrical high voltage from affecting a lower power system receiving a signal.

In its simplest form, an optoisolator consists of a light-emitting diode (LED), IRED (infrared-emitting diode) or laser diode for signal transmission and a photosensor (or phototransistor) for signal reception. Using an optocoupler, when an electrical current is applied to the LED, infrared light is produced and passes through the material inside the optoisolator. The beam travels across a transparent gap and is picked up by the receiver, which converts the modulated light or IR back into an electrical signal. In the absence of light, the input and output circuits are electrically isolated from each other.

Electronic equipment, as well as signal and power transmission lines, are subject to voltage surges from radio frequency transmissions, lightning strikes and spikes in the power supply. To avoid disruptions, optoisolators offer a safe interface between high-voltage components and low-voltage devices.

Fig 5



The optoisolator is enclosed in a single device, and has the appearance of an integrated circuit (IC) or a transistor with extra leads. Optocouplers can be used to isolate low-power circuits from higher power circuits and to remove electrical noise from signals.

Optoisolators are most suited to digital signals but can also be used to transfer analog signals. The isolation of any data rate of more than 1 Mb/sec is considered high speed. The most common speed available for digital and analogoptoisolators is 1 Mb/sec, although 10 Mb/sec and 15 Mb/sec digital speeds are also available.

Optoisolators are considered too slow for many modern digital uses, but researchers have created alternatives since the 1990s.In communications, high-speed optoisolators are used in power supplies for servers and telecom applications -- Power over Ethernet (PoE) technology for wired Ethernet LANs, for example.

Optoisolator components can also protect Ethernet and fiber optic cables from electrical surges. In VoIP phones, electrical signals can be isolated using a transistor output optocoupler.Although no longer common, where modems are used to connect to telephone lines, the use of optoisolators allow a computer to be connected to a telephone line without risk of damage from electrical surges or spikes. In this case, two optoisolators are employed in the analog section of the device: one for upstream signals and the other for downstream signals. If a surge occurs on the telephone line, the computer will be unaffected because the optical gap does not conduct electric current.

Digital IC families and their operational characteristics

Objectives : At the end of this lesson you shalll be able to
- **define the basic terms related to digital IC gates**
- **recognize the different types of packages of ICs used in the digital IC**
- **list different levels of integration used in fabrication of digital IC**
- **differentiate logic families and their characteristics**
- **explain safety precaution to be adopted while handling CMOS ICs**
- **compare the TTL and CMOS families**
- **explain digital IC numbering system.**

Introduction

A digital system is a combination of devices designed to Process information that are represented in digital form. Example of a few most popular digital systems are,

– Digital computers

– Calculators,

– Digital audio and video equipments

– Telephone system ..... etc.,

Digital Telephony is probably the world's largest digital system.

In electronic circuits, signals are represented in voltage or current. In these circuits, the signal representation will have a number of voltage or current levels.

In such analog signals, the transition from one level to another is usually smooth rather than sudden diffence between and the transition between them is also smooth rather than sudden.

Digital signals on the other hand can have only two discrete states. These states can be called as,

– **ON state**: A state at which a predefined voltage is present. For example, the level could be, +5 Volts, +10Volts and it is also represented as high, one, etc.

– **OFF state**: A state at which a predefined voltage is other than the ON state voltage is present. For example, the level could be, 0 Volts, -5 Volts and it is also represented as low, zero etc.,

The discrete levels in digital signals are technically referred to as logic levels. Generally, the ON state described above is referred as the LOGIC 1 state and the OFF state as the LOGIC 0 state. It is very essential to note that, in digital signal representation, no state exists in between the logic-0 and logic-1 state.

For example,if we say Logic-0 corresponds to 0 volts and Logic-1 corresponds to 1 volt. In such a digital system, voltage levels of 2V,3V,4V etc., have no meaning (further details are discussed in lessons that follows).

Because the transition time between ON to OFF state or vice versa is abrupt in digital signals, analysis of digital systems varies from that of pure analog systems such as amplifiers etc.,

Compared to analog circuits, digital circuits contains less number of discrete components such as resistors, capacitors atc., This is mainly for the reason that the Integrated circuit(IC) technology has advanced so much, millions of components can be prefabricated in a single IC. Most digital circuits are made of such VLSI (very large scale Integration) IC as its main circuit component with a few decoupling capacitor for suppling clean DC voltage.

It is important to note that any analog signal can be converted to a digital signal (in the form 1s or 0s). Example given below gives a clue about how analog signals can be represented as digital signals,

ANALOG VOLTAGE	DIGITAL VALUE
0 volt	0 0 0 0
1 volt	0 0 0 1
2 volt	0 0 1 0
3 volt	0 0 1 1
4 volt	0 1 0 0
5 volt	0 1 0 1
6 volt	0 1 1 0
7 volt	0 1 1 1
8 volt	1 0 0 0
9 volt	1 0 0 1
10 volt	1 0 1 0

Details of how this conversion is done is discussed in further lessons.

Digital systems offer the following advantages over analog systems

– Easier to design

– Information storage is easy

– Accuracy and precision are greater

– Programmable

– Circuitry can be fabricated on IC chips more easily

– High speed functions

The operations carried out using digital signals are called Logic operations. Example of Logic operation are given below;

Assuming there are two inputs and if the Inputs are,

– the circuit output should be Logic-1 if atleast any one of the two inputs is Logic-1.

  A circuit that performs such a logical operation is called as a **OR** gate.

– the circuit output should be Logic-1 only when both the inputs are Logic 1's.

  A circuit that performs such a logical operation is called as a **AND** gate.

– the circuit output should be inverse of the input. If the input is Logic-1, then the output should be Logic-0 and vice-versa.

A circuit that performs such a logical operation is called as a **NOT** gate.

Every logic operation, even the most extensive and the most complicated - can be reduced to combinations of the above said three basic logic functions. By combining these three operations, several other functions such NAND, NOR and so on (discussed in further paragraphs).

These basic functional circuits are called Gates, such as OR gate, AND gate and NOT gate. The practical implemantation of logic operations is effected by logic circuits. In the meantime, a large number of circuit families have been produced in integrated circuit technology. The starting point of standard development was the TTL (Transistor-Transistor-Logic) family(earlier to it was the RTL and DTL families), from which several other families with improved properties have been derived. The TTL family of gates have defined voltage levels and permissable tolerences. Some of the important terminologies associated with digital ICs are given below;

Terminology of digital ICs

Saturated logic gate

A form of logic gate in which one output state is the saturation voltage of a transistor.

Example

Resistor Transistor Logic (RTL), Diode Transistor Logic (DTL) and Transistor Transistor Logic (TTL).

Unsaturated logic or current mode logic gate

A form of logic with transistors outside the saturated region.

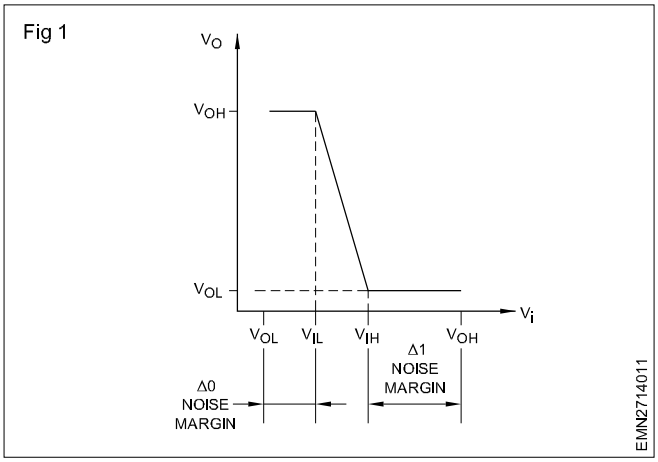
Example

Current Mode Logic (CML) and Emitter Coupled Logic. This has ultra-fast switching speed and low logic swing.

Operating voltages

The various operating voltages of a logic gate can be understood with the help of the transfer characteristic of the gate as shown in Fig 1.

Fig 1



V_{OH} - The minimum voltage which will be available at a gate output when the output is supposed to be at logic '1'.

V_{IL} - The minimum gate input voltage which will unambiguously be accepted by the gate as logic '1'.

V_{OL} - The maximum voltage which will appear at a gate output when the output is supposed to be at logic '0'.

V_{IL} - The maximum gate input voltage which will unambiguously be accepted by the gate as logic '0'.

Logic swing: The difference between the two output voltages (V_{OH} - V_{OL}) is known as the logic swing of the circuit. That is,

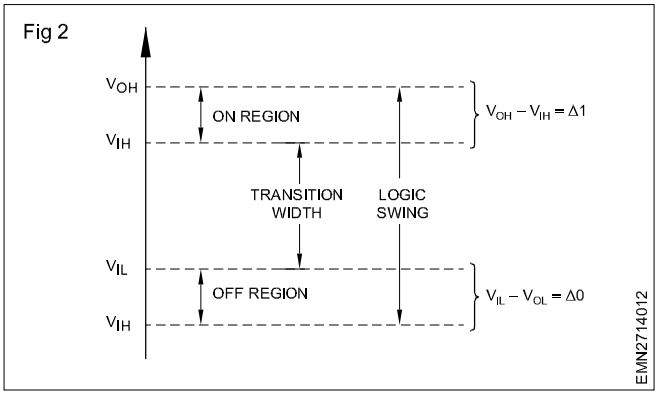
logic swing = V_{OH} - V_{OL}

Noise margin

The amount of voltage of extraneous signal which can be tolerated before an output voltage of gate deviates from the allowable logic voltage levels.

The different noise margins of a logic gate can be understood with the help of logic level diagram at Fig 2.

Fig 2



Low-level noise margin

The difference (V_{IL} - V_{OL}) is low level noise margin (D_o)
$D_o = V_{IL} - V_{OL}$

High level noise margin

The difference (VOH - VIH) is high level noise margin (D_1)
$D_1 = V_{OH} - V_{IL}$

Transistion width:

From Fig 2, transistion width = $V_{IH} - V_{IL}$

It can be seen that an increased noise margin capability is obtained as either VOH and VOL move away from each other or as VIH and VIL move toward each other. With a larger logic swing or a narrower transistion width, the noise margins will improve.

Noise immunity

Stray electric and magnetic fields can induce voltages on the connecting wires between logic circuits. These unwanted signals are known as noise and they may cause the voltage at the input to a logic circuit to drop below VIH (min) or rise above VIL (max), which may lead to unpredictable operation. The noise immunity of a logic circuit refers to the ciruit's ability to tolerate noise without causing unwanted changes in the output voltage.

Fan-out

The number of loads connected to a gate is known as fan-out of the gate. The number of load gates need not be a limiting number of load gates need not be a limiting number. It is also known as loading factor. For example, a logic gate that is specified to have a fan-out of 10 can drive 10 standard logic inputs. If this number is exceeded, the output logic-level voltages cannot be guaranteed.

Types of IC package

The ICs come in a wide variety of package types. The factors which determine the type of package are

– amount of circuitry contained in the IC

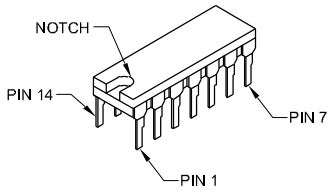
– number of external connections that need to be made to it.

– humidity of the environment, ambient temperature at which the IC is to operate

– method of mounting on the PCB.

DIP [Dual in line package]

Fig 3

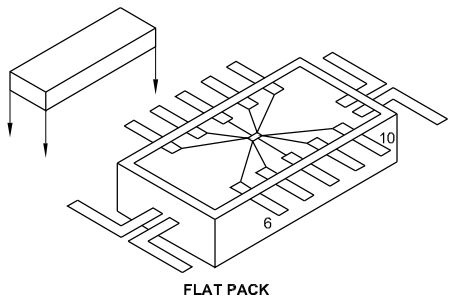


The external connecting pins are in parallel rows along the two long edges of the package as shown in Fig 3. In DIP ICs, number of pins varies from 4 to 64 depending on the internal circuitry. For low temperature and low humidity, epoxy plastic packages are used. For high temperature or for devices that dissipate large amount of power, ceramic packages are used.

Ceramic flat package

This type of IC packages are hermetically sealed as shown in Fig 4, which means that they are totally immune to the effects of humidity. These packages are often used in military equipments that they must be able to withstand harsh environments. Pins are counted around the package from notch or dot. These packages are usually mounted in high quality sockets on the circuit board.

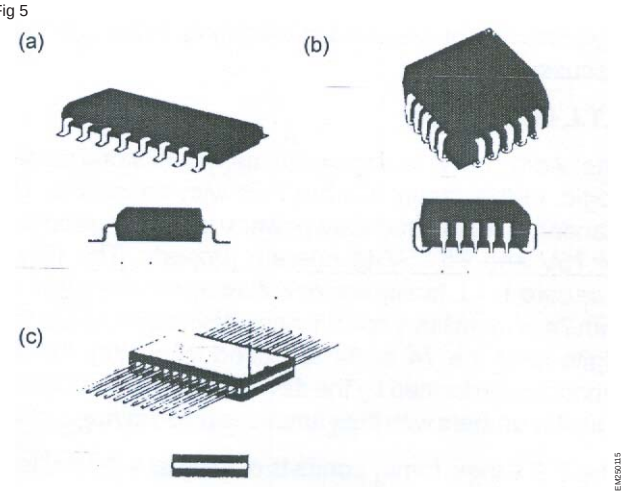
Fig 4



Surface mount package

This popular package is similar to the standard DIP except that it is smaller and, as the name implies, its pins are constructed so that it can be soldered directly to metal pads on the PCB. One type of SMT package called small out line IC is shown in Fig 5a. Since surface mount packages are soldered on one surface of the circuit board, holes don't have to be drilled on the PCB. Surface mount devices have further advantages, that they are more easily handled by equipment, which automatically mounts components in the correct position on circuit boards during manufacturing. The PLCC (Plastic Leaded chip carrier) type package is shown in Fig 5b. Another variety of SMT package is known as Flat pack is shown in Fig 5c.

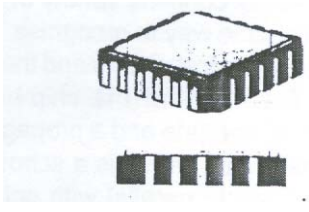
Fig 5



Ceramic chip carrier package

These chips are intended to be clamped into a socket as shown in Fig 6 so that the pads press against contacts which are connected to P.C.B signal lines pin 100 this package is to the right of the notched corner.

Fig 6



Pin grid array package

These ICs are used for VLSI digital circuits such microprocessor. The number of pins in the array depends on the complexity of the internal circuit. The four corner pin positions are usually left without pins. Common array sizes are 10 x 10, 13 x 13 and 14 x 14, large ICs such as these are put in sockets so they can easily be replaced if the device fails.

Fig 7

S.No.	Complexity	Number of Gates	Application
1	Small-Scale Integration (SSI)	Fewer than 12	Basic gates
2	Medium-Scale Integration (MSI)	12 to 99	Flip-flops, regiater etc.
3	Large-Scale Integration (LSI)	100 to 9999	Memories, microprocessor
4	Very large-Scale Integration (VLSI)	10,000 to 99,999	-do-
5	Ultra large-Scale Integration (ULSI)	100,000 or more	-do-

Logic family

Digital ICs are classified not only by their complexity, logical operation, speed of operation but also by the specific circuit technology to which they belong. The circuit technology is referred to as a digital logic family. Each logic family has its own basic electronic circuit upon which more complex digital circuit and components are developed. The basic circuit in each technology is NAND, NOR or an inverter gate. The electronic components, and material used in the construction of the basic circuit are usually used as the name of the technology. The various logic families of ICs used in electronic circuit are briefly discussed below.

TTL Logic family

The word TTL is expanded as Transistor-Transistor Logic. In this family ICs are built with transistors. Most standard TTL ICs require a power supply voltage between +4.75V and +5.25V to operate properly. The ICs of standard TTL family are identified by numbers that start with 74 or for military specification devices 54, two or three digits after the 74 or 54 are used to identify the logic functions performed by the device. Some of the 74 series TTL IC numbers with their functions given at Appendix 'D'.

The TTL logic family consists of several sub families as shown in logic family tree. The difference between the various TTL series are in their electrical characteristics, such as power dissipation, propagation delay and switching speed. They do not differ in the pin assignment or logic operation performed by the internal circuits.

The most popular 7400 series is a line of standard TTL chips. This bipolar family contains variety of compatible SSI and MSI devices. One way to recognise TTL design is the multiple emitter input transistors and the totem pole output transistors. The standard TTL chip has a power dissipation of about 10mw/gate and a propagation delay of around 10ns. The series 74S00 is a schottky version having a schottky diode in parallel with collector-base terminals. In this, transistors are prevented from saturating thereby propagation delay is reduced typically to 3ns. By increasing internal resistances and including schottky diodes, low power schottky diodes numbered from 74LS00 are manufactured limiting the power dissipation to 2mw per gate low power schottky TTL is the most widely used of the TTL types. In this family of devices, a floating input is equivalent to a high input. In electrically noise environment, floating inputs may pick up enough noise voltage to produce unwanted changes in the output stages and hence inputs should not kept be floating in TTL family. A modified TTL design namely three state TTL allows us to connect outputs directly. Earlier computers used open-collector devices with their bases but the passive pull-up limited the operating speed. These newer devices are much faster and have a control input that can turn off the devices. When this happens the output floats and presents a high impedance to whether it is connected to and hence are widely used for connecting to bases.

E.C.L

Emitter-coupled logic circuits provide the highest speed with propagation delay typically of 5ns. The most common ECL ICs are designated as the 10000 series. E.C.L is used in systems such as super computers and signal processors where high speed is essential. The ECL family IC use is restricted to few applications because of the following reasons.

– The gates in ICs dissipate relatively large amounts of power.

– Needs extra circuitry for gates to operate.

– The -ve power supply voltage and logic levels make ECL gates difficult to interface with other logic family members.

MOS

The Metal Oxide Semiconductor is a unipolar transistor that depends upon the flow of only one type of carrier, which may be either electrons or holes. A p-channel MOS is referred to as PMOS and an N-channel as NMOS. NMOS is the one that is commonly used in circuits with only one type of MOS transistor. MOS technology allows a very large number of circuits to be built in a single IC. It is this

technology which has made possible the microprocessors, memories and other LSI devices which are used to build microcomputers.

CMOS

PMOS circuitry or NMOS circuitry can't be used alone for making simple logic gate devices such as done in T.T.L devices, for various reasons. However by building the circuits on the IC by using one PMOS and NMOS transistors connected in complementary fashion, it is possible to produce logic gate devices which have the desired characteristics. That is why these ICs are called complementary metal oxide semiconductors or just CMOS.

CMOS ICs are designated in 4000 series. The family includes logic functions such as those available in T.T.L family. CMOS sub families operate properly with a power supply voltage of +3V to +15V.

By the time the 4000 series of CMOS was developed, most logic designers has become very familiar with the logic functions, part numbers and pin connections of the devices in the standard T.T.L sub family. So as to make CMOS ICs more compatible with T.T.L standards, the CMOS, TTL compatible ICs are made available in 74C00 series. 74HC00 series (high speed) 74HCT00 series, refer Table Performance comparison of CMOS and TTL logic families is given in the Table below:

Technology	CMOS		TTL				
	Silicon Gate	Metal-Gate	Std.	Low-Power Schottky	Schottky	Advanced Low-Power Schottky	Advanced Schottky
Device series	74HC	4000	74	74LS	74S	74ALS	74AS
Power dissipation (mW/gate)							
Static	0.0000025	0.001	10	2	19	1	8.5
AT 100 kH_z	0.17	0.1	10	2	19	1	8.5
Propagation delay time (ns)							
(CL = 15 pF)	8	50	10	10	3	4	1.5
Maximum clock frequency (MHz)							
(CL = 15 pF)	40	12	35	40	125	70	200
Speed/Power product (pJ)							
(at 100 kHz)	1.4	11	100	20	57	4	13
Minimum output drive IOL (mA)							
(VO = 0,.4V)	4	1.6	16	8	20	8	20
Fan-out;							
LS loads	10	4	40	20	50	20	50
Same-series	*	*	10	20	20	20	40
Maximum input current, IIL (mA)							
(VI = 0.4V)	±0.001	-0.001	-1.6	-0.4	-2.0	-0.1	-0.5

*Fan-out is frequency dependent

COMPARISON OF TYPICAL NOISE MARGINS:

Noise Margin	HCMOS (V)	Std TTL (V)	LS TTL (V)	S TTL (V)	AS TTL (V)
V_{NH}	1.4	0.4	0.7	0.7	0.7
V_{NL}	0.9	0.4	0.4	0.4	0.4

Digital I.C numbering system

Number and letters on IC packages identify the logic family and the logic function of a device. In addition to these numbers and letters, an IC may have numbers and letter which indicate manufacturers name, the factory where the device was manufactured, the year and month the device manufactured, the package type and a code which indicates how thoroughly the device was tested.

Ex: 74HCTOON

74 HCT OO N

XXX XXX X

Letter codes for common package type

N = Plastic dip

J = Ceramic dip

D = Glass/metal dip

W = Flat pack

Manufacturer code

Code	Manufacturer
AM	Advanced microdevice
CD	GE/RCA
DM	National semiconductor
F	Fair child
GD	Gold star
H	Harris
HD	Hitachi
IM	Intersil
KS	Samsung
LR	Sharp
M	SGS
MC	Motorola
MM	Monolithic memories
MN	Panasonic
N	Signetics
P	Intel
SN	Texas instruments
SP	SPI
US	Sprague
TC	Toshiba

Number systems

Objectives : At the end of this lesson you shalll be able to

- **differentiate between different number systems like decimal, octal, binary and hexadecimal and conversion between them and different types of codes**
- **explain NOT gate using transistor**
- **explain the characteristics of TTL NOT gate IC 7404, list commercially available NOT gate IC**
- **explain logic probe based on CMOS NOT gate IC.**

Introduction

When we hear the word 'number' immediately we recall the decimal digits 0,1,2....9 and their combinations. Modern computers do not process decimal numbers. Instead, they work with binary numbers which use the digits '0' and '1' only. The binary number system and digital codes are fundamental to digital electronics. But people do not like working with binary numbers because they are very long when representing larger decimal quantities. Therefore digital codes like octal, hexadecimal and binary coded decimal are widely used to compress long strings of binary numbers.

Binary number systems consists of 1s and 0s. Hence this number system is well suited for adopting it to the digital electronics.

The decimal number system is the most commonly used number system in the world. It uses 10 different characters to show the values of numbers. Because this number system uses 10 different characters it is called base-10 system. The base of a number system tells you how many different characters are used. The mathematical term for the base of a number system is radix.

The 10 characters used in the decimal number systems are 0,1,2,3,4,5,6,7,8,9.

Positional notation and weightage

A decimal integer value can be expressed in units, tens, hundreds, thousands and so on. For example decimal number 1967 can be written as 1967 = 1000 + 900 + 60 + 7. In powers of 10, this becomes

10^3	10^2	10^1	10^0	
				$1 \times 10^3 = 1000$
				$9 \times 10^2 = 900$
				$6 \times 10^1 = 60$
1	9	6	7	$7 \times 10^0 = 7$
				1967

i.e. $[1967]_{10} = 1(10^3) + 9(10^2) + 6(10^1) + 7(10^0)$

This decimal number system is an example of positional notation. Each digit position has a weightage. The positional weightage for each digit varies in the sequence 10^0, 10^1, 10^2, 10^3 etc starting from the least significant digit.

The sum of the digits multiplied by their weightage gives the total amount being represented as shown above.

In a similar way, binary number can be written in terms of weightage.

To get the decimal equivalent, then the positional weightage should be written as follows.

$$[1010]_2 = 1(2^3) + 0(2^2) + 1(2^1) + 0(2^0)$$
$$= 8 + 0 + 2 + 0$$
$$[1010]_2 = [10]_{10}$$

Any binary number can be converted into decimal number by the above said positional weightage method.

Decimal to Binary conversion

Divide the given decimal number by 2 as shown below and note down the remainder till you get the quotient - zero.

Example

	0		
2	1	1	$\rightarrow$ MSB
2	2	0	
2	4	0	
2	8	0	
2	17	1	
2	34	0	LSB

The remainder generated by each division form the binary number. The first remainder becomes the LSB and the last remainder becomes the MSB of binary number.

Therefore, $[34]_{10} = [100010]_2$

Counting binary number

To understand how to count with binary numbers, let us see how an odometer (Km indicator of a car) counts with decimal numbers,

The odometer of a new car starts with the reading 0000.

After traveling 1km, reading becomes 0001.

Successive km produces 0002, 0003 and so on upto 0009

At the end of 10th km, the units wheel turns back from 9

to 0, a tab on this wheel forces the tens wheel to advance by 1. That is why the number changed from 0009 to 0010. That is, the units wheel is reset to 0 and sent a carry to the tens wheel. Let us call this familiar action as reset and carry. The other wheels of odometer also reset and carry. For instance, after covering 999km, the odometer shows 0999.

After the next km, the unit wheel resets and carries, the tens wheel resets and carries, the hundreds wheel resets and carries and the thousands wheel advances by 1 to get the reading 01000.

Binary odometer

Visualize a binary odometer, a device whose wheels have only two digits 0 and 1. When each wheel turns, it displays 0 then 1 and then back to 0 and the cycle repeats. A four digit binary odometer starts with 0000.

After 1km, it indicates - 0001.

The next km forces the units wheel to reset and sends carry. So the number changes to 0010.

The third km results in 0011.

After 4km, the units wheel resets and sends carry, the second wheel resets and sends carry and the third wheel advances by 1. Hence it indicates 0100.

Table below shows all the binary numbers from 0000 to 1111 equivalent to decimal 0 to 15.

Decimal	Binary
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

Hexadecimal number system: In hexadecimal system there are 16 characters. They are 0,1,2,3,4,5,6,7,8,9, A,B,C,D,E,F where A=10, B=11, C=12, D=13, E=14,

F=15 in decimal. In this system, the base is 16. This system is mainly used to develop programmes for computers.

For Example

$[23]_{16} = [35]_{10}$; $16^1 \times 2 + 16^0 \times 3 = 32 + 3 = 35$;

$[2C]_{16} = [44]_{10}$; $16^1 \times 2 + 16^0 \times 12 = 32 + 12 = 44$;

Decimal to hexadecimal conversions

The conversion of decimal to hexadecimal is similar to binary conversion. Only difference is that divide the decimal number successively by 16, and note down the remainder.

	0		
16	1	1	MSB
16	27	11 or B	
16	432	0	LSB

$[432]_{10} = [1B0]_{16}$

Hexadecimal to Decimal

This conversion can be done by putting it into the positional notation.

Ex: $223A_{16} = 2 \times 16^3 + 2 \times 16^2 + 3 \times 16^1 + A \times 16^0$

$= 2 \times 4096 + 2 \times 256 + 3 \times 16 + 10 \times 1$

$= 8192 + 512 + 48 + 10$

$= 8762_{10}$

Octal number

The octal number system provides a convenient way to express binary numbers. It is used less frequently compared to hexadecimal in conjunction with computers and microprocessors to express binary quantities for input and output purposes.

The octal number system is compared of digit symbols such as right symbols such as 0,1,2,3,4,5,6,7.

Since there are 8-symbols, radix or base is 8. Positional weightage is .....8^3, 8^2, 8^1, 8^0.

To distinguish octal numbers from other number systems subscript 8 is used as follows:

Ex: $(15)_8 \tilde{} (13)_{10}$

Octal Decimal

Octal to Decimal conversion

	0		
8	1	1	MSB
8	13	5	LSB

As in other number systems, each digit should be multiplied by its positional weightage and added to get decimal equivalent.

Convert $(2374)_8$ into decimal number

Positional weightage : 8^3, 8^2, 8^1, 8^0

Octal number 2 3 7 4

$(2374)_8 = (2 \times 8^3)+(3 \times 8^2)+(7 \times 8^1)+(4 \times 8^0)$

$= (2 \times 512)+(3 \times 64)+(7 \times 8)+(4 \times 1)$

$= 1024 + 192 + 56 + 4$

$(2374)_8 = (1276)_{10}$

Decimal to octal conversion

A method of converting a decimal number to an octal number is the repeated division by 8, each successive division by 8 yields a remainder that becomes a digit in the equivalent octal number. The first remainder generated is the least significant digit (LSD).

$(359)_{10} = (547)_8$

	0		
8	5	5	MSB
8	44	4 or B	
8	359	7	LSB

Octal to binary

Each octal digit can be represented by a 3-bit binary number, because of this it is very easy to convert from octal to binary. Each octal digit is represented by three bits as shown in the table.

Octal digit	0	1	2	3	4	5	6	7
Binary	000	001	010	011	100	101	110	111

To convert each octal number to a binary, simply replace each octal digits with the corresponding binary bits.

Example

1 $(25)_8 = (\ )_2$

2 5

010 101

$(25)_8 = (010101)_2$

2 $(7526)_8 = (\ )_2$

7 5 2 6

111 101 010 110

$(7526)_8 = (111101010110)_2$

Binary to octal

Conversion of a binary number to an octal number is the reverse of the octal-to-binary conversion. The procedure is as follows.

1 Start with the right most group of three bits and moving from right to left, convert each 3-bit group to the equivalent octal digit.

2 If there are not three bits available for the left most group, add either one or two zero's to make complete group. These leading zero's will not affect the value of the binary number.

Example

$(110101)_2$ = ( )$_8$

110 101

6 5 = $(65)_8$

$(11010000100)_2$ = ( )

011 010 000 100 = $(3204)_8$

3 2 0 4

BCD (Binary Coded Decimal)

Binary Coded Decimal (BCD) is a way to express each of the decimal digits with a binary code, since there are only ten code groups in the BCD system, it is very easy to convert between decimal and BCD. Because decimal system is used for read and write, BCD code provides an excellent interface to binary systems. Examples of such interfaces are keypad inputs and digital readouts.

8421 code

The 8421 code is a type of binary coded decimal (BCD), binary coded decimal means that each decimal digit, 0 through 9 is represented by a binary code of four bits. The designation 8421 indicates the binary weights of the four bits (2^3, 2^2, 2^1, 2^0). The ease of conversion between 8421 code numbers and the familiar decimal numbers in the main advantage of this code. All you have to remember are the ten binary combinations that represents the ten decimal digits as shown in Table.

Decimal digit	0	1	2	3	4	5	6	7	8	9
BCD	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001

The 8421 code is the pre-dominant BCD code, and when we refer to BCD, we always mean the 8421 code unless otherwise stated.

Invalid code

You should realize that with four bits, sixteen numbers (0000 through 1111) can be represented, but in the 8421 code only ten of these are used. The six code combinations that are not used 1010, 1011, 1100, 1101, 1110 and 1111 are invalid in the 8421 BCD code.

To express any decimal number in BCD, simply replace each decimal digit with the approximate 4-bit binary code.

Example

1 $(35)_{10}$ = (?) 8421 code

3 5

0011 0101 = 00110101

2 $(2458)_{10}$ = (?) 8421 code

2 4 5 8

0010 0100 0101 1000 = 0010010001011000

There are many specialized codes used in digital system other than BCD code. Some codes are strictly numeric, like BCD and others are alphanumeric which are used to represent numbers, letters, symbols and instructions.

The commonly used codes other than BCD codes are

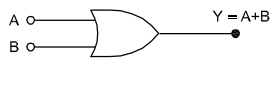
1 Gray code

2 Excess 3 code

3 ASCII code - American, Standard code for Information interchange

4 Alphanumeric code

Fig 1



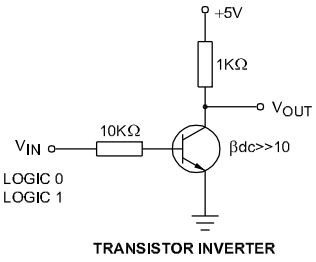
EMN2714021

Inverters (NOT Gate)

An inverter is a gate with only one input signal and one output signal. The output state is always the opposite of the input state. Logic symbol is shown in Fig 1.

Transistor inverter

Fig 2



TRANSISTOR INVERTER

EMN2714022

The above circuit shows the transistor inverter circuit. The circuit is a common emitter amplifier which works in saturation or in cut off region depending upon the input voltage. When V_{in} is in low level, say less than the transistor cut in voltage 0.6V in silicon type, the transistor goes to cut off condition and the collector current is zero. Therefore, V_{out} = +5V which is taken as high logic level. On the other hand, when V_{in} is in high level, the transistor saturates and V_{out} = V_{sat} = 0.3V i.e low level.

The table summarizes the operation

Vin	Vout
Low(0)	High(1)
High(1)	Low(0)

The logic expression for the inverter is as follows: If the input variable is 'A' and the output variable is called Y, then the output Y = A.

Logic gates and logic probes

Objectives : At the end of this lesson you shall be able to
- **explain the funtion of logie gates**
- **explain the AND gate using diode and its truth table**
- **explain the OR gate using diode and its truth table**
- **explain a NOT gate using transisteor and its truth table**
- **explain the NAND,NOR gate and their truth table**
- **explain the EX-OR and EX - NOR gates and their truth table.**

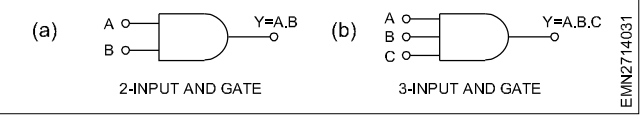
Introduction

Lagic gates are electcronic circuits used in digital circuits for the purpose of decisions. Logic circuits are basically of two types namely decision making circuits and memory circuits. Their functioning depends on the binary inputs they receive and produce binary output which are a function of the input as well as the characteristics of the logic circuit they implemented.All logic gates have a single output and they may have two or more inputs. For specific decision making function there are several types of logic gates are used. Basic Logic gates are a group of the logic gates spcifically called as AND,OR and NOT gates.All these gates have their own identical,logical function. By the combination of these gates we can obtain any Boolean or logical functions or any logical function.

AND gates

The AND gate has two or more inputs but only one output. All input signals must be held high to get a high output. Even if one of the inputs is low, the output becomes low.

Fig 1



The schematic symbols for 2 input and 3 input AND gates are shown in Fig 1a and 1b.

Truth table

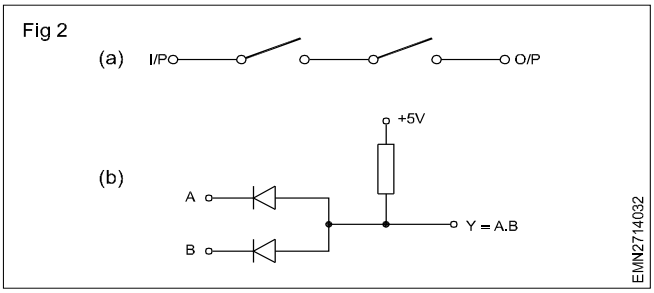
Two input AND gate

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Electrical equivalent circuit of an AND gate

The electrical equivalent of AND gate and AND gate using diodes are shown in Fig 2a and 2b.

Fig 2



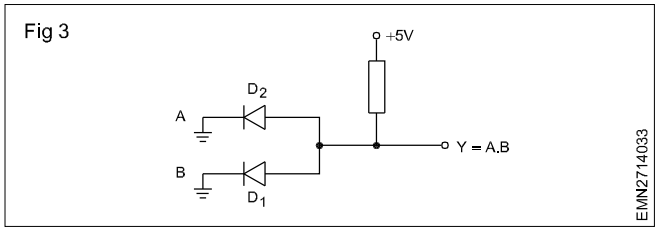
Two input AND gate using diode

Condition-1

A=0, B=0, Y=0 as shown in Fig 3.

During the above condition inputs A and B are connected to ground to make logic low inputs. During this condition, both the diodes conduct, and pulls the output Y to logic0.

Fig 3

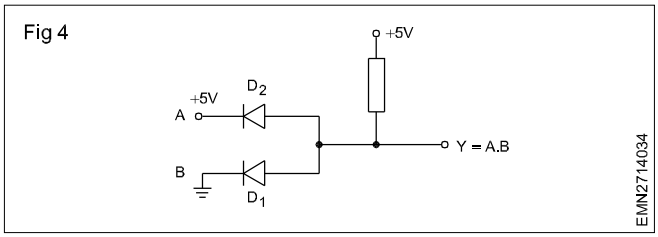


Condition-2

A=0, B=1, Y=0 as shown in Fig 4.

In the condition shown in Fig 4, diode D_1 is connected to logic-0 input and diode D_2 is connected to +5V [Logic high]. Diode D_1 is in forward bias and conducts. Diode D_2 is having equal potential (+5V) at anode and cathode. So potential difference between anode and cathode is 0. Hence diode D2 does not conduct. The output Y is pulled down to logic zero, since D_1 is conducting.

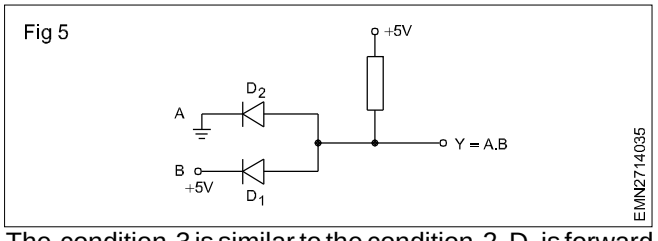
Fig 4



Condition- 3

A=1, B=0, Y=0 as shown in Fig 5.

Fig 5



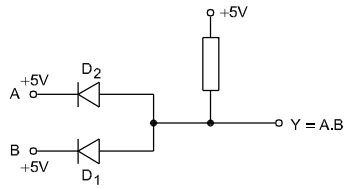
The condition-3 is similar to the condition-2. D_2 is forward biased. D_1 is reverse biased. Hence, output Y is pulled to logic-0.

Condition- 4

A=1, B=1, Y=1 as shown in Fig 6.

In this condition both the diodes are reverse biased. So both the diodes act as open circuit. Therefore, output Y is

Fig 6



+5V i.e y is in logic1 condition.

For pin diagram refer to the data sheet of the IC.

A. For example, if 1000 pulses pass through the gate in the 1 second interval of the enabled pulse, there are 1000 pulses/sec. That is, frequency is 1000Hz.

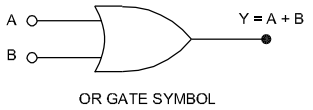
AND gates are available in the form of IC.IC7408 is a TTL type AND gate IC having 4 numbers of AND gates in side it.

OR gate

The OR gate has two or more inputs,but only one output.

The output of an OR gate will be in 1 state if one or more of the inputs is in 1 state. Only when all the inputs are in 0-state, the output will go to 0-state. Fig 7 shows the schematic Symbol of an OR Gate

Fig 7



The boolean expression for OR gate is Y=A+B.

The equation is to be read as Y equals A ORed B. Two-input truth table given below is equivalent to the definition of the OR operation.

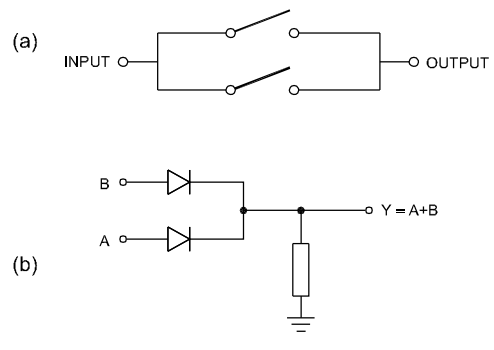
Truth table for OR gate

A	B	Y=A + B
0	0	0
0	1	1
1	0	1
1	1	1

Electrical equivalent circuit

The Fig 8a shows the electrical equivalent circuit of an OR gate. It is evident that if any one of the switch is closed, there will be output.

Fig 8



2 in-put OR gate using diode

The Fig 8b shows one way to build a 2-input OR gate, using diodes. The inputs are labeled as A and B, while the output is Y.

Assume logic 0 = 0V (low)

logic 1 = +5V (high)

Since this is a 2 input OR gate, there are only four possible cases,

Condition:1 A is low and B is low. With both the input voltage low, both the diodes are not conducting. Therefore the output Y is in low level.

Condition:2 A is low and B is high, The high B input voltage (+5V) forward biases the lower diode, producing an output voltage that is ideally +5V (actually +4.3V taking the diode voltage drop 0.7V into consideration). That is, the output is in high level. During this condition, the diode connected to input A is under reverse bias or OFF condition.

Condition:3 A is high and B is low, the condition is similar to case 2. Input A diode is ON and Input B diode is OFF and Y is in high level.

Condition:4 A is high, B is high. With both the inputs at +5V, both diodes are forward biased, since the input voltages are in parallel, the output voltage is +5V ideally [+4.3V to a second approximation]. That is, the output Y-is in high level.

OR gates are available in the IC form. IC7432 is a TTL OR gate IC having 4 OR gates inside it. For pin diagram refer to the data sheet of the IC.

Simple application of OR gate

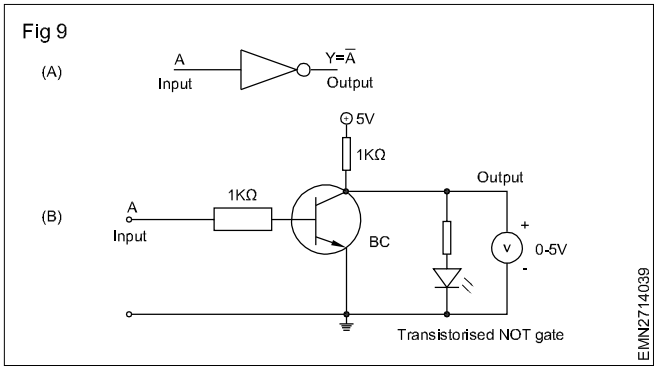
Intrusion detection

Simplified portion of an intrusion detection and alarm system is two windows and a door. The sensors are magnetic switches that produce a high(1) output when windows and doors are opened and a low(0) output when closed. As long as the windows and the door are secured, the switches are closed and all three of the OR gate inputs are in low(0). When one of the windows or the door is opened, a high(1) output is produced on that input of the OR gate and the gate output goes high. It then activities an alarm circuit to warn of the intrusion.

NOT gate

The NOT gate has only one input and one output as per the schematic symbol shown in Fig 9a and the circuit to construct the NOT gate using descrete comporents in Fig 9b.

Fig 9



The NOT gate inverts the logic stage of a binary signal input. The small circle (bubble) at the output of the symbol is formally called a negation indicator and designates the logical complement.

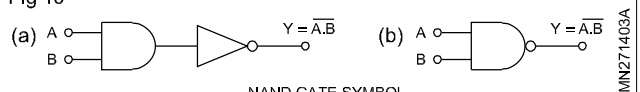
NAND gate

The **NAND** gate is the complement of the **AND** operation. Its name is an abbreviation of NOT **AND**.

The schematic symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that that a complement operation is performed on the output of the AND gate.

The schematic symbol and truth table of NAND gate is shown in Fig 10a &b.

Fig 10



Truth table

A	B	Y=$\overline{A.B}$
0	0	1
0	1	0
1	0	0
1	1	0

The truth table cleary shows that the NAND gate opertion is the complement of the AND gate.

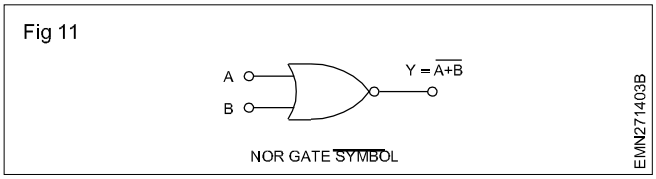
NOR gate:

The NOR gate is the complement of the OR operation. ITS name is an abbreviation of NOT OR.

The schematic symbol for the NOR gate consists of an OR symbol with a bubble on the output, denoting that a complement opertaion is performed on th eoutput of the OR gate.

The schematic symbol and the truth table of NOR gate is shown in the figure 11.

Fig 11



Truth table

Input		Output
A	B	Y=$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

The output of NOR gate is '0' even if one of the input is in logic1. Only when both the inputs are in logic '0',the output is in logic '1'.

The IC 7402 is a TTL type NOR gate IC.It contains 4 NOR gates. For pin details of the IC refer to the data sheet of the IC.

EX-OR gate

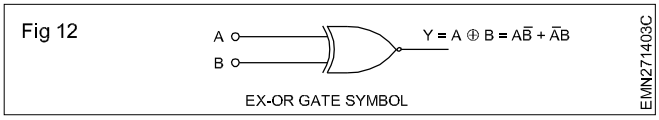
Exclusive-OR gate

Exclusive OR gate is actually formed by a combination of other gates already discussed. However, because of their fundamental importance in many applications, these gates are treated as basic logic elements with their own unique symbols.

The EX-OR gate has only two inputs unlike the other gates, it never has more than two inputs.

The schematic symbols of Exclusive-OR (XOR for short) is gate shown in Fig 12.

Fig 12



The truth table of EX-OR gate is given below.

Truth Table

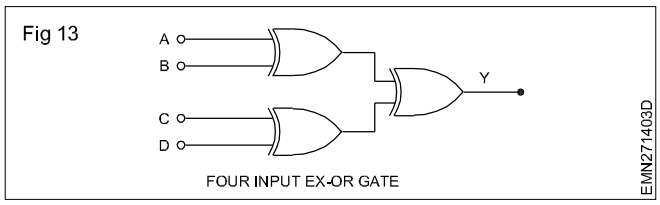
A	B	Q=A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

Using 2-input EX-OR gates as building blocks, an EX-OR gate with more than two inputs can be built as shown in Fig 13

Four input EX-OR gate

Y = A+B+C+D

Fig 13



Truth Table

A	B	C	D	Y	Remarks for input
0	0	0	0	0	Even
0	0	0	1	1	Odd
0	0	1	0	1	Odd
0	0	1	1	0	Even
0	1	0	0	1	Odd
0	1	0	1	0	Even

0	1	1	0	0	Even
0	1	1	1	1	Odd
1	0	0	0	1	Odd
1	0	0	1	0	Even
1	0	1	0	0	Even
1	0	1	1	1	Odd
1	1	0	0	0	Even
1	1	0	1	1	Odd
1	1	1	0	1	Odd
1	1	1	1	0	Even

To summarizes the action by referring truth table of 4-input XOR gate, each input word with an odd number of 1's produces a logic HIGH(1) output and for words with an even number of 1's it produces logic-Low(0) output. Because of this reason the EX-OR gate is used for parity check, IC 7486 is an quad 2 input EX-OR gate which is available both in TTL and CMOS family.

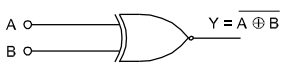
Application of EX- OR gate as a parity checker.

Parity is the term used to mention the number of 1's in a binary word. Even parity means an n-bit input has even number of 1s. For instance, 110011 has even parity because it contain four 1s. Odd parity means an n-bit input has an odd no. of 1s. For example, 110001 has odd parity because it contains three 1s.

Parity checker

Exclusive-OR gates are ideal for checking the parity of a binary number because they produce an output 1 when the input has an odd no. of 1s. Therefore an even parity

Fig 14



EX-NOR GATE SYMBOL

EMN271403E

input to an Exclusive-OR gate produces a low output, while an odd parity input produce a high output.

Exclusive-NOR gate

Inputs		Output
A	B	Q= A ⊕ B
0	0	1
0	1	0
1	0	0
1	1	1

The schematic symbols for the EX-NOR (XNOR) gate is shown in Fig 14. Like the XOR gate, XNOR has only two inputs. The bubble on the output of the XNOR symbol indicates that its output is opposite that of the XOR gate.

In an exclusive-NOR gate operation, "Output Q is LOW' if input A is LOW and input B is HIGH or if A is HIGH and B is LOW, Q is HIGH if A and B are both HIGH or both LOW.

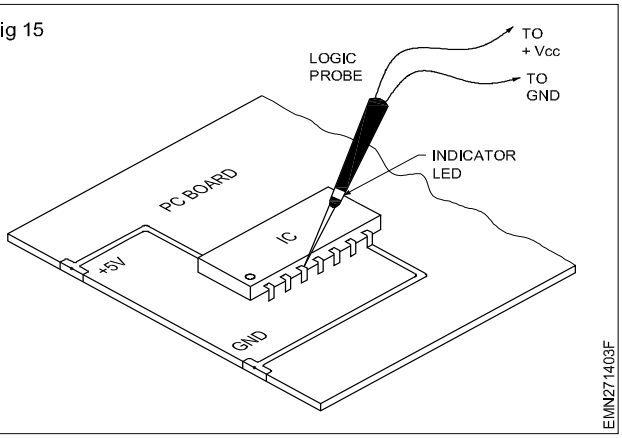
Application

EX-OR gate can be used as a controlled inverter. One of its inputs can be used to control whether the signal at the other input will be inverted or not. This property will be useful in certain application.

Logic probe

A logic probe is used to monitor the logic level activity at an IC pin or any other accessible point in a logic circuit. Logic probe normally has one or more indicator LEDs that indicate the various conditions of the logic signal. The indication may be related to logic HIGH, LOW, Intermediate & Pulsing states that are present at that point in the circuit which the probe tip is touching. Fig 15 shows how a logic probe is connected to an IC pin.

Fig 15



EMN271403F

A logic probe is used as a troubleshooting tool of digital systems. The most common internal failures of digital ICs are as follows

1 Malfunction in the internal circuitry.

2 Inputs or Outputs open circuited.

3 Inputs or Outputs shorted to ground or Vcc.

4 Short between two pins (other than ground or Vcc).

Malfunction in the internal circuitry

This is usually caused by one of the internal components failing completely or operating outside its specifications. When this happens the IC do not respond properly to the IC inputs. The behaviour of outputs cannot be predicted because it depends on what internal component has failed. This type of internal IC failure is not as common as other three.

Inputs shorted to ground or Vcc

This type of internal failure will cause the input to be struck in the LOW or HIGHstate. This kind of faults result short circuiting either with Vcc or ground depending on the state of input.

Outputs shorted to ground or Vcc

This type of internal failure will cause the output to be stuck in the LOW or HIGHstate. This type of failure has no effect on othe logic signals at the inputs.

Open circuited input or output

Sometimes very fine conducting wire that connects an IC pin to the ICs internal circuitry will break, producing an open circuit. The open gate will be in the floating state and this state will be assumed by TTL devices as a valid logic 1 and CMOS devices will respond erratically and may even become damaged from overheating.

Short between two pins

An internal short between two pins of an IC will force the logic signals at those pins always be identical. Whenever two signals that are supposed to be different show the same logic-level variatiions, there is a good possiblility that the signals are shorted together.

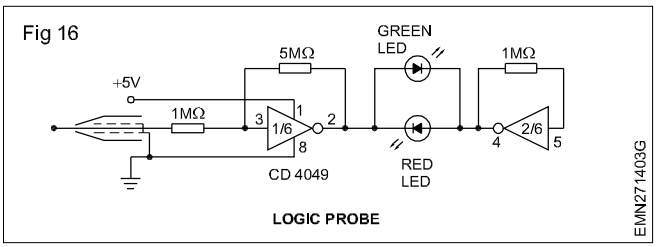
In most of the cases discussed above, a logic probe acts as a good troubleshooting tool to diagonise faulty circuits. Among other things, the logic probe is useful for locating short circuits that occur in manufacturing. For example during the stuffing and soldering of printed circuit boards, an undesirable splash of solder may connect two adjacent tracks. Known as solder bridge, this kind of trouble can short-circuit a node to the ground or to the supply voltage. The node is then stuck in a low or high state. The probe helps you to find short-circuited nodes because it stays in one state, no matter how the inputs are changing.

Logic probe circuit using inverters

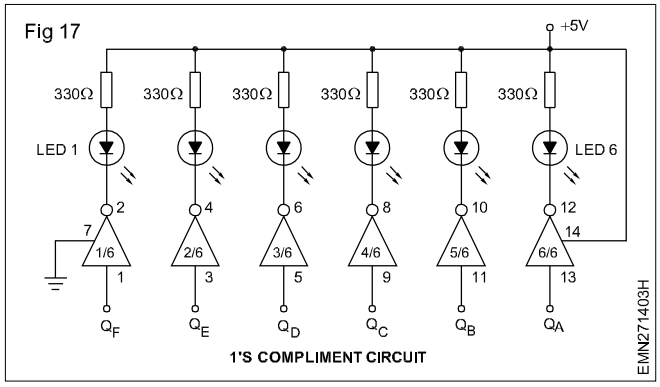
A simple circuit for indicating the logic levels using NOT gates is shown in Fig 2. The circuit consists of two inverters biased in the linear region. If the logic probe is connected to a 'low' level input, the 'high' going output of NOT gates makes LED-1 to glow. On the other hand, if the input probe is connected to a high level, the low going output of NOT gate makes LED-2 to glow. The two back to back connected LEDs protect each other against excessive reverse voltage. As the input impedance is very high, a shielded wire is required to connect the probe to the input of IC.

7404 is a TTL IC having six inverters inside, CD4011 is a CMOS IC having six inverters, refer table book for IC pin configuration.

1s complement circuit using inverter



The Fig 16 shows a circuit for producing the 1s complement of an 6-bit binary number. The bits of the binary number are applied to the inverter inputs and the 1s complement of the number appears at the o/ps. LED1 to LED6 indicate the status of inputs Q_F to Q_A. Logic 1 on any of the inverter inputs Q_F to Q_A, will make the output low causing corresponding LED to glow. If the LED glows, input to that particular inverter gate is high. In this matter the above circuit works as logic level indicator.Logic probe



An universal gate is a that can be used to implement any Boolean function without the need to use any other type of gate.

The NAND and NOR gates are universal gates.

In actual practice, teh NAND and NOR gates are used to fabricate all the basic gates required in IC digital logic famillies.

In practcie, an AND gate is typically implemented as a NAND gate followed by an inverter not the other way around.

In the some way an OR gate is typically implemented as a NOR gate followed by a NOT gate.

Now let us discuss how to implement the NOT,AND,and OR gates using universal gate.

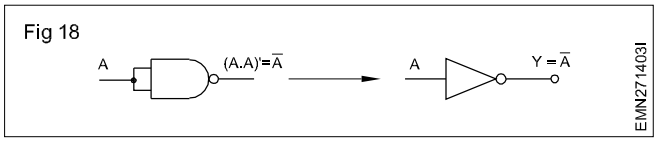
NAND gate as a universal gate:

To prove that any Boolean function can be implemented usinmg only NAND gates,we will show that the AND,OR, and NOT operations can be performed using only these gates.

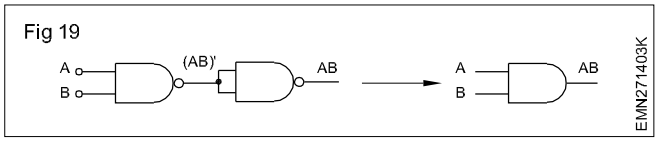
NAND gate implemented as NOT gate.

In the following circuit NAND gate is used as **an inverter (NOT gate).**

All input pins of NAND gates are connected to the input signal A gives an output A as shown in Fig 18.

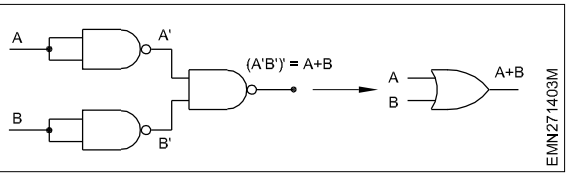


NAND gate implemented as AND gate. An AND gate can be implemented by NAND gate as shown in figure19. (The AND is replaced by a NAND gate with its output complemented by a NAND gate inverter).



NAND gates implemented as OR gate. An OR gate can be implemented by NAND gates as shown in figure20. (The OR gate is replaced by a NAND gate with all its inputs complemented by NAND gate inverters).

Fig 20



Thus it is proved that the NAND gate is auniversal gate since it can implement the AND, OR and NOT logic functions.

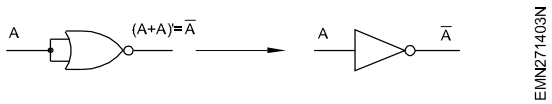
NOR gate as a universal gate. In the following paragraphs the NOR gate is used to prove that any Boolean function can be implemented only with NOR gates.NOR to replace the AND,OR and NOT opertaions .

NOR gate implemented as NOT gate.In the following circuit a NOR gate is used as **an inverter (NOT gate).**

All input pins of NOR gate is connected to the input signal

A gives an output $\overline{A}$ as shown in Fig 21.

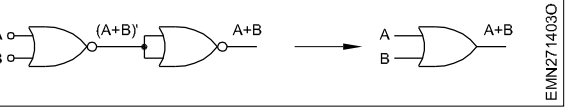
Fig 21



NOR gate implemented as AND gate.

An OR gate can be implemented by NOR gates as shown in figure22.(The OR is replaced by a NOR gate with its output complemented by a NOR gate inverter)

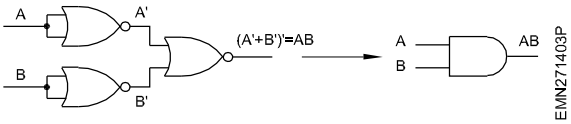
Fig 22



NOR gate implemented as AND gate

An AND gate can be implemented by NOR gates as shown in the figure 23.(The AND gate is replaced by a NOR gate with all its inputs complemented by NOR gate inverters)

Fig 23



Thus it is proved that the NOR gate is a universal gate since it can implement the AND, OR and NOT logic functions.

Heat Sink used in electrical and electronic component

In any electrical circuit some amount of heat while the circuit is functioning.Typically power handling semiconducter devices like power transistors and the opto electronics such as light emitting diodes, lasers generate heat in considerable amounts and these components are inadequate to dissipate heat,as their dissipation capability is signnificantly low.

Due to this, heating up of the components leads to malfuncting problems and may cause failure of the entire circuit or system's performance.So,to solve these problems, heat sinks are the solution that must be provided to those semiconductor devices for cooling purpose.

Heat sink is a device made of aluminium metal attached of an electronic circuit , that dissipates heat mainly from the power transistors of a circuit into the surrounding medium and cools them for improving their performance, reliability and also avoids the damage to the components. For the cooling purpose, it incorporates a fan or cooling device.

Whenever two objects with different teperature come into contact with each oher, conduction occurs causing the fast- moving molecules of the high - heat object to collide with the slow- moving molecules of the cooler objects, and thus, transfers thermal energy to the cooler object, and this is termed as thermal conductivity.

Similarly, heat sink transfers the heat or thermal energy from a high- temperature component to a low- temperature medium like air.

The heat sinks are classified into different categories based on different criteria. Let us consider the major types,namely active heat sinks and passive heat sinks.

Binary arithmetic

Objectives : At the end of this lesson you shalll be able to

- **define binary arithmetic**
- **perform binary addition**
- **perform binary subtraction using 1's compliment and 2's compliment**
- **explain half adder circuit, full adder circuit**
- **explain 4 bit parallel adder circuit using IC 74LS83**
- **explain IC 74LS83 4 bit parallel adder can be used for subtraction.**

Binary arithmetic is essential in all digital computers and in many other types of digital systems. To understand digital systems, you must know the basics of binary addition, subtraction, multiplication and division.

Binary addition

Physical quantities are represented by numbers. Addition represents combining of physical quantities. Digital computers do not process decimal numbers, they process binary numbers. Addition is a key process to perform subtraction, multiplication and division. The four basic cases for adding binary digits are as follows.

0 + 0 = 0; Sum is 0 with a carry of 0.

0 + 1 = 1; Sum is 1 with a carry of 0.

1 + 0 = 1; Sum is 1 with a carry of 0.

1 + 1 = 10; Sum is 0 with a carry of 1.

Notice that the first three cases result in a single bit and in the forth case the addition of two 1's yields a binary two i.e. 10. When binary numbers are added, the last condition creates a sum of 0 in a given column and a carry of 1 over to the next column to the left, as illustrated in the following addition of 11 + 01.

carry	1	1	
	0	1	1
+	0	0	1
	1	0	0

In the right most column, 1+1=0 with a carry of 1 to the next left column. In the middle column, 1+1+0=0 with a carry of 1(one) to the next left column. In the left most column, 1 remains as final carry of the 2 bit addition. Hence the result is 100.

Example:

1		carry	1110
	14		1110
	10		1010
	24		11000
2	10 + 12		
	10		1010
	12	+	1100
	22		10110

The above process is column-by-column addition which can be applied to find the sum of two binary numbers of any length. The following example shows 8-bit arithmetic addition operation.

$A_7A_6A_5A_4A_3A_2A_1A_0$

$B_7B_6B_5B_4B_3B_2B_1B_0$

———————

?

———————

The most significant bit (MSB) of each number is on the left side and least significant bit is on the right side. For the first number, A7 is the MSB and A0 is the LSB, similarly for the 2nd number B7 and B0 are the MSB and LSB respectively.

Signed numbers

Digital systems such as the computer, must be able to handle both +ve and -ve numbers, A signed binary numbers consists of both sign and magnitude information. The sign indicates whether a number is +ve or -ve and the magnitude is the value number. There are three ways in which signed numbers can be represented in binary form: sign magnitudes, 1s compliment, and 2's compliment.

Sign-magnitude system

The left most bit in a signed binary number is the sign bit, which tells you whether the number is +ve or -ve, A zero in the left most position represents +ve number and a ONE represents -ve number. The remaining bits are the magnitude bits. The magnitude bits are in true (uncomplimented) binary form for both +ve and -ve numbers.

Example:

+25 is expressed as an 8 bit signed binary number using the sign magnitude system as

+ 25 = 0 0 0 1 1 0 0 1

Sign bit Magnitude bit

- 25 = 1 0 0 1 1 0 0 1

Notice that the only difference between +25 and -25 is with the sign bit because the magnitude bits are same for both +ve and -ve numbers.

"In the sign-magnitude system, a -ve number has the same magnitude bits as the corresponding +ve number but the sign bit is a 1." Although sign magnitude system is straight forward, calculators and computers do not use it, because circuit implementation is more complex than other systems.

1's complement system

Positive numbers in the 1's complement system are represented the same way as the positive sign magnitude numbers. In the 1's complement system, a negative number is the 1's compliment of the corresponding +ve number.

Example:

The decimal number -25 is expressed as the 1's compliment of +25 (00011001) as 11100110.

i.e 1's compliment of 00011001 (+25) = 11100110 (-25)

(The 1's compliment of a binary number is obtained by simply changing each 0 to a 1 and each 1 to a 0).

Example:

Determine the decimal value of the signed binary numbers expressed in 1's compliment.

1 1 1 0 1 0 0 0

The bits and their powers of two weights for the -ve number are as follows.

Notice that the -ve sign bit has a weight of -2^7 or -128.

-2^{+7}	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	1	0	1	0	0	0

Summing the weights where there are 1s.

1 x -2^7 (128) = -128

1 x 2^6 (64) = +64

1 x 2^5 (32) = +32

1 x 2^3 (8) = +8

= -128+104

= -24

Adding 1 to the result, the final number is = -24 + 1 = -23.

The decimal value of the signed number 11101000 expressed in 1's compliment is = - 23.

2's compliment system

Positive numbers in the 2's complement system are also represented the same way as in sign magnitude and 1's complement system. Negative numbers are 2's complement of the corresponding positive no's.

2's compliment of a binary number is found by adding ONE(1) to the LSB of the 1's compliment.

2's Compliment = (1's compliment) + 1

Example:

Find the 2's compliment of 1011011

Solution

1011011	-	Binary number
0100100	-	1's compliment
1	-	Add 1
+ 0100101		

For example, the decimal number -25 can be expressed in binary form by writing 2's complement for +25.

+25 = 00011001	-	Binary number
11100111	-	2's compliment

Example:

Express the decimal -39 as an 8 bit number in sign-magnitude using 2's compliment system.

Solution

In the 2's compliment system, -39 is produced by taking the 2's compliment of +39 (00100111) as follows.

+39 =	00100111		Binary number
	11011000		1's compliment
+	1		
-39 =	11011001		2's compliment

Verification =

-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
-128	64	32	16	8	4	2	1
1	1	0	1	1	0	0	1

Since the MSB of the binary equivalent is one so, 2^7 should be taken as -ve sign.

-128+64+16+8+1 = -128+89

= -39

The 2's complement system is preferred for representing signed numbers as it requires a summation weights regardless of whether the number is +ve or -ve. It is used in most computers because it makes arithmetic operations earier.

Basic Adder

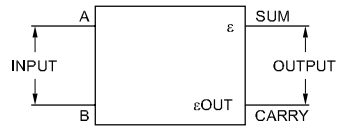
Adders are used in many types of digital systems in which numerical data are processed. Computers and calculators perform binary operations on two binary numbers at a time, where each number can have several binary digits. The logic symbol for a half adder is shown in Fig 1. There are two basic categories of adders.

1 Half adder

2 Full adder

Half adder

Fig 1



The half-adder accept two binary digits on its inputs and produces two binary digits on its outputs, a sum bit and a carry bit.

Table 1 (Truth table)

A	B	Sum $S=A + BC_{out} = AB$	Carry
0	0	0	0
0	1	1	0
1	0	1	0

1	1	0		1

From the logic operation of the half-adder as stated in the Table 1, expression can be derived for the sum and the output carry as functions of the inputs, notice that the output carry is a 1 only when both A and B are 1s. Therefore carry (C_{out}) can be expressed as the AND of the input variables.

$C_{out} = A.B$ ——> 1

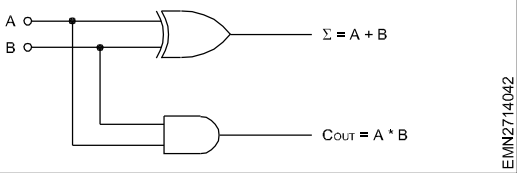
The sum output(S) is a 1 only if the input variables, A and B are not equal. The sum can therefore be expressed as the exclusive -OR of the input variables.

Sum(S) = A + B ——> 2

From equation 1 and 2 the logic implementation required for the half-adder function can be developed. The output carry is produced with an AND gate with 'A' and 'B' on the inputs and the sum outputs is generated with an Ex-OR gate, as shown in Fig 2.

Full adder

Fig 2

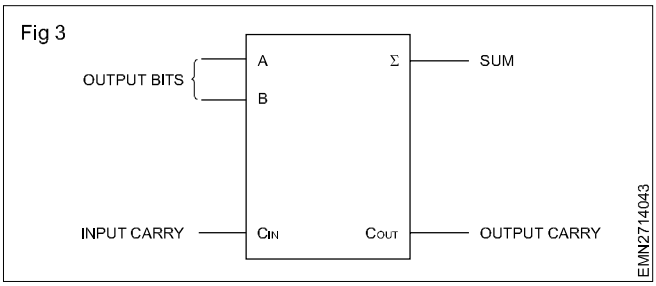


The full adder accepts three inputs including an input carry and generates a sum output and an output carry.

The basic difference between a full-adder and a half-adder is that the full-adder accepts an input carry. A logic symbol for a full-adder is shown in Fig 3 and the truth table in the Table 2 shows the operation of a full-adder.

Table 2

Fig 3



A	B	C_{in}	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The full-adder must add the two input bits alongwith the input carry. From the truth-table of the half-adder we know that the sum of the input bits A and B is A + B. To get the sum output of the full edder the input carry (C_{in}) must be exclusive-ORed with A + B. Then the sum

$S = (A + B) + C_{in}$

This means that to implement the full-adder sum function, two exclusive-Or gates can be used. The first must generate the term A + B, and the second has the inputs from the output of the XOR gate and the input carry, as shown in Fig 4.

The output carry of the full-adder is therefore produced by the inputs A, ANDed with B and A + B ANDed with C_{in}. These two terms are ORed, and expressed in equation shown below and this function is implemented and combined with the sum logic to form a complete full-adder circuits, as shown in Fig 4.

2 Bit parallel adder (para)

$C_{out} = AB + (A + B) C_{in}$

Fig 4

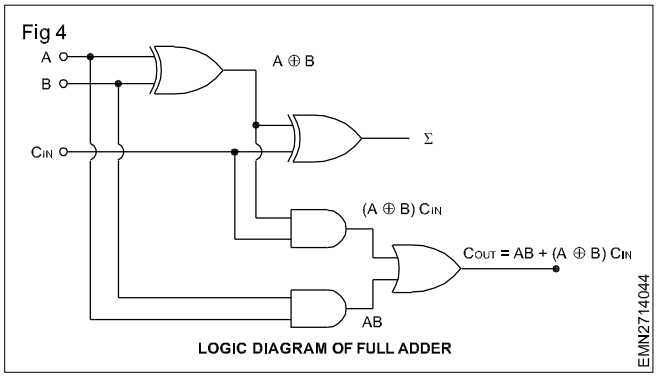
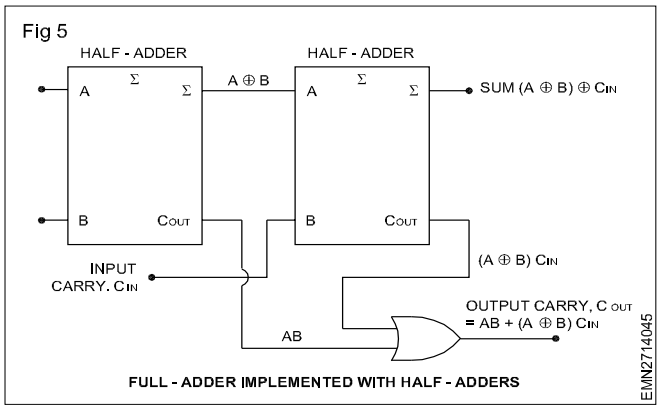


Fig 5



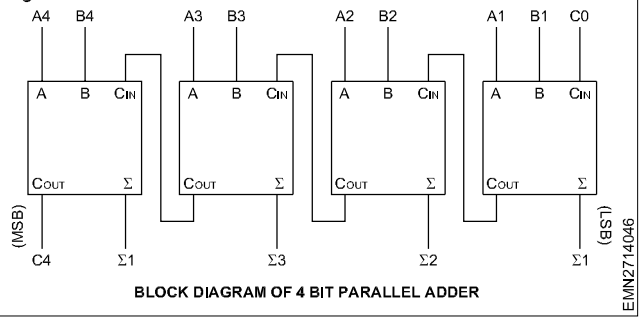
The Fig 5, shows there are two half-adders, connected as shown in block diagram to form full-adder.

Four bit parallel adder

A basic 4-bit parallel adder is implemented with four full-adders as shown in the Fig 6.

Block diagram of 4 bit parallel adder

Fig 6



BLOCK DIAGRAM OF 4 BIT PARALLEL ADDER

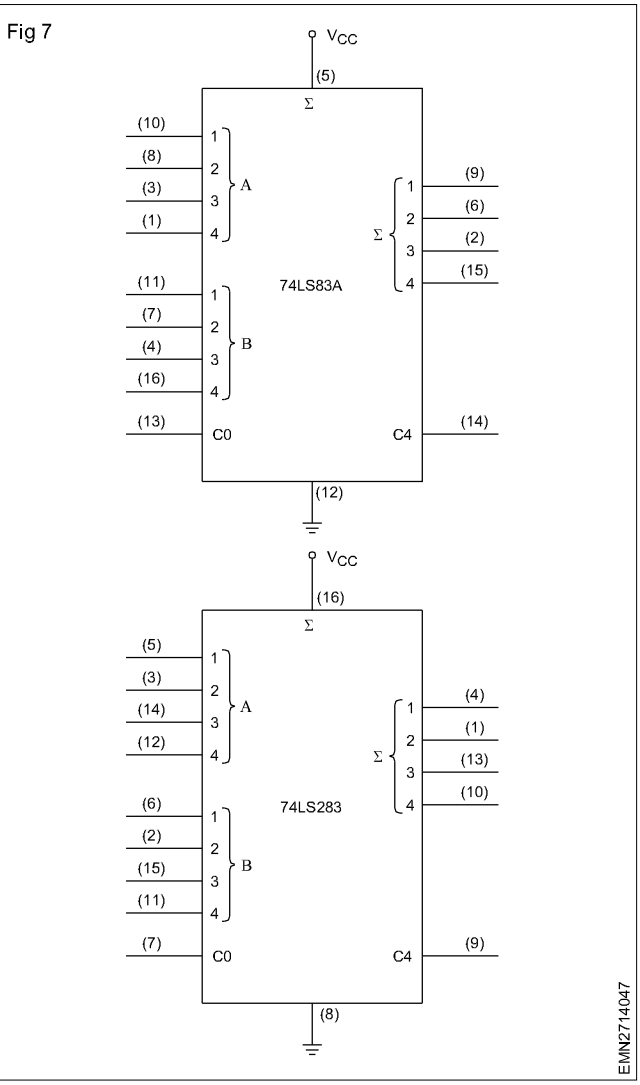
The LSB, (A1 and B1) in each number being added into the right most full-adder; the higher order bits are applied as shown to the successively higher order adders, with MSBs (A4 and B4) in each number being applied to the left most full adder. The carry output of each adder is connected to the carry input of the next higher order adder as indicated.

In the manufacturer's data sheets the input labeled C_0 is the input carry to the least significant bit adder, C_4 is the output carry of the most significant bit adder, and S_1(LSB) through S_4(MSB) are the sum outputs.

74LS83 4 bit parallel adder

4-bit parallel adders that are available as Medium-Scale Integrated(MSI) circuits are the 74LS83A and the 74LS283

Fig 7



low-power Schottky TTL devices. These devices are also available in other logic families such as standard TTL (7483A and 74283) and CMOS (74HC283). The 74LS83A and the 74LS283 are functionally identical to each other but not pin compatible, that is the pin numbers for the inputs and outputs are different due to different power and ground pin connections. For the 74LS83A, V_{CC} is pin 5 and ground is pin 12 on the 16-pin package. For the 74LS283, V_{CC} is pin 16 and ground is pin-8, which is a more standard configuration. Logic symbols for both of these devices are shown in Fig 7 with pin numbers in parenthesis.

The 4 bit parallel adder can be expanded to handle the addition of higher bit numbers by a process called cascading. In this process, the carry output of the lower-order adder is connected to carry input of the higher-order adder being cascaded.

Binary subtraction

Subtraction is a special case of addition. For example Subtracting +6 (the subtrahend) from +9 (the minuend) is equivalent to adding -6 to +9. Basically the subtraction operation changes the sign of the subtrahend and adds it to the minuend. The result of a subtraction is called the difference.

9 - 6 = 9+(-6)

The sign of a positive or negative binary number is changed by taking its 2's compliment.

Example:

The result of 2's compliment of the positive number 0110(+6) is 1's compliment of the number + 1

i.e 1001 + 1 = 1010

1010 is 2's compliment of 0110(+6), which is equal to -6 in decimal system, as shown below.

1 0 1 0

-8 + 0 + 2 + 0 = -6

Example:

Subtract 6 from 9 in 2's compliment method

9-6 = 3 normal method

9+(-6) = 3 2's compliment method

Binary form

9 = 1001 (minuend) 1001 - 0110 = 0011

6 = 0110 (subtrahend)

2's compliment method

I step: 2's compliment of subtrahend 0110 is

1's compliment of subtrahend + 1

i.e 1001 + 1 = 1010 (equal to -6 in decimal system)

II step: Add minuend with 2's compliment of subtrahend

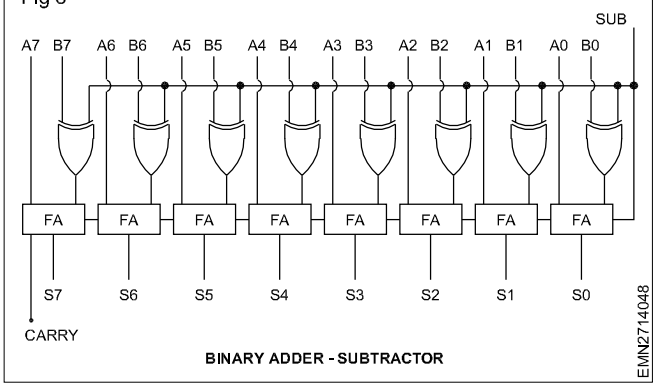
i.e 1001 + 1010 = 10011

Discard the carry 1, then the result is 0011.

Adder-Subtracter

Full adder can be used for to add or subtract binary numbers. The Fig 8 shows the how adder circuit can be used as subtractor.

Fig 8



The carry out from each full adder is the carry into the next-higher full adder. The numbers being proposed are A_7....A_0 and B_7.....B_0 while the output sum is S_7.....S_0. With 8 bit arthimetic, the final carry is ignored. With 16-bit arthimetic, the final carry is the carry into the addition of the upper byte.

Addition

A_7.....A_0

+ B_7.....B_0

———————

S_7.....S_0

———————

During an addition, the SUB signal is deliberately kept in the low state, therefore the binary number B_7.....B_0 passes through the controlled inverter (through Ex-OR gate) with no change. The full-adders then produce the correct output SUM.

For instance, suppose that the numbers being added are +125 and -67, then $A_{7.....A0}$ = 01111101 and B_7.....B_0 = 10111101.

Since SUB=0 during an addition, the CARRY IN to the LSB column is 0.

0	<—— Sub input
01111101	<—— Input 'A'
+ 10111101	<—— Input 'B'
————————	
100111010	
————————	

During 8 bit arithmetic operation 'last carry' is ignored, therefore the answer is S_7.....S_0 = 00111010.

Subtraction

A_7.....A_0 (minuend)

(-) B_7.....B_0 (subtrahend)

———————————-

S_7.....S_0

———————————-

During the subtraction, the SUB signal is deliberately put into high state. Therefore the controlled inverter (Ex-OR gates) produces the 1's compliment of 'B' inputs, because the SUB is the carry IN, to the first full-adder (tied to logic-1) circuit processes the data as given.

1 <—SUB

A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0

\+ B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0

———————————————-

S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0

———————————————-

When A_7.....A_0 is applied with all zeros the circuit produces the 2's compliment of B_7.....B_0 because 1 is being added to the 1's compliment B_7.....B_0, when A_7.....A_0 doesn't equal zero the effect is equivalent to adding A_7.....A_0 and the 2's compliment of B_7.....B_0.

Example:

(A - B)

82 - 17

A B S

= 01010010 - 00010001 = ?

The controlled inverter produces the 1's compliment of B, which is 11101110, since SUB=1 during a subtraction, the circuit performs the following condition.

1	<—— SUB
01010010	<—— A input
11101110	<—— B input
————————	
101000001	<—— S output
————————	

For 8-bit arithmetic, the final carry is ignored, therefore the answer is S_7.....S_0 = 01000001.

This answer is equivalent to decimal +65 which is the algebraic difference between the number +82 and +17.

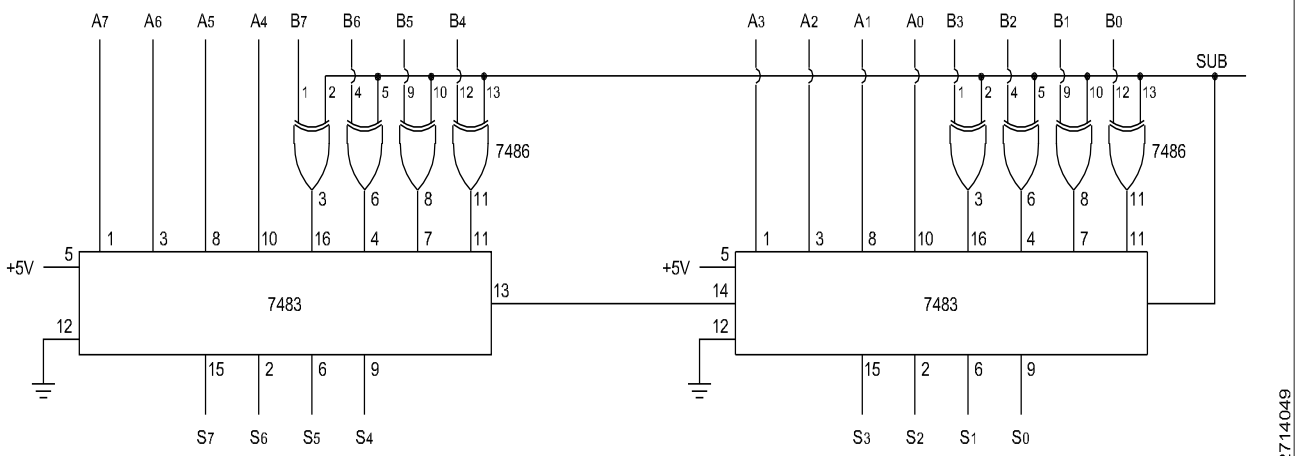
Subtraction circuit based on 2's compliment method using Adder IC

In this circuit the Minuend is applied to the A inputs of IC 7483 and Subtrahend is fed to the B inputs, through EX-OR gates and output is taken at S outputs, as shown in Fig9.

The IC 7486 is on Exclusive-OR gate used for 1's complimenting the SUBTRAHEND.

Carry input and one input from each Ex-or-gate is tied to some logic status. For addition SUB input should be logic-0, for subtraction sub input should be at logic-1 state.

Fig 9



TWO 7483s CAN ADD OR SUBTRACT BYTES

Digital comparator [Magnitude comparators]

Another common and very useful combinational logic circuit is that of the **Digital Comparator** circit.

Digital or Binary compartors are made up from standard AND,NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs.

The digital comparator accomplishes this using several logic gates that operate on the principles of Boolean Algebra. There are two main types of Digital Comparator available and these are.

1. Identity comparator - an identity comparator is a digital comparator with only one output terminal for when A =B, either A=B, either A= B = 1 (HIGH) or A =B= 0 (LOW)

2.Magnitude comparator - a Magnitude comparator is a digital comparator which has three output terminals, one each for equality, A = B greater than, A > B and less than A<B

The purpose of a Digital Comparator is to compare a set of variables or unknown numbers, for example A (A1,A2,A3,.....An, etc) against that of a constant or unknown value such as B (B1,B2,B3,.....Bn, etc) and produce.

1 - bit Digital comparator circuit

The operation of a 1- bit digital comparator is shown in the the below truth table.

Digital Comparator Truth Table

Inputs		Outputs		
B	A	A>B	A=B	A<B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

In the circuit does not distinguish between either two “0” or two “1” ‘s as an output A=B is produced when they are both equal, either A = B= “0” or A = B= “1”. the output condition for A=B resembles that of a commonly avilable logic gate, the Exclusive -NOR or Ex - NOR function (equivalence) on each of the n-bits giving : Q =A + B

Digital comparators actually use Exclusive - NOR gates within their design for comparing their respective pairs of bits. When we are comparing two binary or BCD values or variables against each other, we are comparing the “Magnitude” of these values, a logic “0” against a logic “1” which is where the term Magnitude Comparator comes from.

As well as comparing individual bits, we can design larger bit comparators by cascading togethern of these and produce a n - bit comparator just as we did for the n-bit adder in the previous tutorial. Multi - bit comparators can be constructed to compare whole binary or BCD words to produce an output if one word is larger, equal to or less than the other.

A very good example of this is the 4- bit Magnitude Comparator. Here, two 4 - bit words (“nibbles”) are compared to each other to produce the rrelevant output with one word connected to inputs A and the other to be compared.

4 - bit Magnitude comparator

Some commercially available digital comparators such as the TTL 74LS85 or CMOS 4063 4 - bit magnitude comparator have additional input terminals that allow more individual comparators to be “cascaded” together to compare words larger than 4 - bits with magnitude comparators of “n” - bits being produced. These cascading inputs are connected directly to the corresponing outputs of the previous comparator as shown to compare 8,16 or even 32-bit words.

8 - bit word comparator

When comparing large binary or BCD numbers like the example above, to save time the comparator starts by comparing the highest - order bit (MSB) first. If equality exists, A = B then it compares the next lowest bit and so on until it reaches the lowest - order bit, (LSB).If equality still exists then the two numbers are defines as being

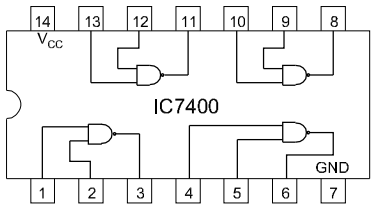
equal.

If inequality is found, either A> B or A<B the relationship between the two numbers is determined and the comparison between any additional lower order bits stops.

Digital Comparator are used widely in Anlogue - to - Digital converters, (ADC) and Arithmetic Logic Units, (ALU) to perform a variety of arithmetic operations.

PIN DIAGRAM OF LOGIC ICs

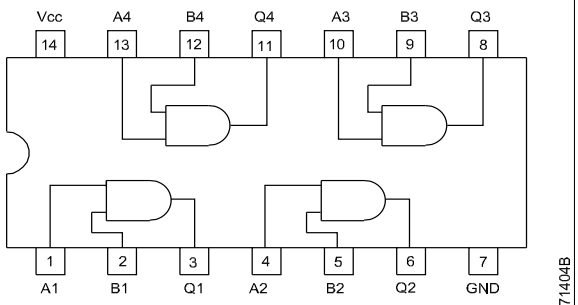
Fig 10



PINOUT DIAGRAM OF IC7400

EMN271404A

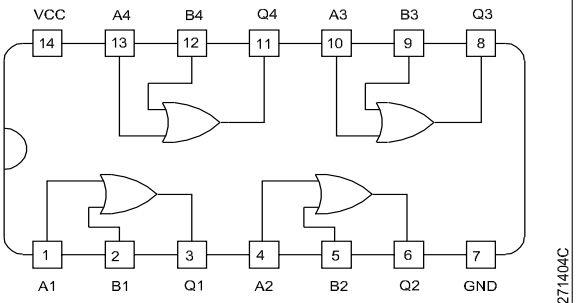
Fig 11



AND GATE IC 7408

EMN271404B

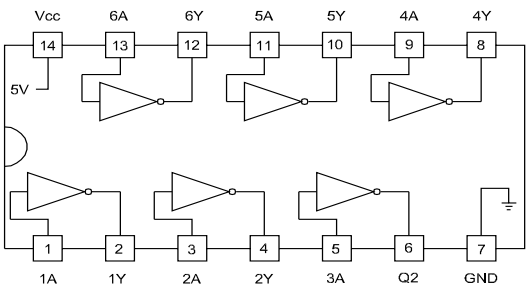
Fig 12



OR GATE IC 7432

EMN271404C

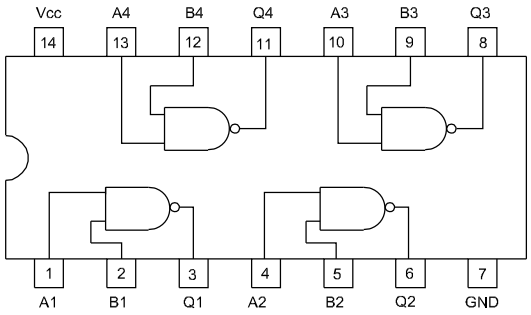
Fig 13



NOT GATE IC 7404

EMN271404D

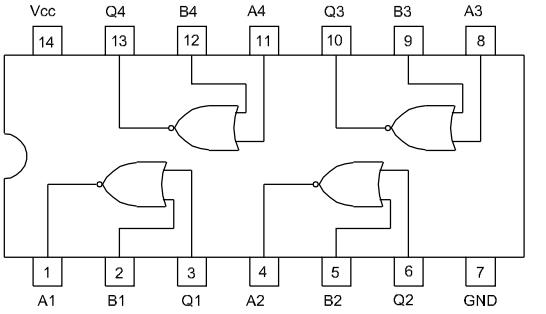
Fig 14



NAND GATE IC 7400

EMN271404E

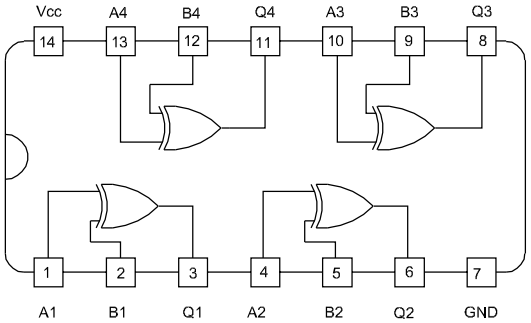
Fig 15



NOR GATE IC 7402

EMN271404F

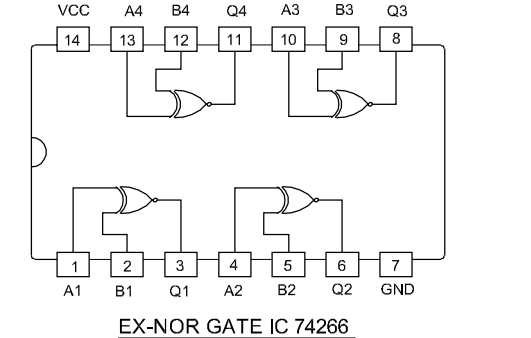
Fig 16



EX-OR GATE IC 7486

EMN271404G

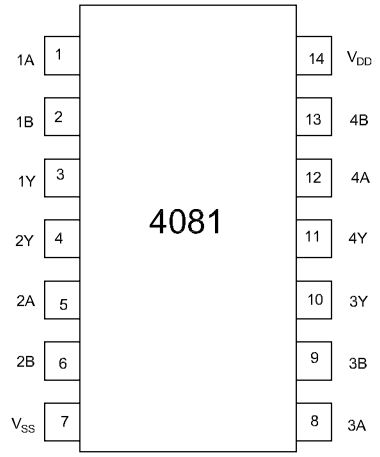
Fig 17



EX-NOR GATE IC 74266

EMN271404H

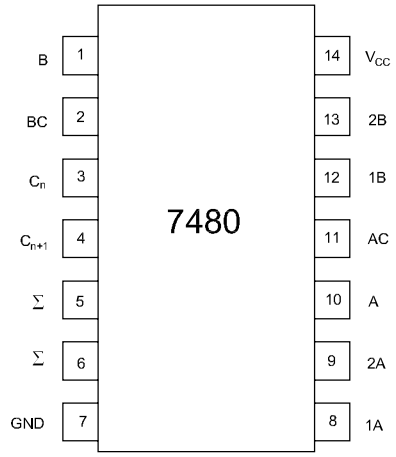
Fig 18



HALF ADDER IC 4081

EMN271404I

Fig 19



FULL ADDER IC7480

EMN271404J

Concept of encoder and decoder

Objectives : At the end of this lesson you shalll be able to

- **concepte of encoder and decoder**
- **explain 2 to 4 binary decoder its working**
- **explain 4 to 2 binary encoder and its working.**

Concept of encoder and decoder

The encoders and decoders play an essential role in digital electronics.

- Encoders & decoders are used to convert data from one from to another form.
- These are frequently used in communication system such as telecommunication, networking, etc... to transfer data from one end to the other end.
- Similarly, in the digital domain, for easy transmission of data, it is often encrypted or placed within codes, and then transmitted. At the receiver, the coded data is decrypted or gathered from the code and is processed in order to be displayed or given to the load accordingly.

Binary Encoder

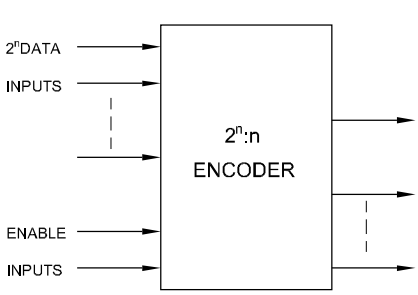
A binary encoder is shown in Fig 1. It has 2^n input lines and n output lines, hence it encodes the information from 2^n inputs into an n- bit code. From all the input lines, only one of an input line is activated at a time, and depending on the input line, it produces the n bit output code.

The figure below shows the block diagram of binary encoder which consists of 2^n input lines and n output lines. It translates decimal number to binary number.

The output lines of an encoder correspond to either true binary equivalent or in BCD coded form of the binary for the input value. Some of these binary encoders include decimal to binary encoders, decimal to octal, to binary encoders, decimal to BCD encoders, ect.

Depending on the number of input lines, digital or binary encoders produce the output codes in the form of 2 or 3 or 4 bit codes.

Fig 1



2^n:n ENCODER

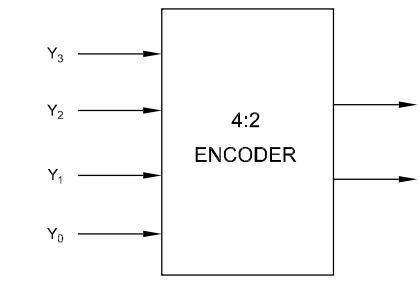
EMN2714051

4 - to - 2 Bit Binary Encoder

The block diagram and truth table of a 4 input encoder is shown in Fig 2. The truth table consists of four rows, since, it is assumed that only one input is the value of 1 then the corresponding binary code associated with that enabled input is displayed at the outputs.

The output Y_0 is 1 when either input Y_1 or Y_3 is 1, also the output Y_1 is set to 1 when either input Y_2 or Y_3 is 1.

Fig 2



4:2 ENCODER

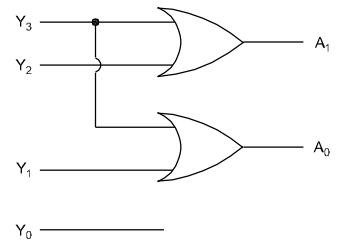
EMN2714052

Y_3	Y_2	Y_1	Y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

The output from 4-to-2 encoder is generated by the logic circuit implemented by a set of OR gates as shown in Fig 3. In the figure a, the output of the encoder is same if input activated is the lo input (Io =1) or if no input is activated i.e. all the inputs are zero.

This causes ambiguity in the encoding output. To avoid this ambiguity, a valid encode output can be added as an additional output assumes a value 1 when lo is equal to 1.

Fig 3



4 to 2 ENCODER USING OR GATES

Decimal to BCD Encoder

This type of encoder usually consists of ten input lines and 4 output lines, Each input line corresponds to the each decimal digit and 4 outputs correspond to the BCD code.

This encoder accepts the decoded decimal data as an input and encodes it to the BCD output which is available on the output lines.

The figure below shows the basic logic symbol of decimal to BCD encoder along with its truth table. The truth table represents the BCD code for each decimal digit.

From this we can formulate the relationship between the BCD bit and decimal digit. It is important to note that there is no explicit input line for decimal zero. When this condition occurs, i.e. decimal inputs 1 to 9 all are zero. than the BCD output is 0000.

Binary Decoder

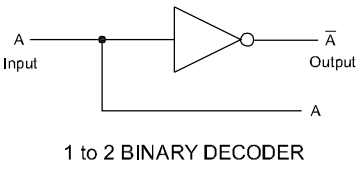
The **Binary Decoder** is another combinational logic circuit constructed from individual logic gates and is the exact opposite to that of an Encoder

The name "Decoder" means to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an equivalent decimal code at its output.

Binary Decoders are another type of digital logic device tha t has inputs of 2 - bit or 3- bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an n - bit code, and therefore it will be possible to represent 2^n possible values. Thus,a decoder generally decodes a binary value into a non - binary one by setting exactly one of its n outputs to logic "1".

If a binary decoder receives n inputs (usually grouped as a single Binary or boolean number) it activates one and only of its 2^n outputs based on that input with all other outputs deactivated.

Fig 4



1 to 2 BINARY DECODER

So for example, an inverter (NOT - gate) can be clased as a 1- to -2 binary decoder as 1 - input and 2- output (2^1) is possible because with an input A it can produce two outputs A and (not - A) as shown in Fig 1.

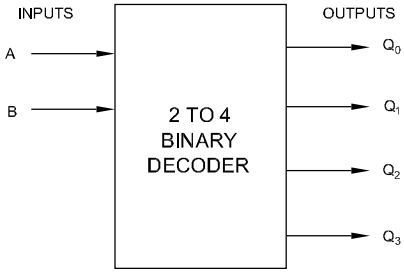
Then we can say that a standard combinational logic decoder is an **n- to - m** decoder, when $m \leq 2^n$, and whose output , Q is dependent only on its current inputs, determines which binary code or binary number is corresponds to that binary input.

A Binary Decoder converts coded inputs into coded outputs, where the input and output codes are different and decoders are available to "decode" either a binary or BCD (8421 code) input pattern to typically a decimal output code. Commonly available BCD - to - Decimal decoders include the TTL 7442 or the CMOS 4028. generally a decoders output decoder" circuits include, 2- to- 4, 3- to - 8 and 4- to -16 line configurations.

An example of a 2- to -4 line decorder along with its truth table is shown in Fig 5a and 5b.

A2-to-4 Binary Decoder

Fig 5



(b)

A	B	Q_0	Q_1	Q_2	Q_3
0	0	**1**	0	0	0
0	1	0	**1**	0	1
1	0	0	0	**1**	0
1	1	0	0	0	**1**

This simple example above of a 2- to-4 line binary decoder consists of an array of four AND gates. The 2 binary inputs labelled A and b are decoded into one of 4 outputs, hence the description of 2- to -4 binary decoder.

This simple example above of a 2- to-4 line binary decoder consists of an array of four AND gates. The 2 binary inputs labelled A and b are decoded into one of 4 outputs, hence the description of 2- to -4 binary decoder. Each output represents one of the miniterms of the miniterms of the 2 input variables, (each output = a miniterm).

The binary inputs A and B determine which output line from Q0 to Q3 is “HIGH” at logic level “1” while the remaining outputs are held “LOW” at logic “0” so only one output can be active (HIGH) at one time. Therefore, whichever output line is “HIGH” identifies the binary code present at the input, in other words it “de - codes” the binary input.

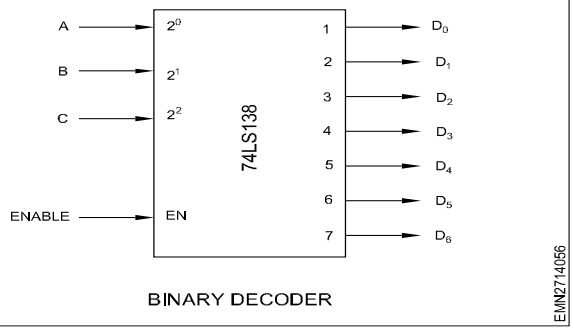
Some binary decoders have an additional input pin labelled “Enable” that controls the outputs from the device. This extra allows the decoders outputs to be turned “ON” or “ “OFF” as required. These types of binary decoders are commonly used as “memory adderss decoders” in microprocessor memory applications.

The binary decoder is a demultiplexer with an additional data line that is used to enable the decoder. An alternative way of looking at the decoder circuit is to regard inputs A,B and C as address signals. Each combination of A,B or C defines a unique memory address.

A 2-to-4 line binary decoder (TTL 74155)can be used for decoding any 2-bit binary code to provide four outputs, one for each possible input combination. However, sometimes it is required to have a Binary Decoder with a number of outputs greater than is available, so by adding more inputs, the decoder can potenially provide 2^n more outputs as show in Fig 6.

So for eample, a decoder with 3 binary inputs (n=3), would produce a 3-to- 8 line decoder (TTL 74138) and 4 inputs (n = 4) would produce a 4-to-16 line decoder (TTL 74154) and so on. But a decoder can also have less than 2^n outputs

Fig 6



such as the BCD to sevensegment decoder (TTL 7447) which has 4 inputs and only 7 active outputs to drive a display rather than the full 16 (2^n) outputs as you would expect.

Here a much larger 4 (3 data plus 1 enable) to 16 line binary decoder has been implemented using two smaller 3-to-8 decoders.

An encoder is device which converts familar numbers or characters or symbols into a coded format. it accepts the alphabetic characters and decimal numbers as inputs and produces the outputs as a coded representation of the inputs.

It encodes the givesn information into a more compact form. In other words,it is a combinatiaonal circit that performs the opposite function of a decoder.

These are mainly used to reduce the number of bits needed to represent given information. In digital systems, encoders are used for transmitting the information. Thus the transmission link uses fewer lines to transmit the encoded information.

In addition, these encoders are used for encoding the data which is to stored for later use asit facilitates fewer bits storing over the available space.

Multiplexers & Demultiplexers

Objectives : At the end of this lesson you shalll be able to

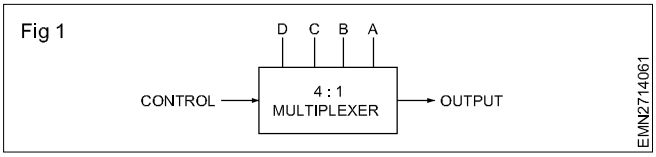
- **state the need of multiplexers and demultiplexers in digital circuits**
- **explain the function of a multiplexer with an example**
- **state the relationship between number of input lines and required number of control lines**
- **list a few commercially available multiplexer and demultiplexer ICs**
- **explain the application of a multiplexer & demultiplexer in data transmission**
- **explain Four to One line multiplexer and its working**
- **explain One to Four Demultiplexer and its working.**

Many applications in digital logic requires circuit with multiple input and single output, single input and multiple outputs. The output of such circuits should however be uniquely determined by a set of control signals. Such circuits find immense application in computer and data transmission. Such circuits that have one or more input lines and give one or more output which are uniquely determined by the inputs are called *Combinational circuits.* Two of the most important combinational circuits are the Multiplexers and Decoders.

Multiplexers

A multiplexer having 2^n data inputs, one data output and an *n*-bit control input which selects one of the input and routes it to the output is shown in Fig 1.

Fig 1



In Fig 1, the multiplexer has two inputs ($2^n = 2^1=2$, hence n=1). It has 1-bit control signal (because, n=1) which selects A or B as the output as given in the Truth Table 1.

Truth Table

INPUTs		Control	Output
A	B		
1	0	0	1 (A -->output)
1	0	1	0 (B -->output)

Demultiplexer

The inverse of a Multiplexer is a Demultiplexer as shown in Fig-2. This has n input (in this case, n=1), 2n output (in this case, $2^n=2^1=2$ outputs) and n number of control signals (in this case n=1, hence control line=1). The single input is routed to one of the 2^n outputs, depending on the value of the n control lines. The truth table for the demultilexer at Fig 2 is given in Table 2.

Fig 2

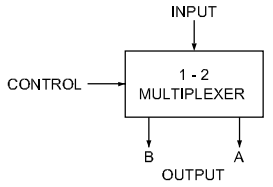


Table 2

INPUT	Control	Output
1	0	Input --> A (Therefore, A=1)
1	1	Input --> B (Therefore, B=1)

8-line Multiplexer

As discussed in earlier paragraphs, a multiplexer is a circuit with 2^n data inputs, one data output and *n* control inputs. The selected data is gated or routed to the output. Fig 3 shows the schematic of an eight-input or eight-line multiplexer.

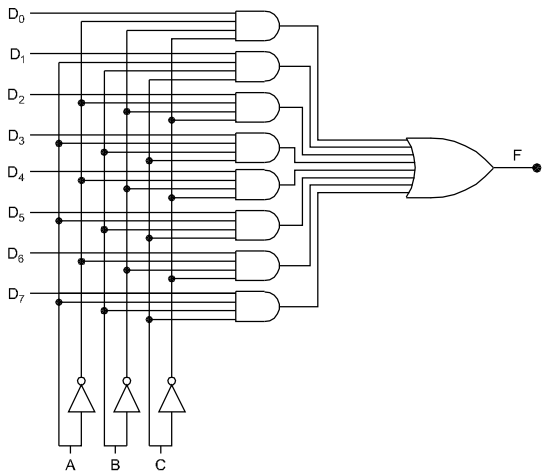
As can be seen in Fig 3, the three control lines A,B and C encode a 3-bit number that specifies which of the eight input lines is gated to the OR gate and then to the output. Immaterial of what value is on the control lines, seven of the AND gate will always output 0, the other one may output 0 or 1 depending on the value of the selected input line. Each gate is enables by a different combination of the control inputs.

Such a eight-line multiplexer is available as a MSI chip. With 8 input lines, 3 control lines, one output, may be an additional compliment output line and power supply and ground lines is implemented as a 16 pin package. One such package is the 74LS151 , 8-line multiplexer IC shown in Fig 4.

Demultiplexer

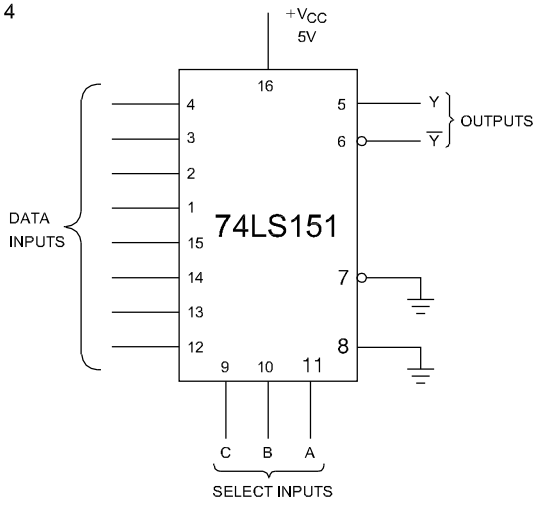
The inverse of a multiplexer is a demultiplexer. A demultiplexer routes its single input signal to one of 2n outputs, depending on the values of the n control lines. For instance, if the binary value on the control signal is all

Fig 3



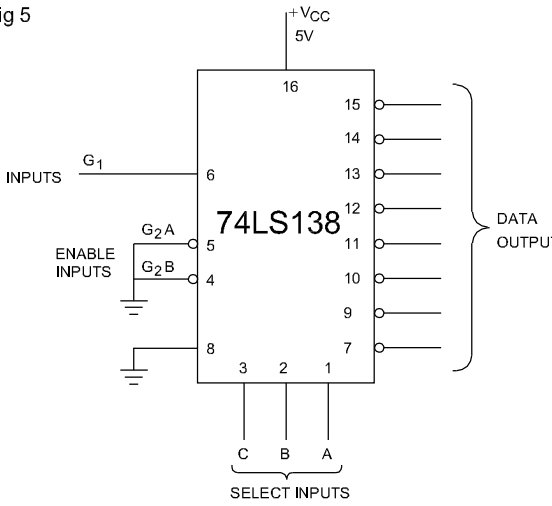
AN EIGHT DIGIT MULTIPLEXER CIRCUIT

Fig 4



8 LINE MULTIPLEXER

Fig 5



8 LINE DEMULTIPLEXER

zeros, the 0th output line is selected and if the binary value on the control lines is *k,* then, the k^{th} output line is selected for routing the input signal. Such demultiplexers are also available in IC package. One such IC is the 1line to 8 line demultiplexer 74LS138 as shown in Fig 5.

Application of Multiplexers and Demultiplexers

There are almost innumerable applications of multiplexers and demultiplexers. Just to list a few are in implementing a multiplexed display, parallel to serial data converter etc.,

The application of multiplexer and demultiplexer can be appreciated in data transmission as shown in Fig 6.

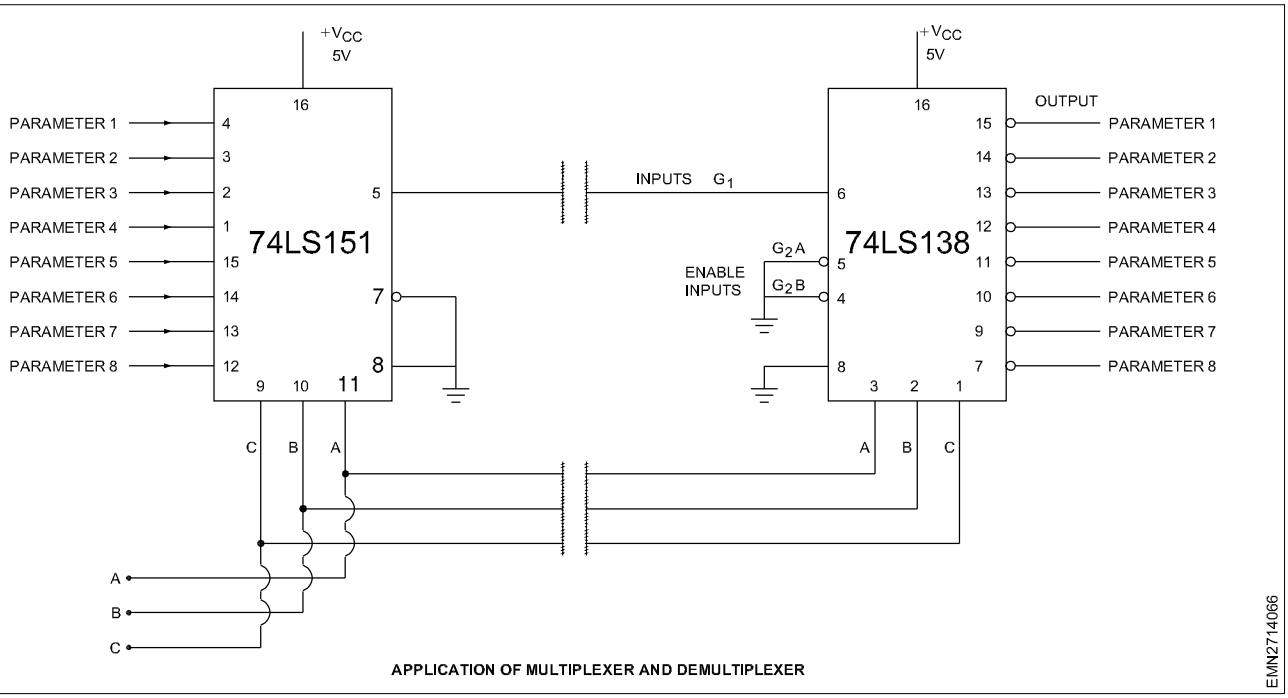
In Fig 6, the eight inputs could be eight signals coming from different transducers measuring eight different type of data (say, temperature, pressure,...) in a industrial environment.

At the other end the output of the demultiplexer may be fed to eight different measuring instruments meant for measuring the individual parameters.

If the control lines of the multiplexer and demultiplexer are simultaneously fed with binary signals sequentially from 000 to 111, then each of the parameter of the input at any given time is communicated over the line to the demultiplxer which in-turn routes it to meter which is meant for displaying the value of the value of the parameter.

Observe from Fig 6, that only one transmission line is used for communicating all the eight parameters at different intervals of time. This is known as Time division multiplexing. Hence, multiplexers and demultiplexers are invariably used in such communication. The three control lines shown in Fig 6 could even be generated at sending and receiving station independently using one of the input line as the synchronizing input.

Fig 6



APPLICATION OF MULTIPLEXER AND DEMULTIPLEXER

Latch circuits and applications

Objectives: At the end of this lesson you shall be able to

- **explain NOR latch and NAND latch using discrete gates**
- **state the concepts of clocked flip flops**
- **discuss the effect of bouncing and debounce circuits**
- **explain D flip-flop and its truth table**
- **explain clocked D flip-flop and its truth table**
- **discuss the difference between edge triggering and level triggering and types of edge trigger**
- **write logic diagram for the given Boolean equations**
- **simplify the logic diagram using Boolean algebra.**

Introduetion

A flip-flop is a digital circuit that has two stable states. It remains in one of these states until triggered into the other.

Flip-flops are used to store binary information. Digital memory circuits that can store bits of data are an essential part of any computer system.

RS flip flops

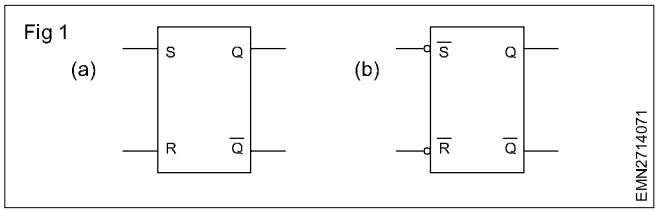
The most basic type of flip flop is the reset/set type, hence it is known as RS flip flop.

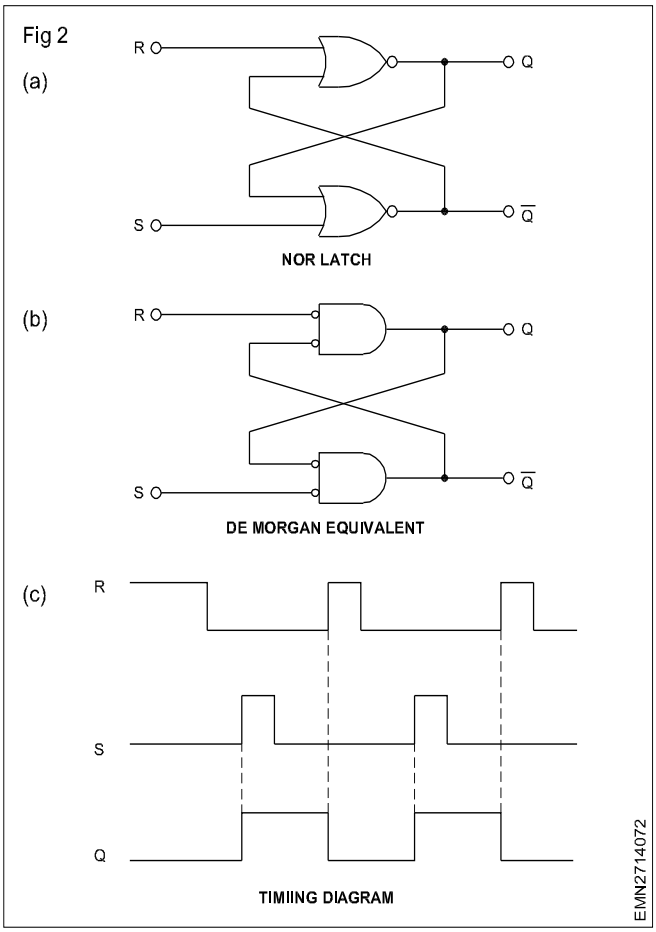
The basic RS flip-flop can be constructed from either two

NOR gates or two NAND gates. The circuit symbols is shown in Fig 1. Fig 1a shows RSF/F with active HIGH inputs. Fig 1b shows RSF/F with active LOW inputs. The NOR gate latch and NAND gate latch both are shown in Fig 2 and Fig 3 respectively.

NOR latch

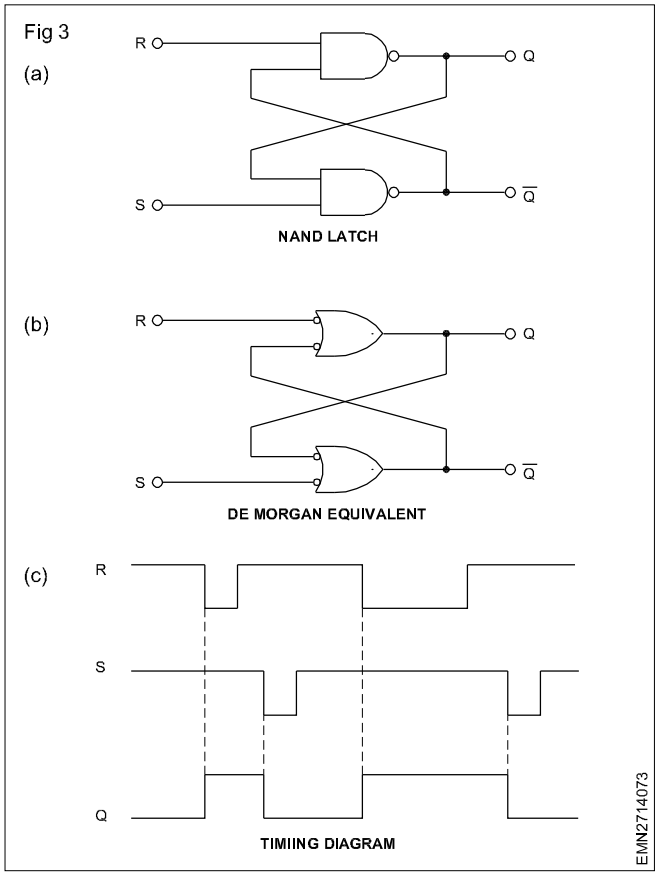
From Fig 2, the two NOR gates are cross-coupled so that out of one NOR gate is connected to other NOR gate input and vice versa.





Truth table for NOR latch

R	S	Q	Comment
0	0	NC	No change
0	1	1	Set
1	0	0	Reset
1	1	*	Race



Truth table for NAND latch

R	S	Q	Comment
0	0	*	Race
0	1	1	Set
1	0	0	Reset
1	1	NC	No change

The NOR latch output are labelled as Q and Q. The outputs will always be the inverse of each other. From the truth table of NOR latch, it can be summarised as follows.

Condition 1

R=0 S=0, this condition produce the inactive state. Output `Q' will remain with no change.

Condition 2

R=0 S=1, this condition cause to go to the Q=1 state where it always remain after R returns high. This is known as setting the latch.

Condition 3

R=1 S=0, this condition cause to go to the Q=0 state where the output remain even after S returns HIGH. This is called resetting the latch.

Condition 4

R=1 S=1, this condition produce a race condition. Therefor

avoid R=1 and S=1 condition while using a NOR latch.

NAND latch

From the NAND gate latch as shown in Fig 3. The two NAND gates are cross-coupled so that output of one NAND is connected to other NAND gate input and vice versa. The NAND latch outputs are labelled as Q and Q. These outputs will always be the inverse of each other.

From the truth table, it can be summarized as follows.

Condition 1

R=0, S=0. This condition produce ambiguous results. It should not be used.

Condition 2

R=0, S=1. This condition cause the output to go the Q=1 state where it will remain after R returns high. This is known as setting the latch.

Condition 3

R=1, S=0. This condition cause the output to go the Q=0 state, where the output will remain even after S returns HIGH. This is called clearing or resetting the latch.

Condition 4

R=1, S=1. This condition is the normal resting state and it has no effect on the output state. The Q and Q outputs will remain in whatever state they were prior to this input condition.

Clocked RS flip-flop

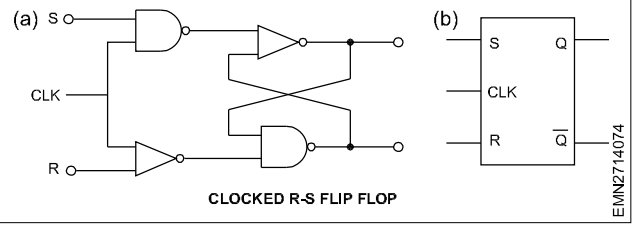
It is possible to strobe or clock the flip-flop in order to store information (set it or reset it) at any time, and then hold the stored information for any desired period of time. This flip-flop is called a clocked RS flip-flop and is shown in Fig 4a and the circuit symbol in 4b.

Truth Table

Clock	R	S	Q
0	0	0	NC
0	0	1	NC
0	1	0	NC
0	1	1	NC
1	0	0	NC
1	0	1	1
1	1	0	0
1	1	1	Illegal

For the flip-flop to operate properly there must be a transition form low to high on the clock input, while clock is high, the information on R and S causes the latch to set or reset. Then when clock transitions back to low, this information is retained in the latch. When this high to low

Fig 4

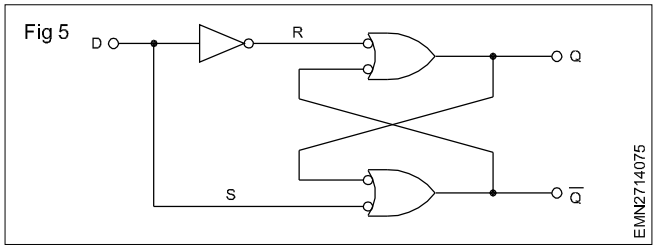


transition occurred both R and S inputs were low(0) and thus there was no change of state.

D-flip-flop

The RS flip-flop has two data inputs, R and S. To store a high bit, you need a high S and to store a low bit, you need a high R. Generation of two signals to drive a flip-flop is a disadvantage in many applications. Further more the RS flip-flop is susceptible to a race condition. We will modify the design to eliminate the possibility of a race condition, to overcome the above disadvantage, R.S flip is slightly modified as shown in Fig 5 to have a single input called D-flip-flop.

Fig 5



Unclocked D latch

D	Q
0	0
1	1

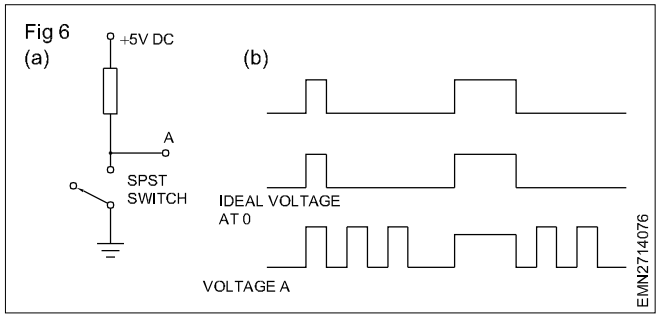
Clock D latch

CLK	D	Q
0	X	NC
1	0	0
1	1	1

Contact bounce circuit

Any mechanical switching device consists of a moving contact arm restrained by some sort of spring system. As a result when the arm is moved form one stable position to the other, the arm bounces as much as hard ball bounces when dropped on a hard surface. The number of bounces that occurs and the period of the bounce differ for each switching device.

Fig 6



In digital system there will be occasions to use mechanical contacts for the purpose of conveying an electrical signal, for example the keyboard of computer. In each case the intent is to apply a high logic level usually [+5V dc] or a low logic level (0 volts DC).

As shown in the Fig 6 above, when the SPST switch is open, the voltage at point 'A' is +5V DC when the switch is closed the voltage at point 'A' is 0 volts.

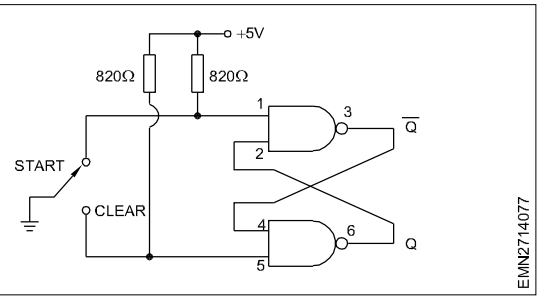
Ideally the voltage waveform at 'A' should appear as shown in the waveform 6b as the switch is moved from open to closed, or vice-versa.

In actuality, the waveform at point 'A' will appear more or less as shown in waveform(C), as a result of contact bounce. Notice carefully that in this particular instance, eventhough actual physical contact bounce occurs each time the switch is opened or closed, contact bounce appears in the voltage level at point 'A' only when the switch is closed.

If the voltage at point 'A' is applied to the input of a T.T.L circuit, the circuit will respond properly when the switch is opened, since no contact bounce occurs. However when the switch is closed, the circuit will respond as if multiple signals were applied, rather than the single-switch closer-intended.

R.S.Latches are often used as switch debouncers. Whenever a switch is thrown from open to the closed position.

Fig 7



Bounce less switch

Floating T.T.L inputs are equivalent to high inputs. With the switch in the start position, Pin 1 is low and pin 5 is high therefore $\overline{Q}$ (pin no.3) is high and Q (pin no.6) is low. When the switch is thrown to the clear position, pin no.1 goes high, as shown in Fig 7. Because of contact bounce, pin 5 goes alternately low and high for a few milliseconds before sets in the low state. The first time pin 5 goes low, the latch sets, Q going high and $\overline{Q}$ going low. Subsequent bounces have no effect on Q and Q because the latch stays set.

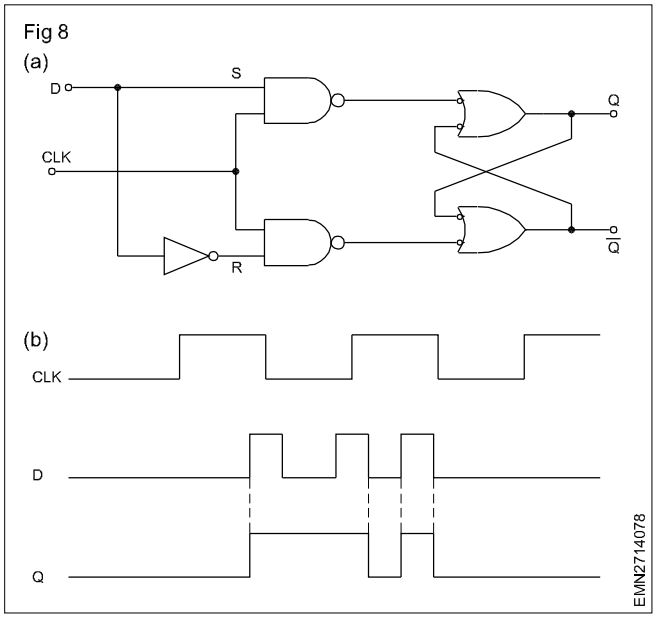
When the switch is thrown back to start, pin 1 bounces low and high for a while. The first time pin 1 goes low, Q goes to low and $\overline{Q}$ going high, later bounces have no effect on Q and $\overline{Q}$.

The Fig 8 shows one way to build a D, latch because of theinverter databit 'D' drives the 'S' input of a NAND latch and the complement of D, drives the 'R' input. Therefore a high 'D' sets the flip-flop, low 'D' resets the flip-flop. Most important thing is no race condition.

Truth table for D-latch

D	Q	Q
1	1	0
0	0	1

Fig 8



Clocked D-flip-flop

The Fig 8a shows the level clocked D type flip-flop. A low clock disables the input gates and prevents the latch from changing states, in other words, while clock is low, the latch is in the inactive state D controls the output, A high D sets the latch, while a low D resets it.

Truth table for level clocked D flip flop

Clk	D	Q
0	X	NC
1	0	0
1	1	1

The truth table summarizes the operation 'X' represents a don't care condition, it stands for either 0 or 1, while clock is low the output can't change, no matter what 'D' is, when clock is high, the output equals the input. Q = D.

Edge triggering versus level clocking

When a circuit is edge triggered, the output can change only on the rising or falling edge of the clock. Edge triggered D - F/F using discrete gate is shown in Fig 9a and the circuit symbol is shown in Fig 9b.

When the circuit is level clocked, the output can change while the clock is high or low.

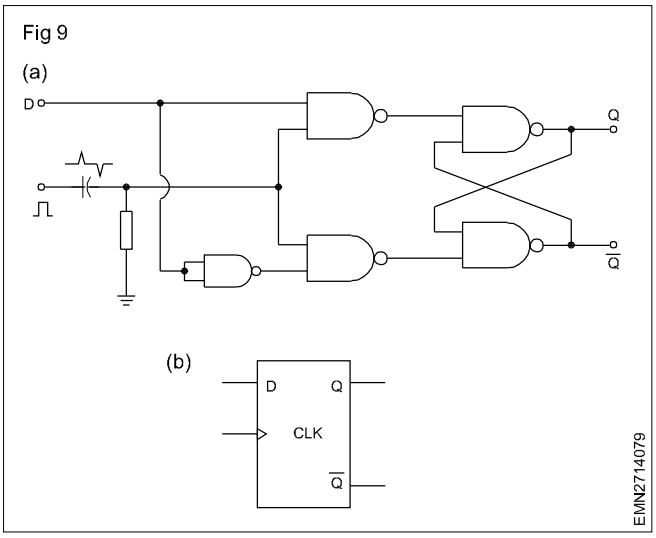
With the edge triggering, the output can change only at one instant during the clock cycle. With level clocking, the output can change during the entire period the level of the clock is maintained.

Edge triggered D-flip-flops

Boolean algebra is convenient and systematic way of expressing and analysing the operation of logic circuits.

Truth table

Edge triggered D-Flip-flop



CLK	D	Q
0	X	NC
1	X	NC
↓	X	NC
↑	0	0
↑	1	1

Variable

A variable is a symbol (usually an Italic uppercase letter) used to represent a logical quantity. Any single variable can have a 1 or 0 value.

Ex: A,B,C,D or X,Y,Z etc

Complements

The complement is the inverse of a variable and is indicated by a bar over the variable.

Ex: The complement of A is $\overline{A}$, the complement of A is read as “A bar”.

Literal

A literal is a variable or the complement of a variable.

Boolean addition

0 + 0 = 0

0 + 1 = 1

1 + 0 = 1

1 + 1 = 0 with carry 1

In Boolean algebra, a sum term is a sum of literals. In logic circuits, a sum term is produced by an OR operation with NAND operation involved.

Ex: A+B, A+$\overline{B}$, $\overline{A}$ + B

A sum term is equal to 1 when one or more of the literals in the term are 1. A sum term is equal to 0 if and only if each of the literal is 0.

Boolean multiplication

Boolean multiplication is equivalent to the AND operation and the basic rules are as follows.

0.0 = 0

1.0 = 0

0.1 = 0

1.1 = 1

In Boolean algebra a product term is the product of literals. In logic circuits a product term is produced by an AND operation with NO OR operations involved.

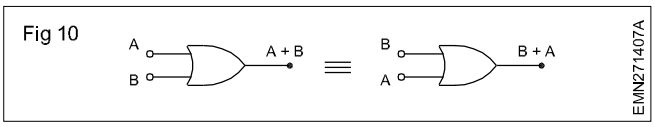
Ex: AB, $\overline{A}$B, A$\overline{B}$, $\overline{A}$ $\overline{B}$

A product term is equal to 1 if and only if each of the literals in the term is one(1). A product term is equal to 0 when one or more of the literal are 0.

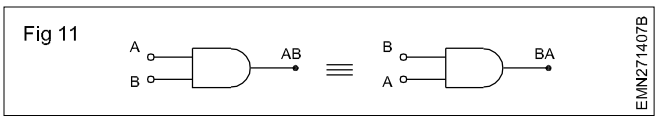
Laws of Boolean algebra

Commutative law

The commutative law for addition for two variables is written algebraically A + B = B + A as shown in Fig 10.



The commutative law for two variable multiplication is AB = BA as shown in Fig 11.

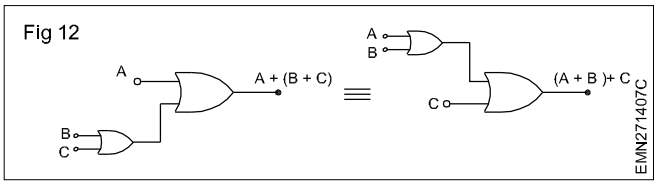


This law states that the order in which the variables are ORed/ANDed make no difference.

Associative law

The associative law of addition is written algebraically as follows for three variables as shown in Fig 12.

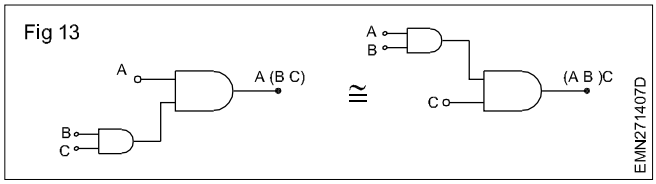
A+(B+C) = (A+B)+C



The associative law of multiplication is written as follows for three variables.

A(BC) = (AB)C

Fig 13



This law states that it makes no difference in what order the variables are grouped when ORing/ANDing more than two variables.

Distributive law

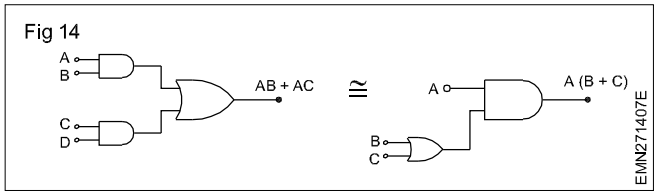
The distributive law is written for three variables as follows.

A(B+C) = AB + AC

This law states that ORing two or more variables and ANDing the result with a single variable is equivalent to ANDing the single variable with each of the two or more variables and then ORing the products as shown in Fig 14. The distributive law also express the process of factoring in which the common variable 'A' is factored out of the product terms.

Ex: AB + AC = A(B+C)

Fig 14



Boolean Algebra Rules

1 $A + 0 = A$

2 $A + 1 = 1$

3 $A + A = A$

4 $A + \overline{A} = 1$

5 $A + AB = A$

6 $A + \overline{A}B = A + B$

7 $A \cdot 0 = 0$

8 $A \cdot 1 = A$

9 $\overline{\overline{A}} = A$

10 $A \cdot A = A$

11 $A \cdot \overline{A} = 0$

12 $(A + B)(A + C) = A + BC$

De-Morgans theorem

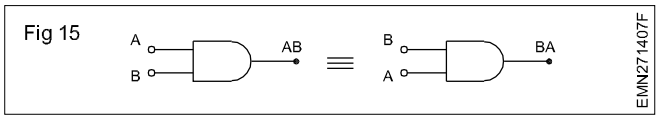
Theorem I

The complement of a product of variables is equal to the sum of the complements of the variables.

$\overline{AB} = \overline{A} + \overline{B}$

The complement of two or more variables ANDed is equivalent to the OR of the complements of the individual variables. The related figure is shown in Fig 15.

Fig 15



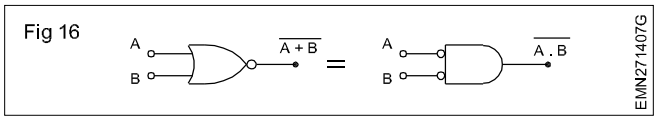
Theorem II

The complement of a sum of variables is equal to the product of the complements of the variables.

$$\overline{A+B} = \overline{A}.\overline{B}$$

The complement of two ore more variables ORed is equivalent to the AND of the complements of the individual variables as shown in Fig 16.

Fig 16



Simplify the equation using De-Morgan's theorem

1 $\overline{(A + B + C)D} = \overline{A + B + C}\ \overline{D}$ $(\overline{AB} = \overline{A} + \overline{B})$

$= \overline{A} . \overline{B} . \overline{C} . \overline{D}$ $(\overline{A + B} = \overline{A} . \overline{B})$

2 $\overline{ABC + DEF} = \overline{ABC} . \overline{DEF}$ $(\overline{A + B} = \overline{A} . \overline{B})$

$= (\overline{A} + \overline{B} + \overline{C}) . (\overline{D} + \overline{E} + \overline{F})$

Simplification of Boolean equations

Prove that $A + \overline{A}B = A + B$

LHS

$= A + \overline{A}B$

$= (A + AB) + \overline{A}B$

$= AA + AB + \overline{A} \cdot B$

$= AA + AB + \overline{A}B + 0$

$= AA + AB + \overline{A}B + A\overline{A}$

$= A(A + B) + \overline{A}(B + A)$

$= (A + \overline{A})(A + B)$

$= 1.(A + B)$

$= A + B$

Prove that (A+B) (A+C) = A + BC

LHS = (A+B) (A+C)

= AA + AB + AC + BC — Since $A = A . A$;

= A + AC + AB + BC — $A = 0$

= A(1+C) + AB + BC — $A + \overline{A} = 1$

= A + AB + BC

= A(1+B) + BC

= A + BC

Simplification of logic circuit using Boolean Equation

AB + A(B+C) + B(B+C)

I step: Simplify the Boolean equations

AB + AB + AC + BB + BC (Distributive law)

AB + AC + B + BC Since BB=B

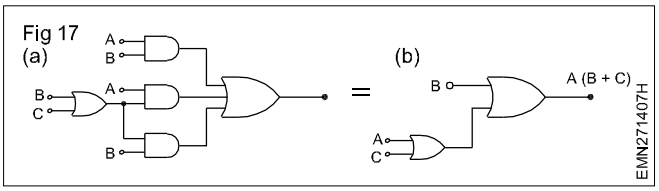
AB + B + AC (A+ A = A, A.A =A)

B(A + 1) + AC (1+A=1)

B + AC

II step write logic diagram for the equations

AB + A(B+C) + B(B+C) = B + AC



Circuit before simplification is shown in Fig 17a. Circuit after simplification is shown in Fig 17b.

The above logic diagram and corresponding Boolean equations show how one can use Boolean Algebra for simplification of logic circuits for the desired logic output.

From the above example it is proved that how the logic circuit gates can be reduced for the same set of output result, using Boolean Algebra. The reduced logic circuit consumes less power and propagation delay time is also reduced, in other words the speed of the circuit increases.

Example

2 Simplify the Boolean expression, and write logic diagram for the given equation and for simplified equation.

$$\overline{A}BC + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}C + ABC$$

$$\overline{A}BC + \overline{B}\,\overline{C}(A + \overline{A}) + AC(\overline{B} + B)$$

$$\overline{A}BC + \overline{B}\,\overline{C} + AC$$

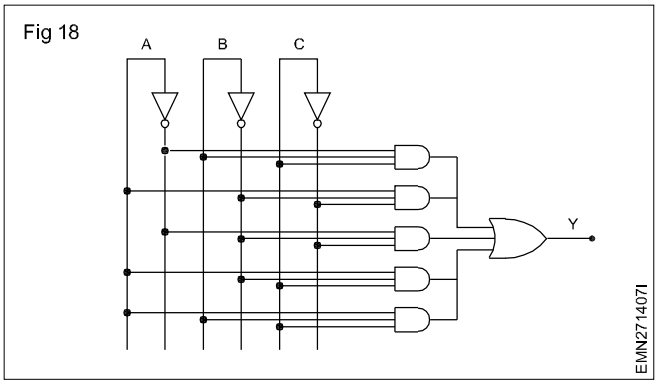
$$\overline{A}BC + AC + \overline{B}\,\overline{C}$$

$$C(A + \overline{A}B) + \overline{B}\,\overline{C}$$ [Since A + $\overline{A}$ B = A + B]

$$C(A + B) + \overline{B}\,\overline{C}$$

$$AC + BC + \overline{B}\,\overline{C}$$

$$\overline{A}BC + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}C + ABC = Y$$



Logic diagram for the given equation is shown in Fig 18.

J K Flip-flop circuits

Objectives: At the end of this lesson you shall be able to

- **explain construction of JK flip-flop using NAND gates**
- **state the function of Preset and clear inputs**
- **define the meaning active low and active high**
- **explain the working function of JK master slave flip-flop**
- **explain frequency division using flip flops.**

Truth table

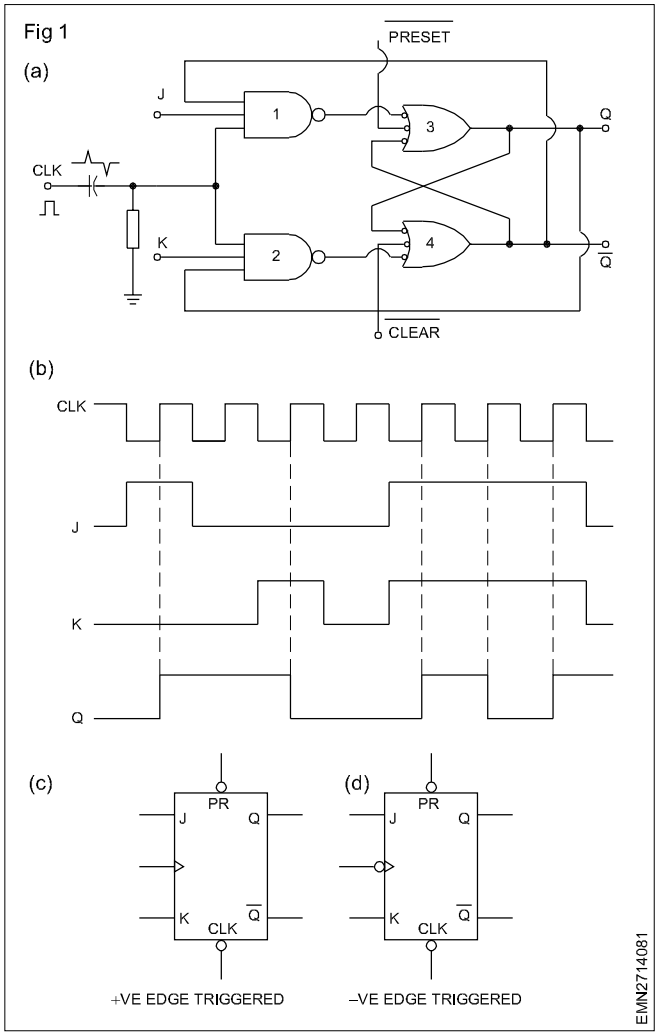
CLK	J	K	Q	
0	x	x	NC	
↓	x	x	NC	
↓	x	x	NC	
x	0	0	NC	
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	Toggle	Toggle

The Fig 1 shows one way to build a JK flip-flop. The variables J and K are called control inputs. An R.C circuit with a short time constant, converts the rectangular clock pulse to narrow spikes. Because of the double inversion through the NAND gates, the circuit is +ve edge triggered. In other words, the input gates are enabled only on the rising edge of the clock as shown in truth table.

Reset

When J is low and K is high the upper output gate is disabled. So there is no way to set the flip flop. The only possibility is reset. When Q is high, the lower gate passes a reset trigger as soon as the +ve clock edge arrives. This

Operation of J-K flip flop



forces Q to become low. Therefore J=0 and k=1 means that a rising clock edge resets the flip-flop.

Set

When J is high and K is low, the lower output gate is disabled. So it is impossible to reset the flip-flop. But flip-flop can be set, when Q is low, Q is high, the gate 1 passes a set trigger on the positive clock edge. This drives Q into the high state. That is J=1 and K=0 means that the next positive clock edge sets the flip flop.

Toggle

When J and K are both high, it is possible to set or reset the flip flop depending on the current state of the output if Q is high, the lower gate passes a reset trigger on the next positive clock edge on the other hand. When Q is low the upper gate passes a set trigger on the next positive clock edge. Either way Q changes to the complement of the last state. Therefore J=1 and K=1 means that the flip-flop will toggle on the next positive clock edge.

To summarize the operation of the JK.flip-flop, the circuit is inactive when the clock is low, high or on its -ve edge. Likewise the circuit is inactive when J and K are both low. Output changes occur only on the rising edge of the clock as indicated by the last three entries of the table. The o/p either resets, sets or toggles.

Racing

Toggling more than once during a clock cycle is called Racing. Assume that the circuit is level clocked. In other words, assume that RC circuit has been removed and run the clock straight, into the gates, with a high J, high K and high clock, the output toggles. New outputs are then fed

Toggling more than once during a clock cycle is called Racing. Assume that the circuit is level clocked. In other words, assume that RC circuit has been removed and run the clock straight, into the gates, with a high J, high K and high clock, the output toggles. New outputs are then fed back to the input gates. After two propagation times (input and output gates), the output toggles again. And once more new outputs return to the input gates. In this way the output can toggle repeatedly as long as the clock is high.

To overcome this racing problem, JK master slave flip-flop has been developed.

Clear

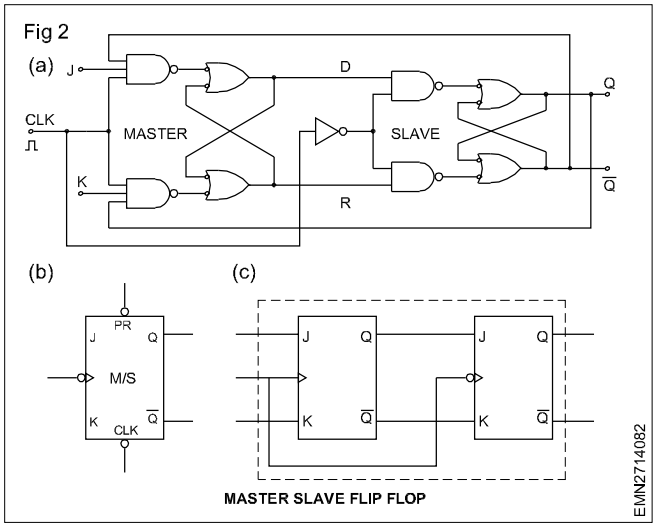
When power is first applied, flip-flops come up in random states. To get some computers started, an operator has to push a master reset button, this sends a clear (reset) signal to all flip-flops, normally clear signal will be active low, (i.e) logic zero should be applied for clear the output. When clear is applied to gate-4 as shown in Fig 1a then the Q will be forced to Logic-0, then automatically $\overline{Q}$ will go to logic-1 condition. This signal, J and K signals have no control over output Q, when clear is set.

Pre-set

Like clear preset is an active low input. This input also independent of CLK, J & K inputs. When preset is made logic-0, the output Q is set to logic one. It is necessary in some digital system to preset the output before the system actually runs.

Master Slave Flip-flop

The Fig 2 shows the JK.Master Slave Flip-flop. It provides another way to avoid racing. A master slave flip-flop is a combination of two clocked flip-flops connected in cas-



cade. Master flip-flop is positive edge triggered, slave flip-flop is negative edge-triggered flip-flop.

– While the clock is high, the master is active and the slave is inactive.

– While the clock is low, the master is inactive and the slave is active.

The J.K master slave flip-flop is used as the main counting device. The popular IC 54LS/74LS76 is a dual JK master slave flip-flop.

Look at the Summarized truth table of J.K master slave flip-flop. A low PR and LOWCLR produces a race condition therefore, PR and CLR are normally kept at a high voltage when inactive. To clear, the flip flop make clear low, to preset the F/F make preset low.

Truth table for positive edge triggered JK flip flop

PR	CLR	CLK	J	K	Q
0	0	X	X	X	Race
0	1	X	X	X	1
1	0	X	X	X	0
1	1	X	0	0	NC
1	1	↑	0	1	0
1	1	↑	1	0	1
1	1	↑	1	1	Toggle

Low J & Low K produces an inactive state regardless of the what the clock is doing. If K goes high by itself, the next clock pulse resets the flip-flop. If J goes high by itself, the next clock pulse sets the flip-flop when J & K are both high, each clock pulse toggle the state of flip flop.

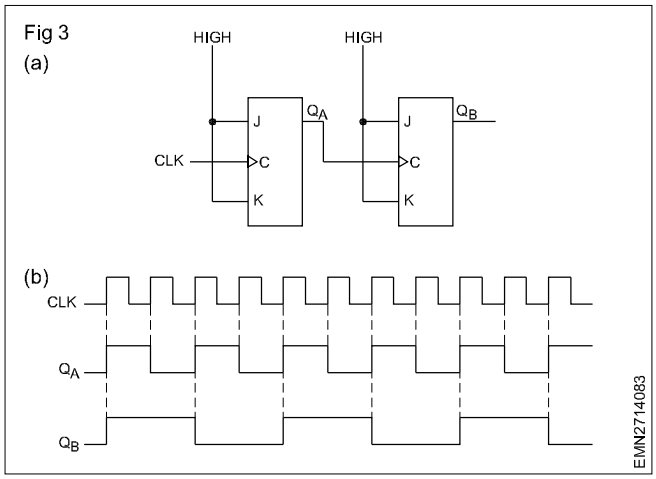
Frequency division using flip flops

Flip-flops are used as frequency dividers of a periodic waveform. When a pulse waveform is applied to the clock input of a J.K flip-flop which is wired for toggle operation, provides square wave output with one half the frequency of the clock input. Thus a single flip-flop can be used for divide by -2 operation as illustrated in Fig 3. The flip-flop changes state on each triggering clock edge. This results in an output which is at half the frequency of the clock waveform.

Further division of clock frequency can be achieved by using the output of one flip-flop as the clock input to a second flip-flop as shown in Fig 3. The frequency of the QA output is divided by 2 by flip-flop B. The QB output is therefore, one fourth the frequency of the original clock input.

By connecting flip-flops in this way, a frequency division of 2^n is achieved, where n is the number of flip-flops. For example, three flip-flops divide the clock frequency by $2^3 = 8$. Four flip-flops divide the clock frequency by $2^4 = 16$; and so on.

Fig 3



Electronic Simulation Software

Objectives : At the end of this lesson you shalll be able to
- **define electronic simulation software**
- **build a circuit with simulation software**
- **virtual instrumentation testing.**

Electronic Simulation Software

Introduction :

- Electronic Circuit simulation is a preparatory software tool designed to create, test and analyse various analog and digital circuits.
- Simulation software allows for modelling of simple to complex circuit operation and is an invaluable analysis tool.
- Electronics simulation software engages the user by integrating them into the learning experience.
- A great collection of most of the electronic components such as passive to active devices are used for circuit drawing, circuit design and analysis.
- There are several free version of electronic circuit simulation softwares available in internet. Also tutorial video guides the user to make use of the application of these simulation softwares.

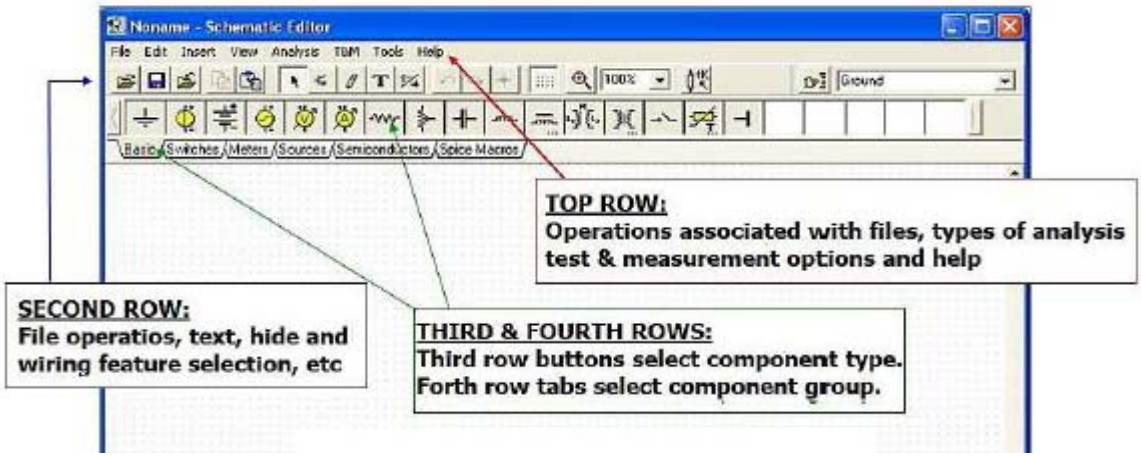
Free and open source circuit simulation software:

- The list of well - structured free circuit simulation software's window based simulator are given below:

– NgSpice
– MultiSim
– QUCS
– MacSpice
– Xspice
– LTSpice
– PECS
– TINA-TI
– Circuit Logix ,etc.

- In the following paragraphs how one of the free version of electronic circuit simulation software can be installed into the computer system after downloaded from the internet and made use of this application software tool for creating, testing virtually using electronic testing & measuring instruments are explained in a step by step manner.
- TINA - TI is a powerful circuit design and simulation tool. IT is ideal for designing,testing,and troubleshooting a broad variety of basic and advanced electronic circuits.
- The tool is ideal for helping designers and engineers to develop and test circuit ideas.
- It is a software program developed by both **Texas Instruments** and **DesignSoft,Inc.**

Fig 1



The schematic editor window

Requirement of PC Configuration:

- The minimum hardware and software requirements for the currently released TINA-TI version are :

i IBM PC - compatible computer running Microsoft windows 98/ME/NT/2000/XP

ii Pentium or equivalent processor

iii 64MB of RAM

iv Hard disk drive with at least 100MB free space

v Mouse

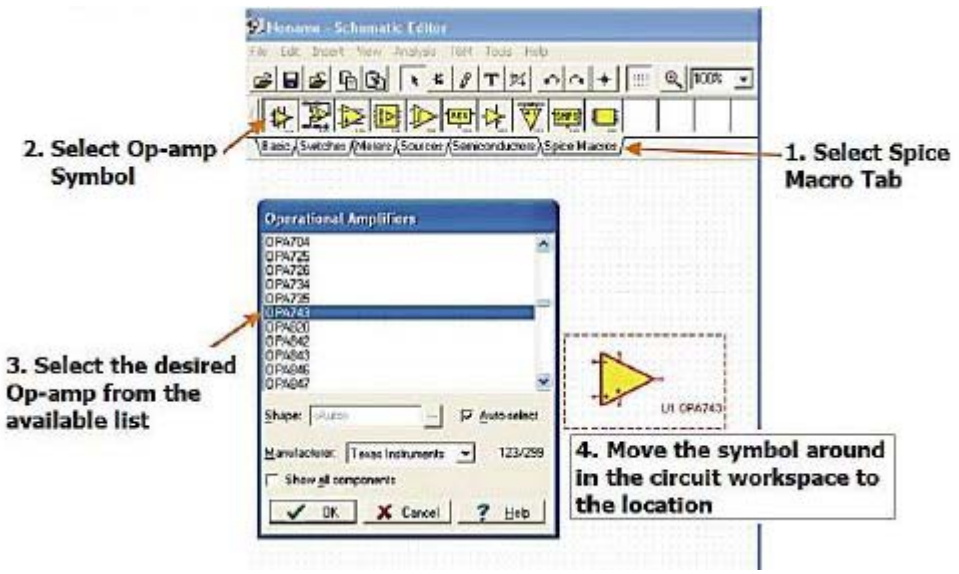
vi VGA adapter card and monitor

- Once the free version of software is downloded to the system, we can select the program through the windows start menu or by clicking the simulation software Icon on the desktop that was created during the installation.
- The first screen appears as shown in figure 1 is the schematic editor layout.
- The empty workspace on the sheet is the design window where the test circuit is to be created.
- Below the schematic Editor title bar is an operational menu row with selections such as file operations, analytical operations, test and measurement equipment selection, etc.
- Located just below the menu row is a row of icons associated with different file and TINA tasks.
- The final row of icons allows selecting a specific component group. These component groups contain basic passive components, semiconductors, and even sophisticated device macro models. These groups are accessed to build the circuit schematic.

Building a circuit using the electronic circuit simulator:

- For building a circuit using simulator,select the required active and passive components and arrange the components and wire the components as per the circuit diagram.
- A search throug a circuit application handbook provides a number of op- amp based designs.A texas instruments 'OPA743 12V CMOS Op- amp is selected for the circuit application.
- This amplifier is well - suited for this design,and provides very good DC and AC performance.
- It operates with supplies of 3.5V to 12V;our example requires 5V (10V).
- The step- by- step procedure is as follows:
- Select the spice macros tab and then the op-amp symbol to access the OPA743 macro model.When the Op-amp model list appears,scroll down and click on the OPA743
- Then click OK. The op-amp symbol appears in teh circuit workspace. With the mouse clicked drag the symbol into position on the workspace as shown in Fig 2.
- It is locked into position on the circuit workspace by clicking the left mouse button.

Fig 2



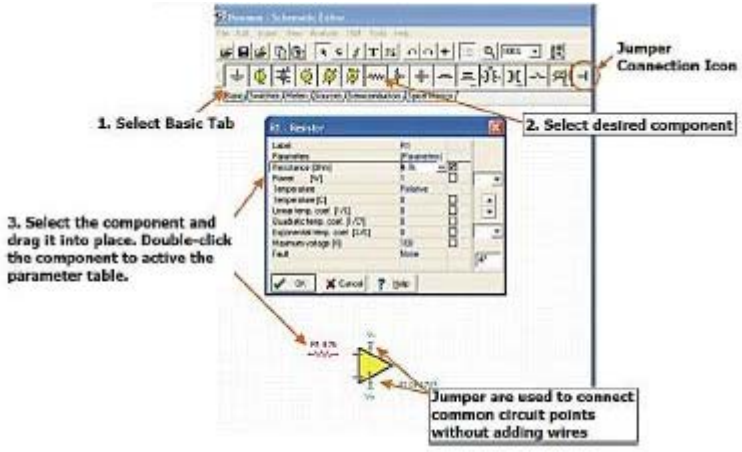
Building a circuit with Op-Amp IC

Adding passive and Active Components:

- Component selection is easily accomplished by clicking on a component group from the lower row of tabs: Basic, switches,Meters,etc.
- These tabs provide a wide variety of passive components, sources,meters, relays, semiconductors,and the previously-mentioned circuit macros.

- Click on the scematic symbol for a particular component and drag it into position in the circuit workspace.A left mouse button click lock it into place.
- In our example ,select a resistor from the basic group, and then position it next to the Op-amp symbol.
- The resistor value and other component characteristics may be altered by selecting the individual parameter boxes and changing the respective values.Select the component parameter box and highlight the value you wish to change.Use the key board,enter a new value by typing over the value that is shown in Fig 3.
- Similar parametric tables are available for passive devices, sources,semiconductors,and other component tyes.

Fig 3

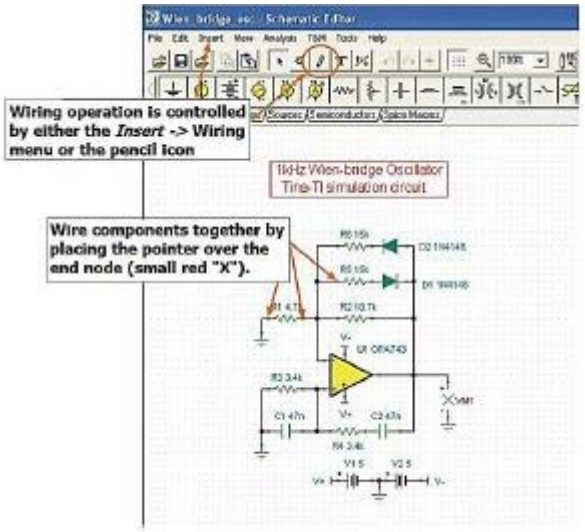


Active and passive component selection

Arranging and wiring components:

- Once all components are selected and properly positioned,they can be wired together.Each component has nodes where circuit connections are needed.
- These nodes with a small red x.(The x looks more like two small lines at the wiring node than the alpha character.)

Fig 4



Wiring components together

- Wiring components to each other is easilydone as shown in Fig 4 by placing the mouse pointer over a node connection and holding the left mouse button down.
- A wire is drawn as the mouse is moved along the circuit space grid.Release the mouse button when the wire reaches the intended end connection point.
- The wiring function also may be accessed from the insert menu,or the icon that looks like a small pencil.

Analysis Capabilities:

- When the circuit schematic entry is complete, the circuit is nearly ready for simulation.The analysis process begins by selecting the Analysis menu.
- A list of different types of analysis-such as AC,DC, Transient, or Noise-appears.
- The first option uder the Analysis menu is an **Error Rules Check (ERC)**.Selecting this feature runs this check on the circuit ; a pop -up window then lists any circuit errors.
- If an error is lited in the window,clicking on that error line highlights the error point in the schematic.The error window also lists types of circuit errors that are found during the analysis.
- Even if the ERC is not selected, the software automatically performs a check at the start of a simulation.
- Upon selecting one type of analysis to perform,

another window appears that displays different setting selections that are associated with that particular analysis.

- Nominal settings are initally provided; these parameters may be set as needed for the desired output.

DC Analysis:

- Follow these steps -(illustrated in Figure - 5) to perform a DC analysis.

– Click on the Analysis menu.

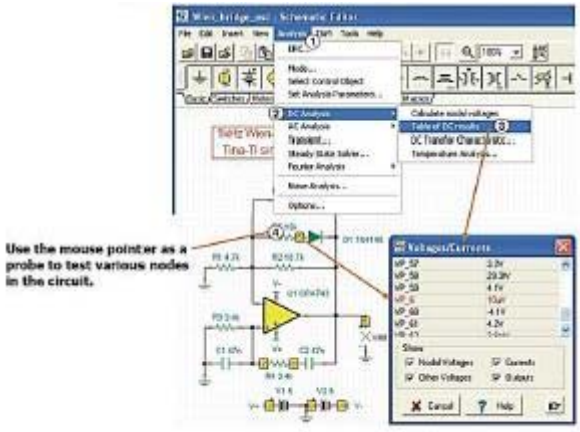
– Select DC Analysis.

– Click on Table of DC Results.The Voltages/Currents table appears.

– Use the mouse pointer as a probe to test the circuit nodes.

- The probed node and measured value are displayed in red in the Voltages/Currents table, as shown in Figure -5.

Fig 5

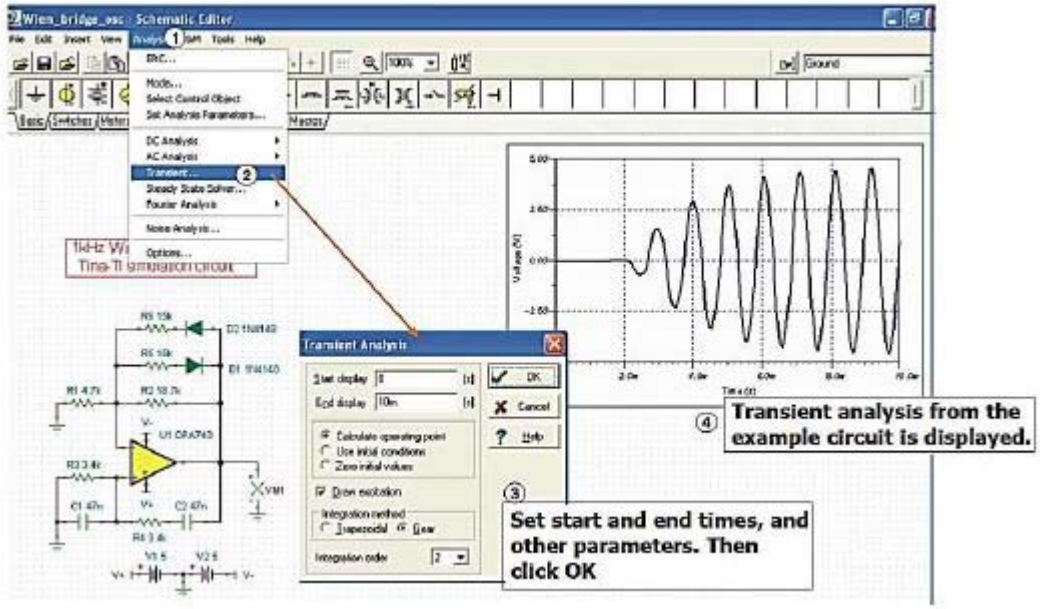


DC Analysis with Voltages/current table

Transient Analysis:

- The transient analysis performed on the example Wien-bridge oscillator circuit is shown in Fig 6.
- It illustrates the Wien-bridge oscillator strat-up and steady-state performance.
- The display in the actual window may be edited with axis labelling, scales, background grid colour, and ect, all set as desired by the individula user.
- Follow these steps (marked in Figure 6) to perform a transient analysis.
- Click on the analysis menu.
- Select Transient.
- The Transient Analysis dialog box appears.Enter start and end times, and other parameters as desired.
- Click OK to run the analysis.

Fig 6

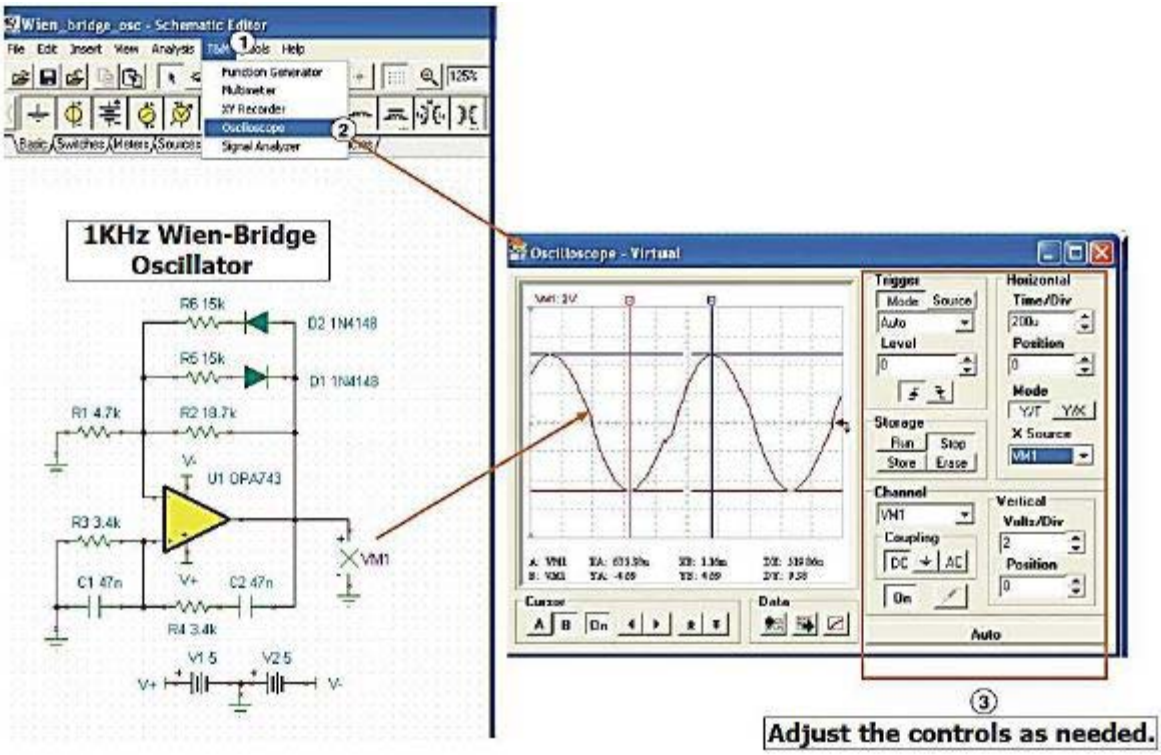


Transient analysis on wein-bridge oscillator

Test and Measurement:

- The Simulation software generates post- simulation result in tables and plots,depending on the type of analysis performed.
- A virtual oscilloscope as shown in Fig 7 is used to observe the steady - state output of the Wien-bridge oscillator circuit. In the same way, a virtual signal analyzer can also be used together with an amplifier circuit so that the harmonic performance of a simulation can be observed.
- To access the virtual oscillosocope, select T&M (step 1 in Figure), and then osilloscope (step 2).Place the cursor at the output of the simulated circuit, and adjust the controls in the virtual oscilloscope dialog box as needed.
- The T&M selection options also include a virtual AC/DC multi-meter, function generator, and an X-Y recorder.
- The function generator may be adjusted in combination with a virtual oscilloscope or analyser.

Fig 7



Virtual instrumentation testing

Thus , the electronic simulation software can be effectively utilized to design,construct,test and analyse various operational parameters using the required electronic components from simple resistor to sophisticated integrated circuits available in the library of resources.After completion of constructing the circuit,required DC power supply, signal generators,digital multimeter even the oscillosope like instruments are simply clicked and connected virtually to make measurements of voltage, current or waveform observation with the ease of clicking the mouse and keyboard.

Counter Circuits

Objectives: At the end of this lesson you shall be able to
- **state basic types of counters**
- **explain the circuit of a ripple counter**
- **explain a down counter using J-K Flip Flops**
- **explain synchronous and asynchronous decade counters**
- **explain module 10 and module 12 counter circuits.**

Counter

A counter is one of the most useful and versatile subsystems in a digital system. A counter driven by a clock can be used to count the number of clock cycles. Since the clock pulses occur at known intervals, the counter can be used as an instrument for measuring time and therefore period or frequency.

Basically there are two types of counters

1 Synchronous counter

2 Asynchronous counter

Synchronous counter

In this counter every flip-flop is triggered by the clock parallely (synchronously) and thus settling time is simply equal to the delay time of a single flip-flop. The increase in speed is usually obtained at the price of increased hardware.

Asynchronous counter

Asynchronous counters are simple and straight forward in operation and construction and usually requires a minimum of hardware, however have a speed limitation. Each flip-flop is triggered by the previous flip-flop, [i.e., clock is applied serially] and thus the counter has a cumulative settling time. Counters such as these are also called as serial counters or ripple counters.

Serial and parallel counters are used in combination to compromise between speed of operation and hardware count. Serial, parallel or combination counters can be designed such that each clock pulse advances the contents of the counter by one, it is then operating in a count-up mode. The opposite is also possible; the counter then operates in the count-down mode. Furthermore, many counters can be either 'cleared' so that every flip-flop contains a zero, or preset such that the contents of the flip-flops represent any desired binary number.

Ripple counter

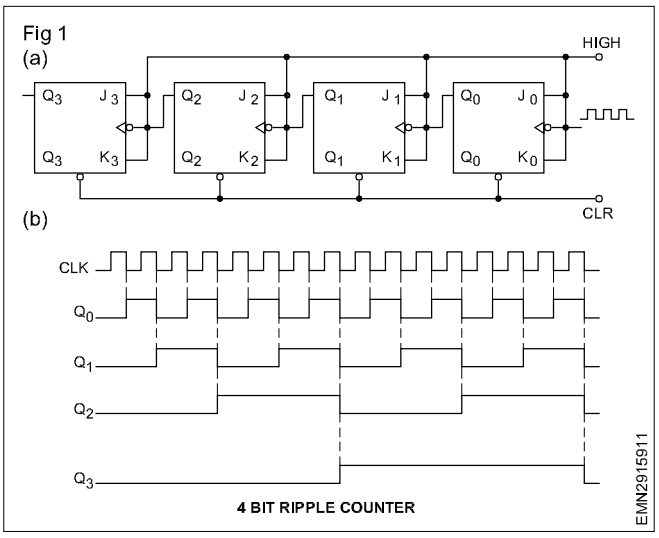
The Fig 1a shows a counter built with JK flip-flops since the J&K inputs are tied to a high voltage, each flip-flop will toggle, when its clock input receives a negative edge.

Visualize the Q outputs as a binary word.

$Q = Q_3Q_2Q_1Q_0$

Q_3 is the most significant bit (MSB) and Q_0 is the least significant bit (LSB). When CLR goes low, all flip-flops

Fig 1



reset, this results in a digital word of Q = 0000.

When clear returns to high, the counter is ready to go, since the LSB flip-flop receives each clock pulse, Q_0 toggles once per negative clock edge, as shown in Fig 1b. The remaining flip-flops toggle less often because they receive their negative edges from the preceding flip-flop outputs(Q). The triggers move through the flip-flops like a ripple in water, that is why this type of counter is called ripple counter.

Counting sequence

When CLR goes from low to high, the Q output of all flip-flops become zeroes.

$Q = Q_3\ Q_2\ Q_1\ Q_0$

Q = 0000

When the first clock pulse triggered the LSB flip-flop, its output Q_0 becomes 1, so the first output word is Q=0001.

When the second clock pulse arrives, Q_0 resets to zero, and this negative falling edge sets next flip-flop output Q_1 to 1 as shown in the timing diagram. Therefore, the next output word is Q=0010.

The third clock pulse advances Q_0 to 1, at this stage Q_0 is having +ve rising edge, so Q_1 output will not change then the counter output is Q=0011.

The fourth clock pulse forces the Q_0 flip-flop to reset and carry. In turn, the Q_1 flip-flop resets and carry, in turn, the Q_1 flip-flop resets and carry.

The resulting output word is Q = 0100.

The fifth clock pulse gives Q = 0101.

The sixth clock pulse gives Q = 0110.

and the seventh pulse gives Q = 0111.

ON the eighth clock pulse Q_0 resets and carrier, Q_1 resets and carrier, Q_2 resets and carry, and Q_3 advances to 1. So the output word becomes Q = 1000.

The ninth clock pulses gives Q = 1001.

The tenth gives Q = 1010 and so on

at the 15th clock pulse Q = 1111

The 16th clock pulse resets all flip-flops. Therefore the counter resets to Q = 0000 and the cycle repeats.

By adding more flip-flops to the left end of the counter circuit, the counter length can be extended. Eight flip-flops gives an 8 bit ripple counter, twelve flip-flops result in a 12 bit ripple counter and so on. The timing diagram is shown in Fig 1b.

Down counter

The counter discussed above is an up counter, counts from 0 to 15 [0000 to 1111]. If a counter counts from 1111 to 0000 then it is called DOWN counter. In a down counter Q output as shown in Fig 2 is connected to the clock input of the next flip-flop. Each flip-flop toggles when its clock input goes from 1 to 0. Flip flop Q_0 toggles with each negative clock transition as before. But flip flop Q_1 will toggle each time Q_0 goes high. Notice that each time Q_0 goes high, Q_0 goes low, and it is this negative transition on Q_0 that triggers Q_1. The timing diagram is in Fig 2b.

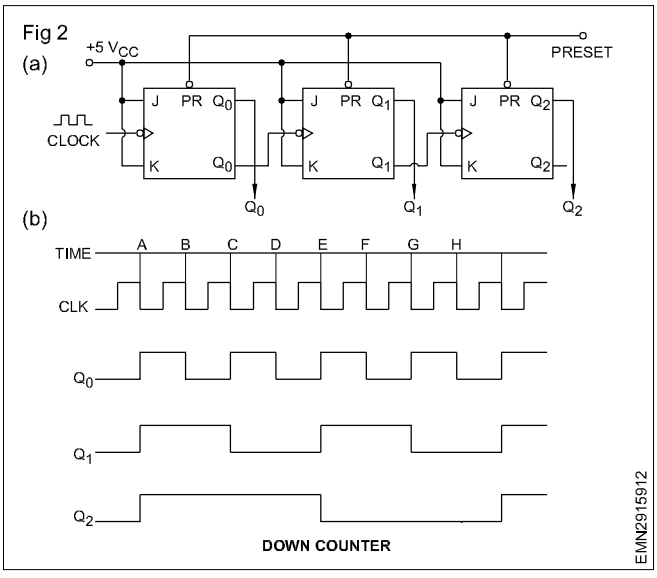
A low preset signal sets all output, producing an output word of Q = 1111.

When pre goes high, the action starts.

The first clock pulse produces a negative toggle in Q_0, nothing else happens. Q = 1110

The second clock pulse produces a positive toggle in Q_0, which produces a negative toggle in Q_1. Q = 1101

On the third clock pulse Q_0 toggles negatively and Q = 1100



On the fourth clock pulse, Q_0 toggles positively Q_1 toggles positively and Q_2 toggles negatively. Q = 1011.

Likewise counting down from 15-0 takes place, when count reaches 0, i.e.Q=0000, on the next clock pulse, all flip-flops toggles positively to get Q=1111 and the cycle repeats.

Modulo -10 Counter

Asynchronous Decade counters

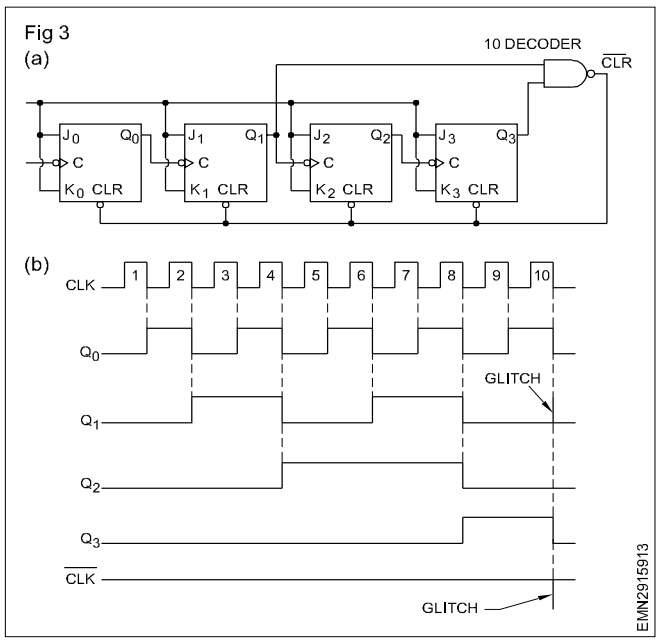
Regular binary counters have a maximum modulus, which means they progress through all of their possible states. The maximum possible number of states (maximum modulus) of a counter is 2^n, where n is the number of flip-flops in the counter.

Counters can also be designed to have a number of states in their sequence that is less than the maximum of 2". The resulting sequence is called a truncated sequence.

One common modulus for counters with truncated sequence is ten. Counters with ten states in their sequence (modulus-10) are called decade counters. A decade counter with a count sequence of zero (0000) through nine (1001) is a BCD decade counter because its ten-state sequence is the BCD code. This type of counter is useful in display applications in which BCD is required for conversion to a decimal readout.

To obtain a truncated sequence, it is necessary to force the counter to recycle before going through all of its normal states. For example, the BCD decade counter must recycle back to the 0000 state after the 1001 state. A decade counter requires four flip-flops (three flip-flops are insufficient because $2^3 = 8$).

We will use a 4-bit asynchronous counter such as the one in Fig 3 and modify its sequence to illustrate the principle of truncated counters. One way to make the counter recycle after the count of nine (1001) is to decode count ten (1010) with a NAND gate and connect the output of the NAND gate to the clear ($\overline{CLR}$) inputs of the flip-flops, as shown in Fig 3.



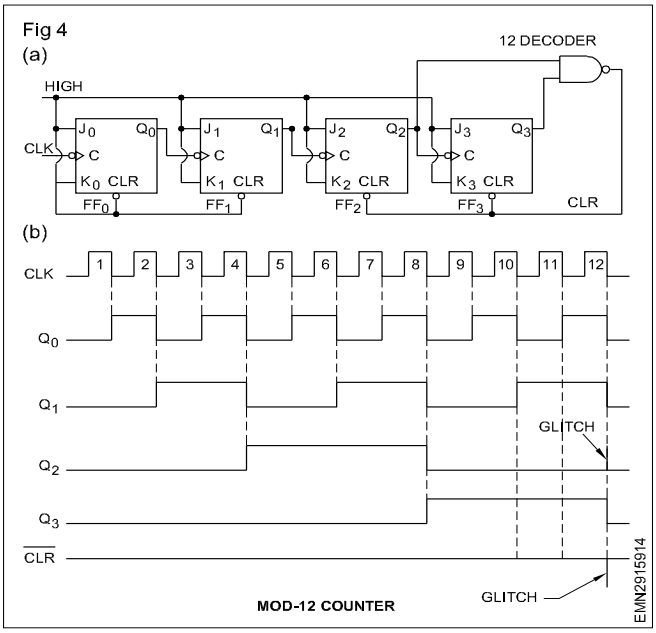
Notice in Fig 3 that only Q_1 and Q_3 are connected to the NAND gate inputs. This arrangement is an example of partial decoding, in which the two unique states (Q_1=1 and Q_3=1) are sufficient to decode the count of ten, because none of the other states (zero through nine) have both Q_1 and Q_3 HIGH at the same time. When the counter goes into count ten (1010), the decoding gate output goes LOW and asynchronously resets all the flip-flops.

The resulting timing diagram is shown in Fig 3. Notice that there is a glitch on the Q_1 waveform. The reason for this glitch is that Q_1 must first go HIGH before the count of ten can be decoded. Not until several nanoseconds after the counter goes to the count of ten does the output of the decoding gate go LOW (both inputs are HIGH) . Thus, the counter is in the 1010 state for a short time before it is reset to 0000, thus producing the glitch on Q_1 and the resulting glitch on the CLR line which resets the counter.

Other truncated sequences can be implemented in a similar way.

Modulo-12 counter

An asynchronous counter can be implemented having a modulus of twelve with a straight binary sequence from 0000 through 1011 as shown in Fig 4a.



Since three flip-flops can produce a maximum of eight states, four flip-flops are required to produce any modulus greater then eight but less than or equal to sixteen.

When the counter gets to its last state, 1011, it must recycle back to 0000 rather than going to its normal next state of 1100, as illustrated in the following sequence chart:

Q_3	Q_2	Q_1	Q_0	
0	0	0	0	
.	.	.	.	
.	.	.	.	Recycles
.	.	.	.	
1	0	1	1	
1	1	0	0	Normal next state

Observe that Q_0 and Q_1 both go to 0 anyway, but Q_2 and Q_3 must be forced to 0 on the twelfth clock pulse. Fig 4a shows the modulus-12 counter. The NAND gate partially decodes count twelve (1100) and resets flip-flop 2 and flip-flop 3. Thus, on the twelfth clock pulse, the counter is forced to recycle from count eleven to count zero, as shown in the timing diagram of Fig 4b. (It is in count twelve for only a few nanoseconds before it is reset by the glitch on CLR)

Up/down Counters

Objectives: At the end of this lesson you shall be able to
- **explain the basic operation of an up/down counter**
- **explain the 74LS190 up/down decade counter.**

UP/DOWN SYNCHRONOUS COUNTERS

An up/down counter is one that is capable of progressing in either direction through a certain sequence. An up/down counter, sometimes called a bidirectional counter, can have any specified sequence of states. A 3-bit binary counter that advances upward through its sequence (0,1,2,3,4,5,6,7) and then can be reversed so that it goes through the sequence in the opposite direction (7,6,5,4,3,2,1,0) is an illustration of up/down sequential operation.

In general, most up/down counters can be reversed at any point in their sequence. For instance, the 3-bit binary counter can be made to go through the following sequence:

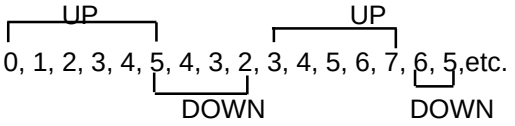
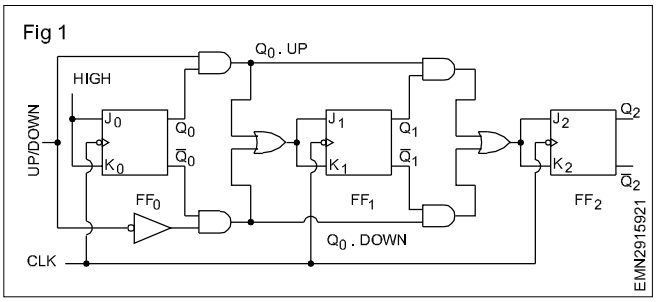


Table 1 shows the complete up/down sequence for a 3-bit binary counter. The arrows indicate the state-to-state movement of the counter for both its UP and its DOWN modes of operation. An examination of Q_0 of Fig 1 for both the up and down sequences shows that FFO toggles on each clock pulse. So the J_0 and K_0 inputs of FFO are

$$J_0 = K_0 = 1$$

Fig 1



For the up sequence, Q_1 changes state on the next clock pulse when Q_0 =1. For the down sequence, Q_1 changes on the next clock pulse when Q_0=0. Thus, the J_1 and K_1 inputs of FFI must equal 1 under the conditions expressed by the following equation:

$$J_1 = K_1 = (Q_0 . UP) + (Q_0 . DOWN)$$

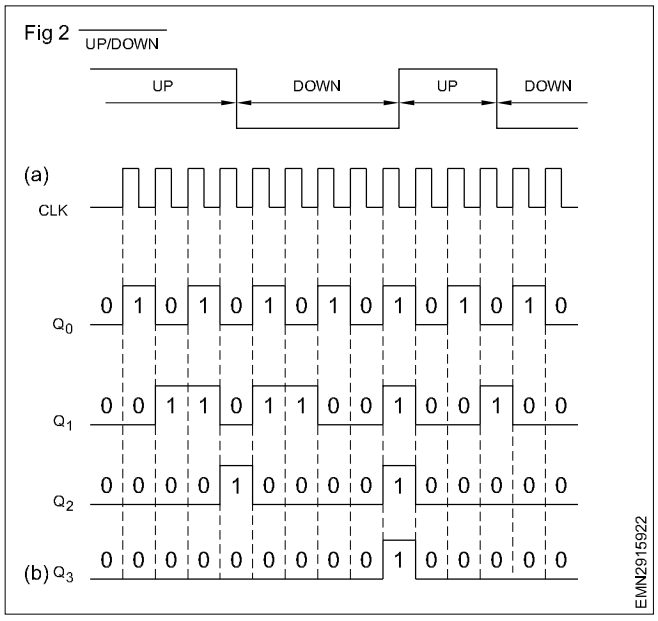
For the up sequence, Q_2 changes state on the next clock pulse when $Q_0 = Q_1 = 1$.For the down sequence, Q_2 changes on the next clock pulse when $Q_0 = Q_1 = 0$. Thus, the J_2 and K_2 inputs of FF2 must equal 1 under the conditions expressed by the following equation:

$$J_2 = K_2 = (Q_0 . Q_1 . UP) + (Q_0 . Q_1 . DOWN)$$

Each of the conditions for the J and K inputs of each flip-flop produces a toggle at the appropriate point in the counter sequence.

A synchronous 4-bit binary up/down counter

Fig 2



A timing diagram and the sequence of a synchronous 4-bit binary up/down counter if the clock and UP/DOWN control inputs have waveforms as shown in Fig 2. The coutner starts in the all 0s state and is positive edge-triggered.

Table 1

Up/Down sequence for a 3-bit binary counter

Clock pulse	UP	Q_2	Q_1	Q_0	Down
0	→	0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	←

The timing diagram showing the Q outputs is shown in Fig 2b. From these waveforms, the counter sequnce is as shown in Table 2.

Table 2

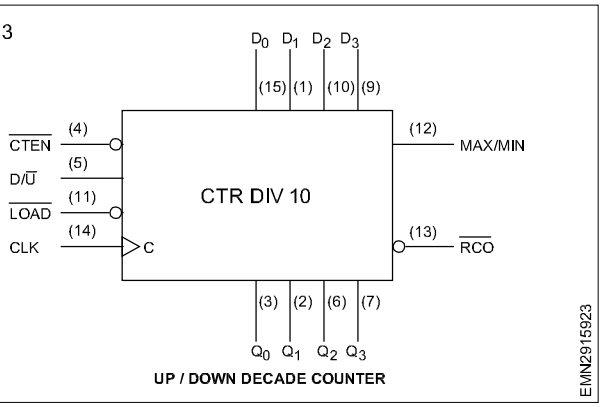
Q_3	Q_2	Q_1	Q_0	Operation
0	0	0	0	
0	0	0	1	
0	0	1	0	UP
0	0	1	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	DOWN
0	0	0	0	
1	1	1	1	
0	0	0	0	
0	0	0	1	UP
0	0	1	0	
0	0	0	1	DOWN
0	0	0	0	

The 74LS190 Up/down decade counter

Fig 3 shows a logic diagram for the 74LS190, a good example of an integrated circuit up/down counter. The direction of the count is determined by the level of the up/down input (D/$\overline{U}$). When this input is HIGH, the counter counts down; when it is LOW, the counter counts up. Also, this device can be preset to any desired BCD digit as determined by the states of the data inputs when the LOAD input is LOW.

The MAX/MIN output produces a HIGH pulse when the terminal count nine (1001) is reached in the UP mode or when the terminal count zero (0000) is reached in the

Fig 3

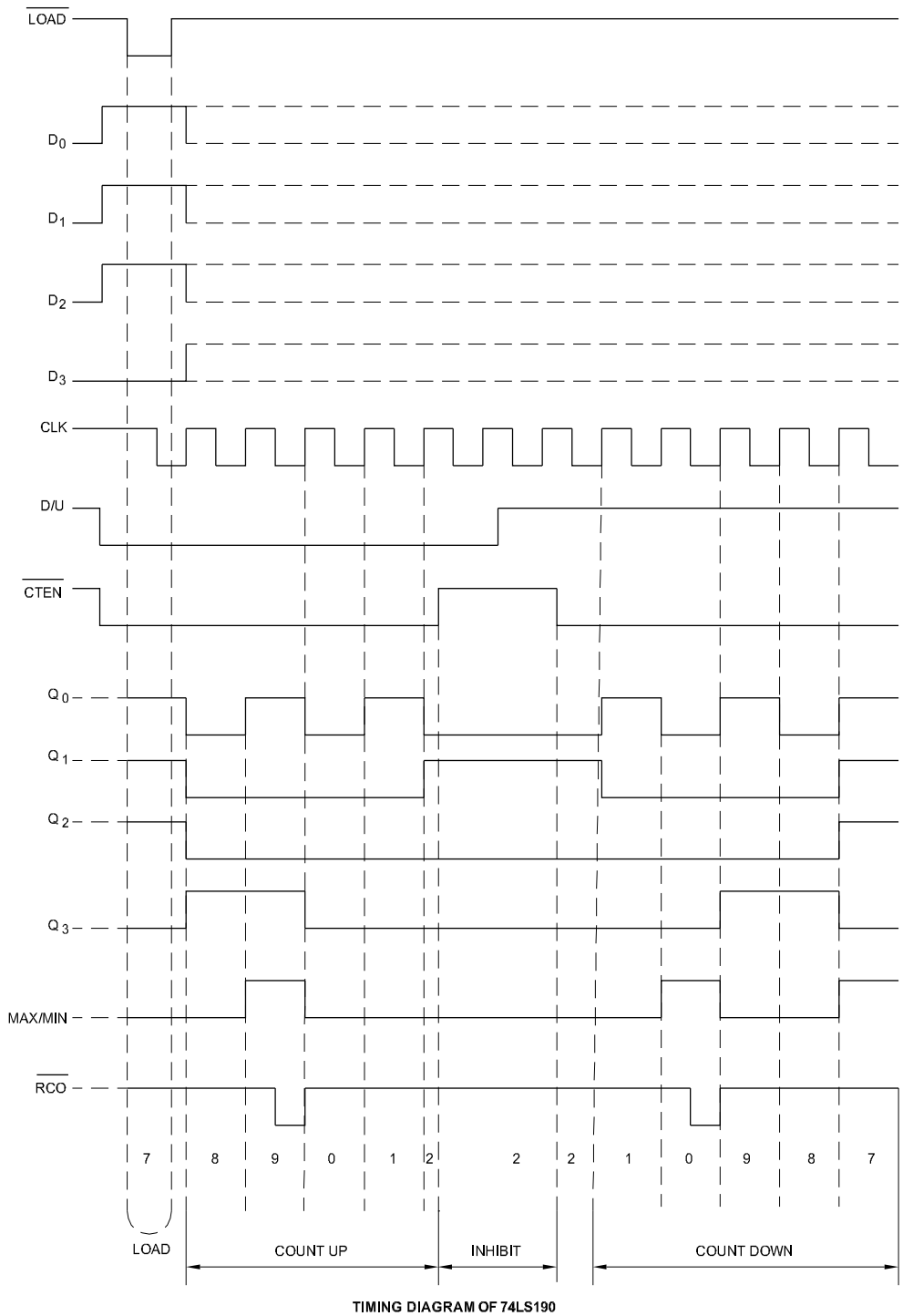


UP / DOWN DECADE COUNTER

DOWN mode. This MAX/MIN output, along with the ripple clock output ($\overline{RCO}$) and the count enable input ($\overline{CTEN}$) is used when cascading counters.

Fig 4 is an example timing diagram showing the 74LS190 counter preset to seven (0111) and then going through a count-up sequence followed by a count-down sequence. The MAX/MIN output is HIGH when the counter is in either the all-0s state (MIN) or the 1001 state (MAX).

Fig 4



TIMING DIAGRAM OF 74LS190

BCD Decoders and Seven Segment Displays

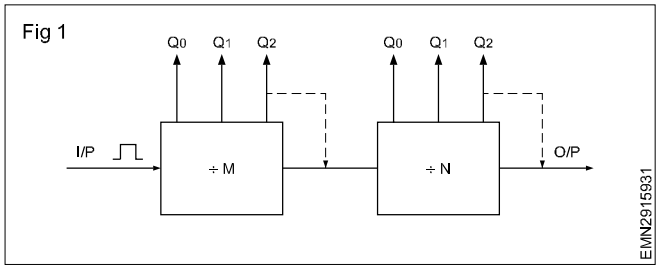
Objectives: At the end of this lesson you shall be able to

- **define cascaded counter**
- **explain the function I.C 7490 decade counter**
- **explain decoder and its application**
- **explain BCD-to-decimal decoder**
- **explain BCD-to-7 segment decoder driver IC 7447**
- **explain 7 segment display and their types and application.**

Cascaded counters

Counters can be connected in cascade to achieve higher modules of operation, cascading means that the last-stage output of one counter drives the input of the next counter.

Fig 1



The Fig 1 shows the two counters [÷M & ÷N] connected in cascade. The final output of the cascaded counter at output occurs once for every M x N clock pulses. The overall modules of the cascaded counters is (MxN); that is they act as ÷[MN] counter. In general the overall modules of cascaded counters is equal to the product of the individual modules.

DM7490 decade counter

DM7490A is a T.T.L MSI decade counter, contains four master slave flip-flops, a careful examination will reveal that flip-flops Q_B, Q_C and Q_D form a MOD-5 counter, and Q_A a divide-by-two counter.

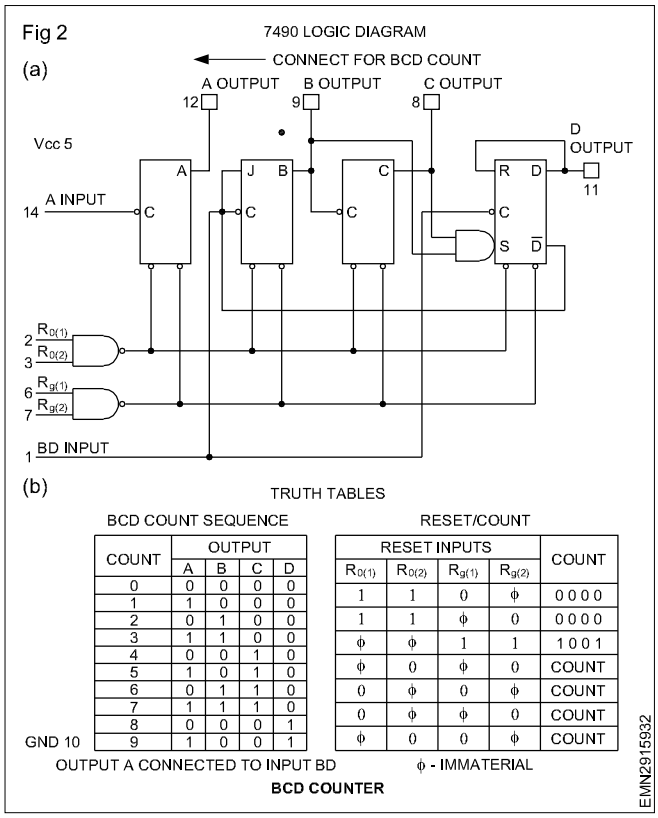
All of these counters have a gated zero reset and the LS-90 also has gated set-to-nine inputs for use in BCD applications. Refer Fig 2 for the detailed internal block diagram.

To use their maximum count length (decade), the output A is connected to the input BD. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divided by ten count can be obtained from the LS90 counters by connecting the Q_D output to the 'A' input and applying the input count to the B input which gives a divided-by-ten square wave at output Q_A.

When reset pins [$R_{o(1)}$ and $R_{o(2)}$] are applied with logic high, an outputs Q_A, Q_B, Q_C and Q_D resets to logic zero are shown in reset/count truth table. To keep counter in count mode one of the reset inputs should be in logic 0(low) state.

The $R_{g(1)}$ and $R_{g(2)}$ inputs are used to preset the counter o/p to BCD nine, to achieve this condition inputs $R_{g(1)}$ and $R_{g(2)}$ should be in logic high state and one of the reset inputs should be in logic 0(low) state. [Ref truth table]

Fig 2



COUNT	OUTPUT A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{g(1)}$	$R_{g(2)}$	COUNT
1	1	0	ϕ	0000
1	1	ϕ	0	0000
ϕ	ϕ	1	1	1001
ϕ	0	ϕ	0	COUNT
0	ϕ	0	ϕ	COUNT
0	ϕ	ϕ	0	COUNT
ϕ	0	0	ϕ	COUNT

During this condition NAND gate o/p will be logic zero and this output is connected to the preset inputs of I[st] and last flip-flop, and sets Q_A and Q_D to logic-1 then the counter reading is 1001.

Decoder

The basic function of a decoder is to detect the presence of a specified combination of bits(code) on its inputs and to indicate the presence of that code by a specified output level. In its general form, a decoder has 'n' input lines to handle 'n' bits and from one to 2^n output lines to indicate the presence of one or more n-bit combinations.

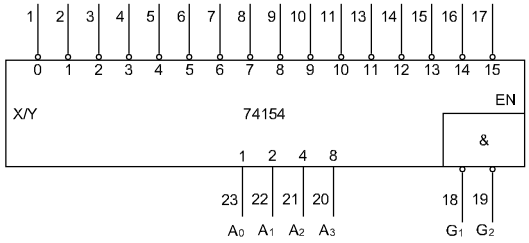
The 4-bit decoder

In order to decode all possible combinations of four bits, sixteen decoding gates are required [2^4 =16]. This type of decoder is commonly called a 4 line to 16 line decoder because there are four inputs and sixteen outputs or a 1-of-16 decoder because for any given code on the inputs, one of the sixteen outputs is activated. The Fig 3 shows the 74154, 4 line to 16 line decoder and the truth table.

BCD-to-Decimal decoder

The BCD-to-decimal decoder converts each BCD code (8421 code) into one of ten possible decimal digit

Fig 3



LOGIC SYMBOL

DECIMAL DIGIT	BINARY INPUTS A_3	A_2	A_1	A_0	DECODING FUNCTION	OUTPUTS 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	$\overline{A}_3\ \overline{A}_2\ \overline{A}_1\ \overline{A}_0$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	$\overline{A}_3\ \overline{A}_2\ \overline{A}_1\ A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	0	1	0	$\overline{A}_3\ \overline{A}_2\ A_1\ \overline{A}_0$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0	0	1	1	$\overline{A}_3\ \overline{A}_2\ A_1\ A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	0	1	0	0	$\overline{A}_3\ A_2\ \overline{A}_1\ \overline{A}_0$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	0	1	0	1	$\overline{A}_3\ A_2\ \overline{A}_1\ A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	0	1	1	0	$\overline{A}_3\ A_2\ A_1\ \overline{A}_0$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	0	1	1	1	$\overline{A}_3\ A_2\ A_1\ A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	0	0	0	$A_3\ \overline{A}_2\ \overline{A}_1\ \overline{A}_0$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1	0	0	1	$A_3\ \overline{A}_2\ \overline{A}_1\ A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1	0	1	0	$A_3\ \overline{A}_2\ A_1\ \overline{A}_0$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1	0	1	1	$A_3\ \overline{A}_2\ A_1\ A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	0	$A_3\ A_2\ \overline{A}_1\ \overline{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
13	1	1	0	1	$A_3\ A_2\ \overline{A}_1\ A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
14	1	1	1	0	$A_3\ A_2\ A_1\ \overline{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	1	1	1	1	$A_3\ A_2\ A_1\ A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

EMN2915933

FUNCTIONS AND TRUTH TABLE FOR A 4 - LINE - TO - 16 - LINE DECODER WITH ACTIVE - LOW OUTPUTS

indications. It is frequently referred to as a 4 line to 10 line decoder or a 1-of-10 decoder. The method of implementation is the same as for the 4 line to-16 line decoder, except that only ten decoding gates are required because the BCD code represents only the ten decimal digits 0 through 9.

7447 BCD-to-7 segment decoder/driver

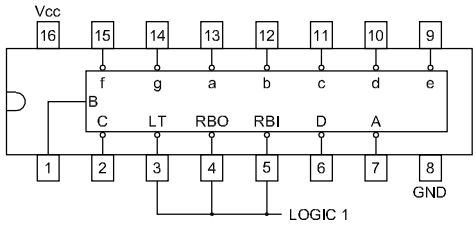
The 7447 [also 74LS47] is an MSI device that decodes a BCD input and drives a 7-segment display. In addition to its decoding and segment drive capability, the 7447 has several additional features as indicated by the LT, RBI and BI/RBO functions in the logic symbol of Fig 4 shown below, as indicated by the bubbles on the logic symbol, all of the outputs (a through g) are active-low as are the LT (lamp test) RBI (ripple blanking input), and BI/RBO [Blanking input (ripple blanking output)] functions. The outputs can drive a common anode 7 segment display directly.

Lamp test

When a low is applied to the LT input and the BI/RBO is high, all of the 7 segments in the display are turned on, lamp test is used to verify that no segments are defective.

Fig 4

(a) PIN LAYOUT



(a) TRUTH TABLE

DECIMAL 0	INPUTS D	C	B	A	OUTPUTS a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

EMN2915934

BINARY TO 7 - SEGMENT DECODER (7447)

Multiplexed Displays

Objectives : At the end of this lesson you shalll be able to

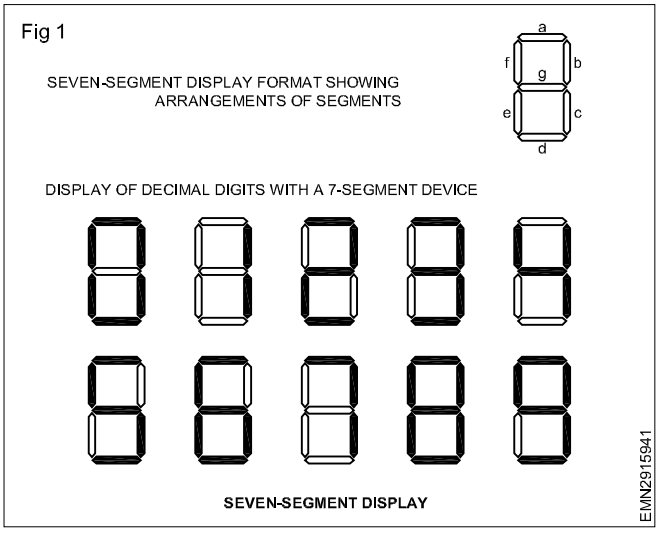
- **explain the constructional details and working of LED type seven segment display**
- **state the need and advantages of multiplexing**
- **explain the process of multiplexing and four digit multiplexed display .**

7-segment display

7 segment displays are used with logic circuits that decode a binary coded decimal (BCD) number and activate the appropriate digits on the display.

The Fig 1 shows a common display format composed of seven elements or segments. Energising certain combinations of these segments can cause each of the ten decimal digits to be displayed. The Fig-b shows the method of digital display for each of the ten digits by using a block segment to represent one that is energized. To produce decimal 'one' on display, segments b and c are energized, to produce 'two' segments a_1,b_1,g_1,e_1 and d_1 are used and so on.

Fig 1



LED display

One common type of 7-segment display consists of light-emitting diodes (LED) arranged as shown in Fig 2. Each segment is an LED that emits light when there is current through it.

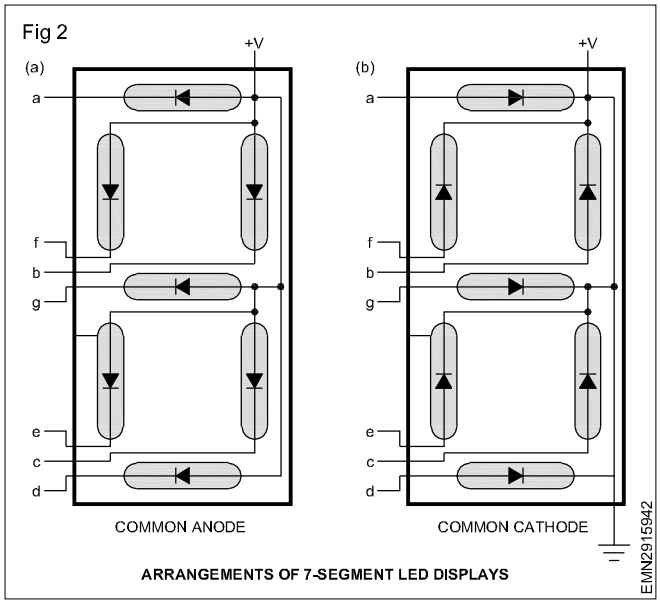
The Fig 2 (a) is common anode arrangement requires the driving circuit to provide a low-level voltage in order to activate a given segment, when a low is applied to a segment input, the LED is turned ON and there is current through it.

In Fig 2(b)the common cathode arrangement requires the driver to provide a high level voltage to activate a segment. When a high is applied to a segment input. The LED is turned ON and there is current through it.

LCD display

Another common type of 7 segment display is the liquid crystal display (LCD), LCDs operate by polarizing light so that a non activated segment reflects incident light and thus appears invisible against its back ground. An activated segment does not reflect incident light and thus appears

Fig 2

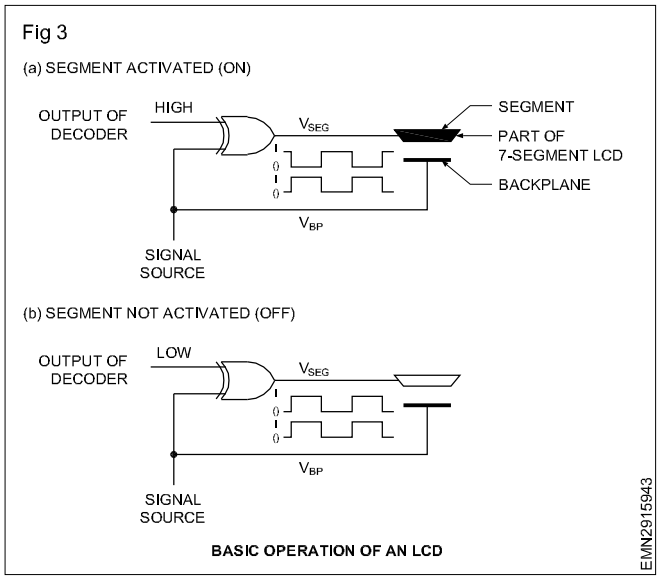


dark. LCDs consume much less power than LEDs but can't be seen in the dark, while LEDs can.

LCDs operate from a low frequency signal voltage (30 Hz to 60 Hz) applied between the segment and a common element called the back plane (bp).

The Fig 3 shows a square wave used as the source signal. Each segment in the display is driven by an Ex-OR gate with one input connected to an output of the seven segment decoder/driver and the other input connected to the signal source. When the decoder/driver output is high the Ex-OR output is a square wave that is 180° out of phase with the source signal. The resulting voltage between the LCD segment and back plane is also a square wave because when V_{seg} = 1, V_{bp}=0, and vice-versa. The voltage difference turns the segmnet ON.

Fig 3

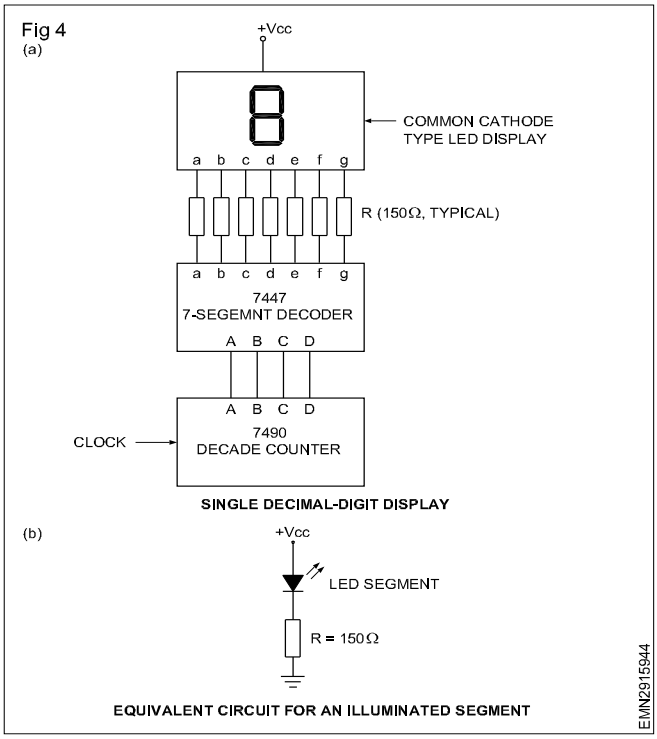


When the decoder/driver output is low(0), the Ex-OR output is a square wave that is in-phase with the source signal, the resulting voltage difference between the segment and the back plane is 0 because $V_{seg} = V_{bp}$. This condition turns the segment off.

For driving LCDs TTL, is not recommended, because its low-level voltage is typically a few tenths of a volt, thus creating a DC component across the LCD, which degrades its performance. Therefore, CMOS is used in LCD applications.

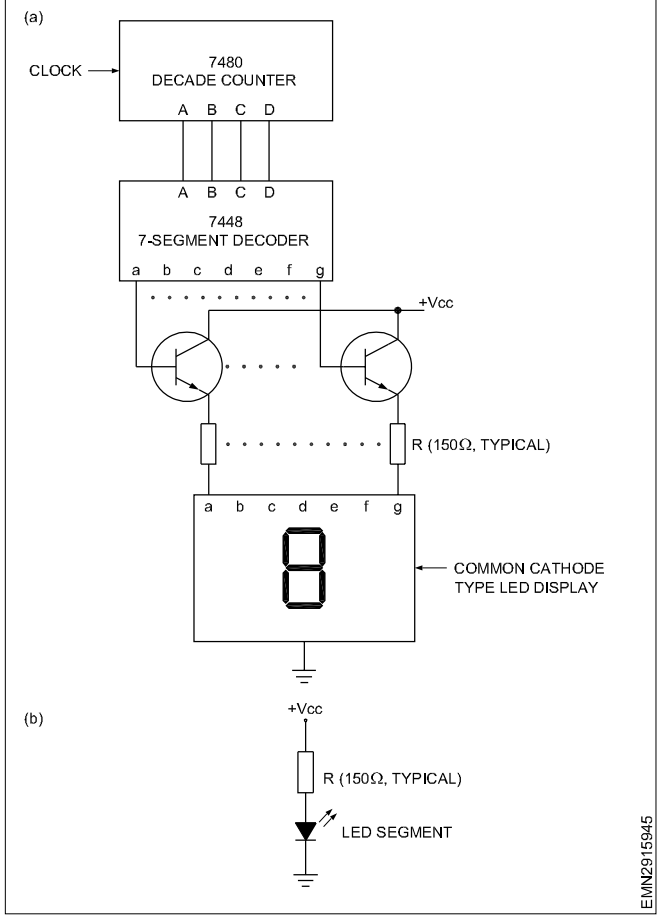
In most of the electronic circuits displays are one common integral block. One hardly finds an electronic circuit interacting with real world, not having one kind or the other display module. The decimal outputs of digital instruments such as digital voltmeters(DVMs), frequency counters, event counters and analog parameter indicators are often displayed using seven segment indicators. Such indicators are constructed by using a fluorescent bar, a liquid crystal bar, or a LED bar for each segment. LED type indicators are convenient because they are directly compatible with TTL circuits, do not require the higher voltages used with fluorescents, and are generally brighter than liquid crystals. On the other hand, LEDs do generally require more power than either of the other two types. Multiplexing is a technique used to reduce display power requirements and the complexity of the display interface circuit. The circuit in Fig 1a is a common anode, LED type,seven segment indicator used to display a single decimal digit. The 7447 BCD-to-seven segment decoder is used to drive the indicator, and the four inputs to the 7447 are the four flip-flop outputs of the 7490 decade counter. The 7447 has active low outputs, so the equivalent circuit of an illuminated segment is in Fig1b. The counter counts upward at the rate of the clock input and the equivalent decimal number will appear on the display.

Fig 4



A similar single decimal digit display using a common cathode type LED indicator is possible with seven segment decoder IC 7448 whose outputs are active high. A buffer amplifier is additionally required as the output current capabilities are too small to drive LEDs directly. This is shown in Fig 5. The npn transistors act as switches to connect dc supply to a segment. When an output of the 7448 is high, a transistor is on, and current is supplied to a LED segment. When the output of 7448 is low, the transistor is off, and segment does not illuminate.

Fig 5



Let us calculate power required for the single digit display of Fig 4. A segment is illuminated when the output of 7447 goes low, causing a 2V drop across it and a current I = (5-2)/150 = 20mA flows through the segment. To display number 8, the indicator require 7x20mA= 140mA. 7447 itself need about 64mA, totalling to 200mA for a single digit display. A digital instrument with four digit decimal display will therefore require 4x200mA = 800mA of current and four such counters and decoders.

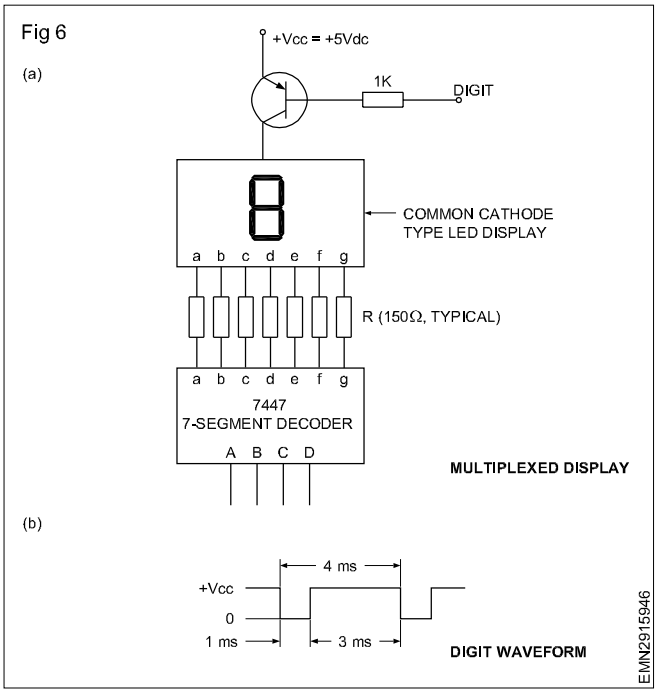
As the no. of digits increase so also the current requirements. These currrent requirements are too much large for small instruments, which can be reduced greatly using a technique known as MULTIPLEXING.Display multiplexing is a process of applying current to each display digit for a very short time interval,but repeatedly. If the pulse repetition rate is sufficiently high, one's eye perceive a steady illumination without any flicker. Indicators illuminated using 50 or 60Hz is reasonably good for flicker free operation.

A single digit display shown in Fig 6a can be multiplexed by applying a waveform as shown in Fig 6b. When DIGIT input is high, the transistor is on and a number is displayed. With the waveform as DIGIT input the segment will display a number for only 1 out of every 4 ms. The display is not illuminated for 3 out of 4 ms but to our eyes it looks as if it is continous.with a pulse rate 4ms, the repetition rate would be 1/4ms=250 Hz. The great advantage here is that this single digit display requires only one fourth the current of a continuously illuminated display. This is the great advantage of multiplexing.

Let us discuss how to multiplex the multiple digit display. Fig 7 shows the multiplexing of four digit display, the BCD inputs to each digit are unchanging. If we apply four no's of similar waveforms as in Fig6b to the four DIGIT inputs, each digit will be illuminated for one fourth of the time and extinguished for three fourths of the time.Look at the timing diagram Fig 7b and see that the digit1 is illuminated druing time t1, digit 2 during time t2 and so on. It is very clear from the waveforms that t1=t2=t3=t4T/4. Suppose t1=1ms then T=4ms and repetition rate(RR)=1/ 0.004=250Hz, this rate is suffiecient for flicker free operation.

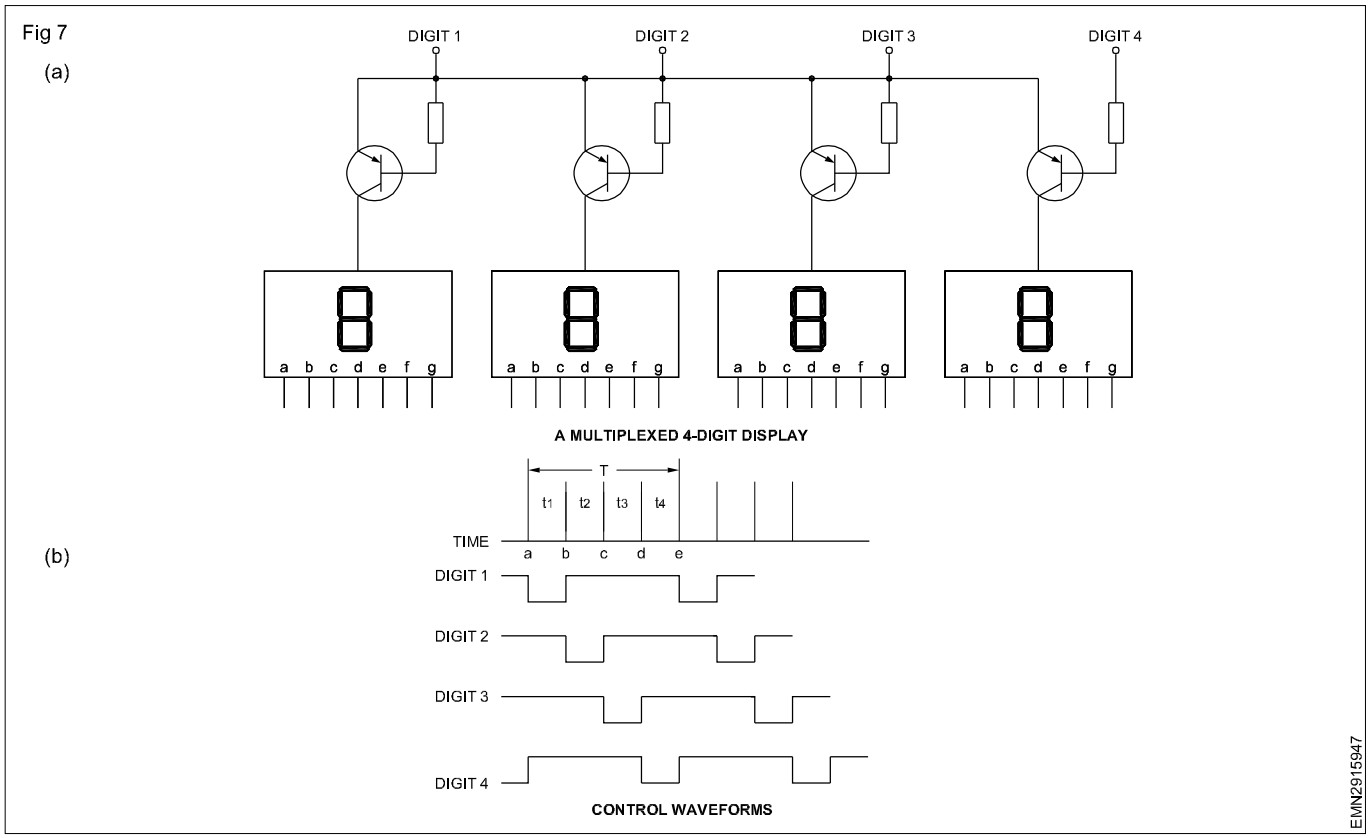
The most important point to be remembered with the multiplexing of displays is that an illuminated digit requires 200mA and since only one digit is illuminated at a time, the current required from the supply is always 200mA. By

Fig 6



multiplexing we are illuminating four indicators but using the current required of only a single indicator. Hence multiplexing displays in this way, the power suplly current is simply the current required of a single display, no matter how many displays are being multiplexed.

Fig 7

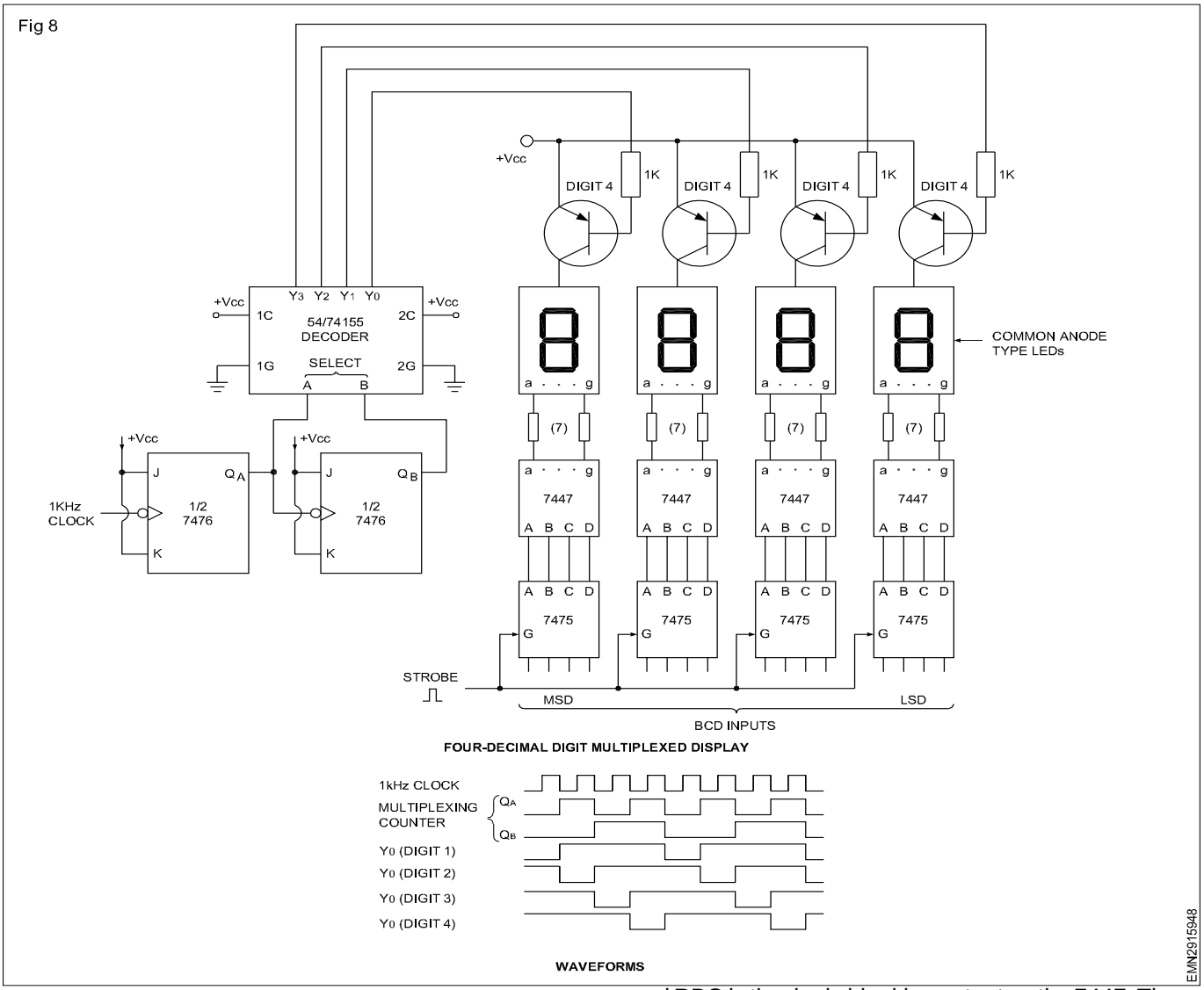


Now the question is how to generate the DIGIT control waveforms show in Fig 7b. A fulfledged four decimal digit multiplexed display is shown in Fig 8. This circuit is capable of displaying decimal numbers from 0000 to 9999. The 54/74155 is a dual 2-line-to-4 line decoder-demultiplexer and it is driven by a two flip flop binary counter called the multiplexing counter. As this counter counts, only one of the 74155 output lines will go low for each counter state. As a result, the DIGIT control waveforms exactly like those in Fig 7b, will be generated. A savings in components as well as power can be realized if four inputs(ABCD) to the seven segment decoder are

multiplexed along with the DIGIT control. The BCD input data is stored in four 7475 D-type latches. Each latch stores a bit and connected to MSD (Most Significant Digit) to LSD(Least Significant Digit). The BCD data can be latched in to the latches by providing a positive going strobe pulse to all the 7475 latches.The BCD input can be applied using thumbwheel switches. The 7476 is a clocked J-K FlipFlop used for generating the address to the SELECT lines. Depending on the address applied at the SELECT input lines, one of the output lines of the decoder 75155 goes low, selecting a specific digt by pulling the base of the transisitor to a logical low. If a transistor connected to any of the digits turned on, that particular digit will be illuminated and displays the BCD number connected to it. Similary the next digit can be selected by changing the address input connected at SELECT input. Now the speed of this whole operation can be changed by applying a different clock frequency to the input of the JK FlipFlops CLOCK input pin.

Commercially LSI chips are available that have all the multiplexing accompllished on a single chip. Examples of this are National Semiconductor's MM74C925, 926, 927 & 928. The only external components needed are the seven segment indicators and current limiting resistors.

Fig 8



Zero suppression

This feature is used for multi-digit displays to blank out unnecessary zeros. For example, in a 6-digit display the number 6.4 may be displayed as 006.400 (i.e) the reading zeros are not blanked out. Blanking the zeros at the front of a number is called leading zero suppression and blanking the zeros at the back of the number is called trailling zero suppression. Keep in mind that only non essential zeros are blanked. With zero suppression, the number 030.080 will be displayed as 30.08.

Zero suppression in the 7447 is accomplished using the RBI and BI/RBO functions. RBI is the ripple blanking input and RBO is the ripple blanking output on the 7447. These are used for zero suppression. BI is the blanking input which shares the same pin with RBO, in the other words the BI/RBO pin can be used as an input or an output. When used in BI mode, all segment outputs are high (non active) with BI is low, which over rides all other inputs. The BI function is not part of the zero suppression capability of the device.

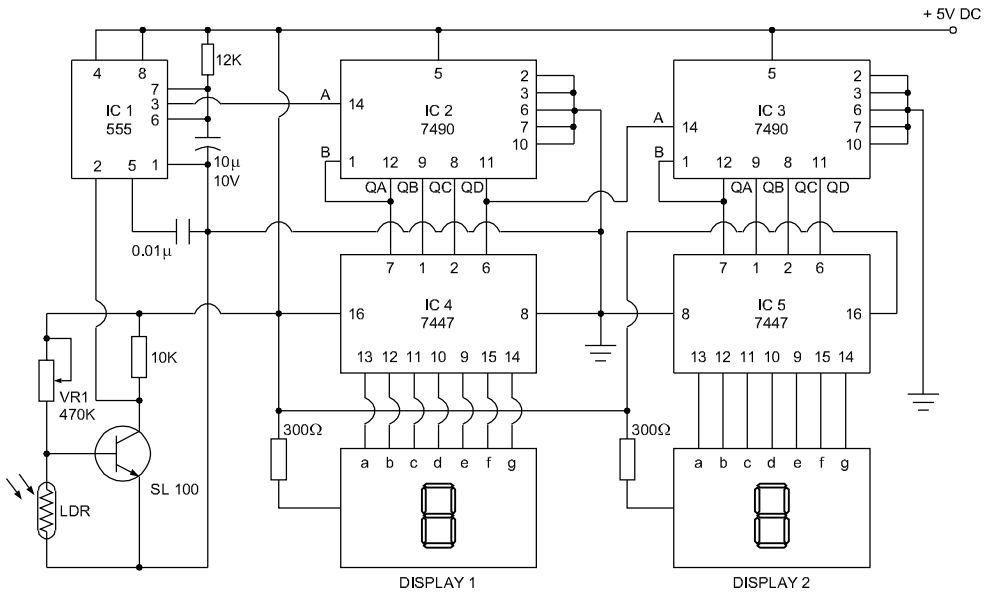
All of the segment outputs of the decoder are non active [HIGH] if a zero code (0000) is on its BCD inputs and if its RBI is low. This causes the display to be blank and produce low RBO. The application zero suppression will be dealt in Digital clock.

Simple interruption counter

Objectives: At the end of this lesson you shall be able to

- **explain how a binary counter can be made to count the no. of objects passing near by.**

Fig 1

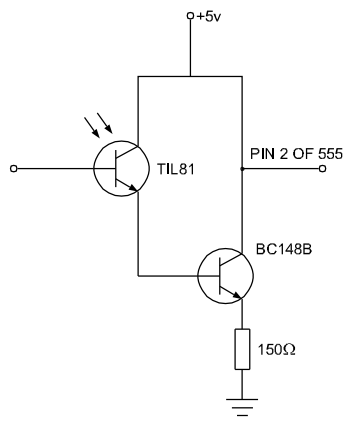


CIRCUIT DIAGRAM OF INTERRUPTION COUNTER

The circuit shown in Fig 1 is a very simple type interruption counter. This circuit provides a novel way to count objects or obstacles or people by focussing a beam of light on LDR which is a IR Photo transistor. Each time the beam is cut by an object, the count increases by one and the same is displayed in a seven segment module connected to it. The operation of the circuit is as follows.

When sufficient amount of light falls on LDR, the resistance of LDR decreases and hence current starts flowing through LDR. The transistor SL100 doesn't get any base drive and hence remain in the off state. However, when the light beam is cut off due to passing of an object or obstacle, LDR resistance increases causing base drive to SL100 and transistor starts conducting. The voltage at collector of the transistor drops. This low voltage at the collector of the transistor SL100 triggers timer IC 555 connected in monostable mode to give a 100ms pulse. This pulse is used as clock input for binary counter IC2(7490). In this circuit IC2,IC3 are configured as mod 10 counter by shorting output Q_A and pin 1 of IC 7490. The output of the decade counter is connected to a decoder cum driver which decodes the binary count to BCD and drives the same to register the number of counts. When count exceeds 9 it goes back to zero, i.e Q_D of IC2 changes from logic 1 to logic 0. IC7490 being negative edge triggered and Q_D of IC2 being connected to input A(pin 14)of IC3 makes it count upward. Thus two 7490 ICs are cascaded to get a count of 99. This number can be increased by cascading 7490 ICs and using corresponding 7447 decoder ICs to decode the circuit. The seven segment data of BCD number to be displayed is connected to a common anode seven segment module.

Fig 2



The 330-ohm at common anode of FND 507 limits current through it and can be varied to alter the intensity to the required level. We can change the sensing part of the circuit so that it can detect interruptions of infrared light using IR phototransistor as shown in Fig 2. In Fig 2 a photo transistor TIL81 is used to sense the light. Depending on the amount of light the phototransistor turns either ON or OFF which inturn drives BC148B pulling the pin 2 of timer IC 555 to logic low. In order to trigger the circuit at the required level of light the circuit is provided with a potentiometer 470K. By changing the potentiometer resistance the circuit can be triggered for different levels of light.

Shift Registers and their Applications

Objectives: At the end of this lesson you shall be able to
- **state the basic functions of a shift register**
- **list and define the different configurations of shift register**
- **explain the function of IC7495 in different configurations.**

Introduction to shift registers

A shift register is a very important digital building block. Registers are often used to momentarily store binary information appearing at the output of an encoding matrix. A register might be used to accept input data from an alphanumeric keyboard and then present this data at the input of a microprocessor chip. Similarly, shift registers are often used to momentarily store binary data at the output of a decoder. For instance, a register could be used to accept output data from a microprocessor chip and then present this data to the circuitry used to drive the display on a CRT screen. Thus registers form a very important link between the main digital system and the input-output channels.

A binary register also forms the basis for some very important arithmetic operations. For example, the operations of complementation, multiplication, and division are frequently implemented by means of a register. A shift register can also be connected to form a number of different types of counters. These counters offer some very distinct advantages.

Types of registers

A register is simply a group of flip-flops that can be used to store a binary number. There must be one flip-flop for each bit in the binary number. For instance, a register used to store an 8-bit binary number must have eight flip-flops. Naturally the flip-flops must be connected such that the binary number can be entered (shifted) into the register and possibly shifted out. A group of flip-flops connected to provide either or both of these functions is called a shift register.

The bits in a binary number (let's call them the data) can be moved form one place to another in either of two ways. The first method involves shifting the data 1 bit at a time in a serial fashion, beginning with either the MSB or the LSB. This technique is referred to as serial shifting. The second method involves shifting all the data bits simultaneously and is referred to as parallel shifting.

There are two ways to shift data into a register (serial or parallel) and similarly two ways to shift the data out of the register. This leads to the construction of four basic register types as shown in Fig 1 -serial in - serial out, serial in - parallel out, parallel in - serial out, and parallel in - parallel out. All of these configurations are commercially available as TTL MSI/LSI circuits. For instance:

Serial in - serial out - 54/74L91, 8 bits

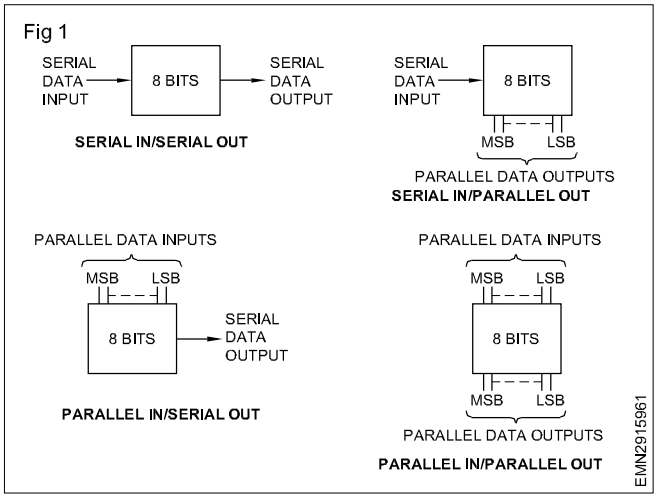
Serial in - parallel out - 54/74164, 8 bits

Parallel in - serial out - 54/75165, 8 bits

Parallel in - parallel out - 54/74194, 4 bits

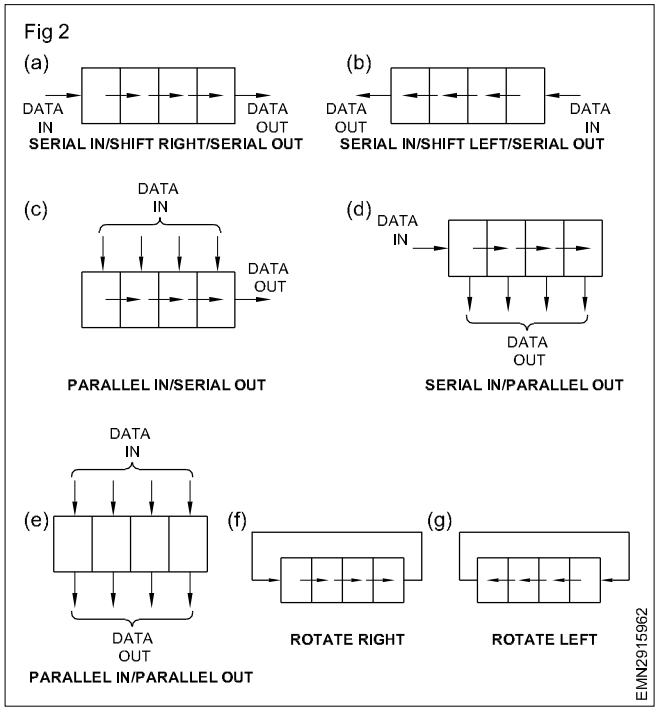
Parallel in - parallel out - 54/74198, 8 bits

Fig 1



The shifting capability of a register permits the movement of data from stage to stage within the register or into or out of the register upon application of clock pulses. Fig 2a to 2g illustrate the types of data movement in shift registers. The block represents any arbitrary 4-bit register and the arrow indicate the direction of data movement.

Fig 2



Serial in - serial out operation

The flip-flops used to construct registers ar usually either JK or D types. So let's begin by summarizing the operation of JK flip-flop.

For a JK flip-flop, the data bit to be shifted into the flip-flop must be present at the J and K inputs when the clock transitions (low or high). Since the data bit is either a 1 or

a 0, there are two cases:

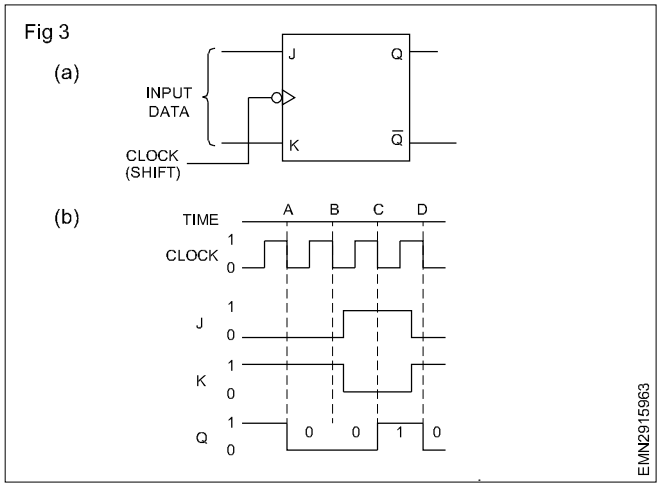
– To shift a 0 into the flip-flop, J=0 and K=1.

– To shift a 1 into the flip-flop, J=1 and K=0.

The important point to note is that the J and K inputs must be controlled to provide the correct input data. The J and K logic levels may be changing while the clock is high (or low), but they must be steady from just before until just after the clock transition (remember, setup time and hold time). For our discussion we shall use JK master-slave flip-flops having clock inputs that are sensitive to negative clock transitions. Incidentally, this negative transition of the clock is frequently referred to as a shift pulse.

The waveforms in Fig 3 illustrate these ideas. At time A, Q is reset low (a 0 is shifted into the flip-flop). At time B, Q does not change since the flip-flop had a 0 in it and another 0 is shifted in. At time C, the flip-flop is set (a 1 is shifted into it). At time D, another 0 is shifted into the flip-flop. In essence, we have shifted 4 data bits into this flip-flop in a time sequence: a 0 at time A, another 0 at time B, a 1 at time C, and a 0 at time D.

Now, consider adding three more flip-flops connected as shown in Fig 4. Let's begin with all the flip-flops reset and



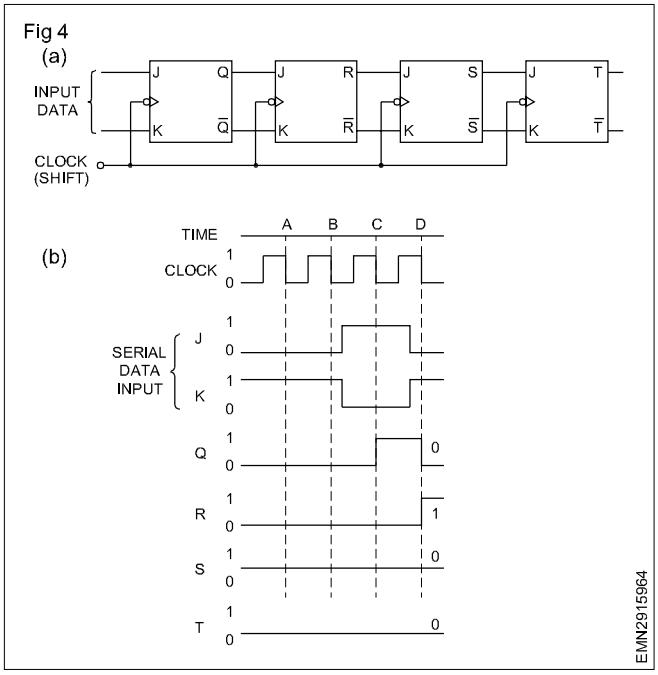
then apply the exact same input signals to flip-flop Q as we did in Fig 3. Here's what happens:

At time A: All the flip-flops are reset, so all J inputs are low and all K inputs are high. Then T is reset (the 0 in S is shifted into T). Similarly, the 0 in R is shifted S, the 0 in Q is shifted into R, and the 0 at the data input is shifted into Q. The flip-flop outputs just after time A are QRST = 0000.

At time B: The flip-flops all contain 0s. Thus the 0 in S is shifted into T, the 0 in R shifts into S, the 0 in Q shifts into R, and the 0 at the data input shifted into Q. The flip-flop outputs are QRST = 0000.

At time C: The flip-flops still all contain 0s. The 0 in S shifts into T, the 0 in R shifts into S, and the 0 in Q shifts into R, but a 1 at the data input now shifts into Q. The flip-flop outputs are QRST = 1000.

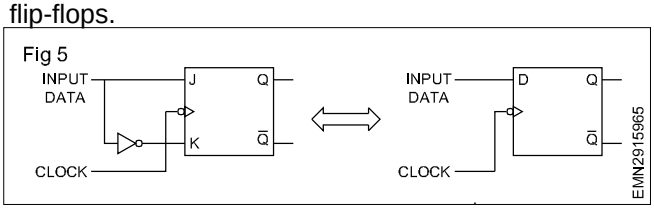
At time D: The 0 in S shifts into T, the 0 in R shifts into S, the 1 in Q shifts into R (the J input to R is high and the K input is low), and the 0 at the data input shifts into Q. The flip-flop outputs are QRST = 0100.



To summarize, we have shifted 4 data bits in a serial fashion into four flip-flops. These 4 data bits could represent a 4-bit binary number 0100, assuming that we began shifting with the LSB first. Notice that the LSB is in T and the MSB is in Q. These four flip-flops could be defined as a 4-bit shift register; thus this is the technique used to construct a serial-input shift register.

The serial data input for the register shwon in Fig 4 requires two input signals J and K. But look carefully at the waveforms. Clearly, K = J, or J=K. In other words, one signal is always the complement of the other. If we were to connect an inverter between J and K on flip-flop Q with the input at J, therefore, we would need to have only one data input signal - the one required for J. But this is precisely a D-type flip-flop as shown in Fig 5. Remember the rules for a type D flip-flop; on the negative clock transition, the data present at the D input (either a 1 or a 0) will shift into the flip-flop.

Thus the 4-bit serial input shift register shown in Fig 5 can be constructed by replacing the JK flip-flops wth type D flip-flops.



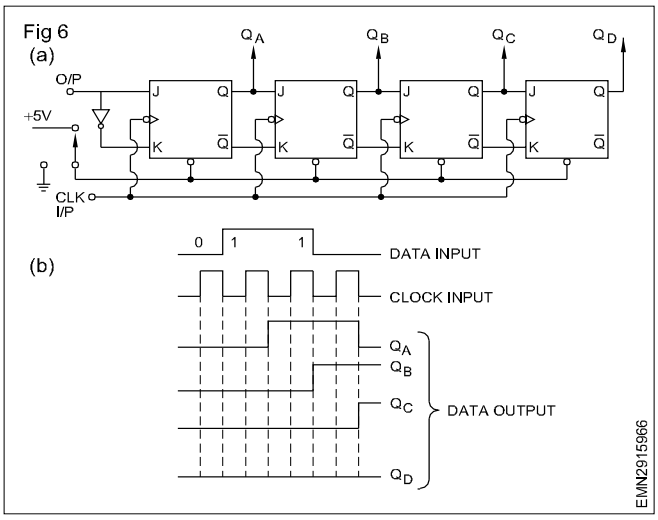
Serial In Parallel Out (SIPO)

Data is entered serially into this type of register, and data bits are taken out of the register parallel from the output of each stage. Once the data bits are stored, each bit appears on its respective output line, and all bits are available simultaneously, rather than on a bit-by-bit basis as with the serial output.

The Fig 6a shows the SIPO shift register using J.K.flip-flops. All the inputs are tied to the compliment of J-inputs. The clock, preset and clear inputs are -ve edge triggered.

Initially all the flip-flops are cleared to logic-0 state by applying logic-0 pulse to the clear inputs.

The sequence of shifting logic information is shown in Fig 6b which gives waveform diagrams of data input, data output and clock input.



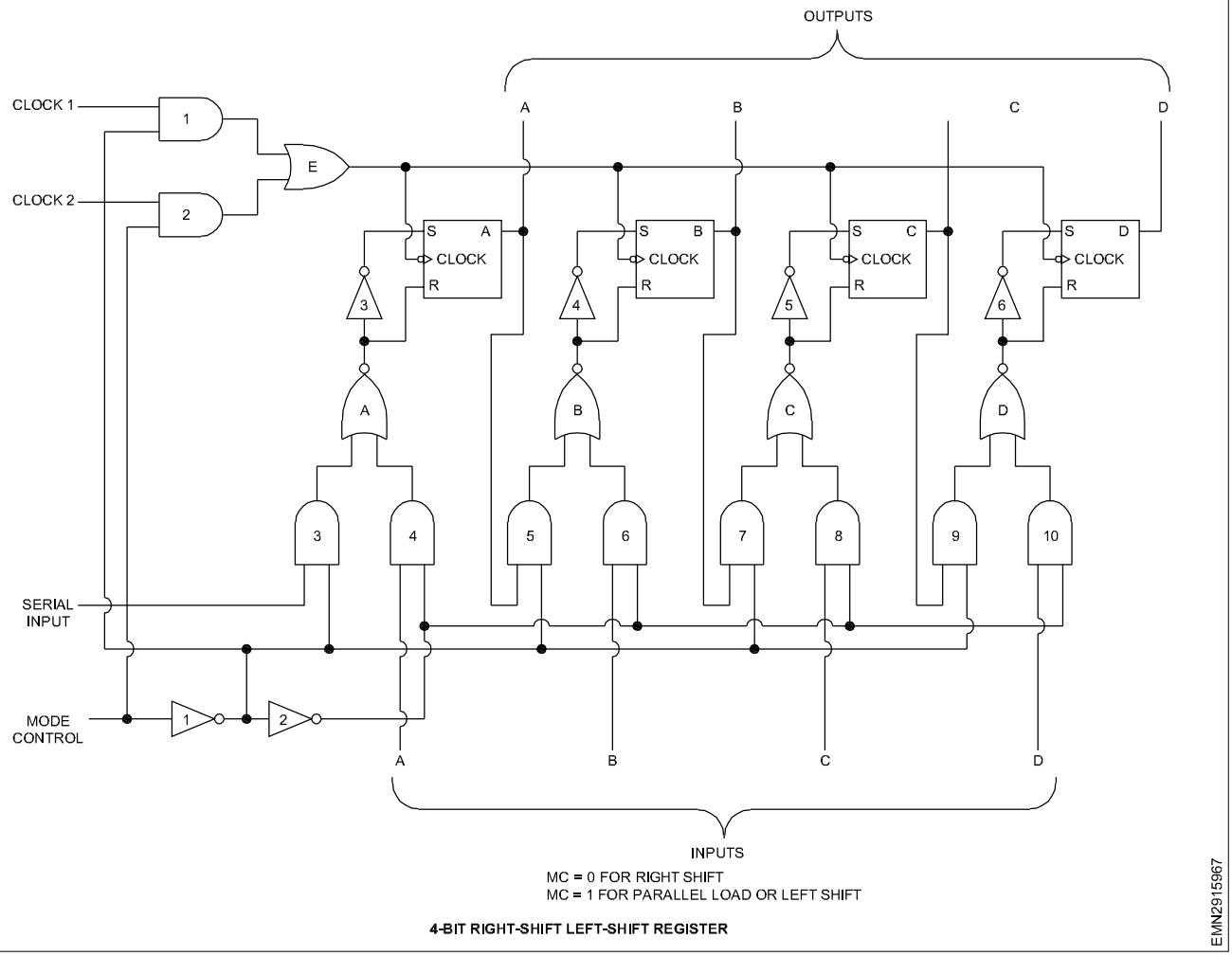
4-bit right-shift left-shift register IC7495

The Fig 7 shows the internal logic diagram of 4 bit shift register with parallel load capability, and with all flip-flop outputs available. This makes it possible to perform the right shift or left shift operation under control of the mode control input. For greater flexibility, the mode control selects clock-1 for the right shift mode and clock 2 for the parallel load (left shift) mode. The clock 1 and clock 2 inputs are tied together if only one clock source is required. Data transfer occurs once the -ve going edge of the clock pulse occurs.

Parallel In Parallel Out (PIPO)

The Fig 8 shows the pins to be used for parallel in parallel out operation in IC7495. For this operation mode control

Fig 7

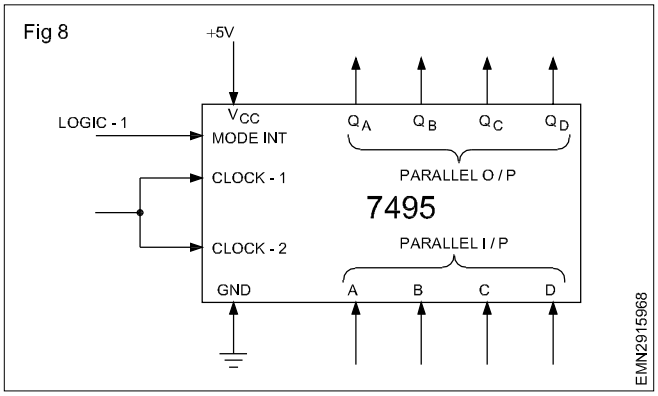


4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER

should be kept at logic high. Clock 2 should selected for applying clock pulse, data inputs are to be connected to the A,B,C & D parallel inputs, data output can be taken simultaneously from Q_A, Q_B, Q_C and Q_D.

When mode control is at logic high, inverter 1 output will be at logic-0. Hence AND gates 1,3,5,7 and 9 are disabled because one of the inputs of those gates will be at logic-0. Therefore clock 1 and serial inputs will be disconnected from the flip-flops. At the same time AND gates 2,4,6,8 and 10 are enabled because, both the AND gate inputs of enabled gates will have high inputs simultaneously, when clock is high. Hence only clock 2 and parallel inputs are routed to the flip-flop inputs. Falling edge of the clock pulse, transmits the data information from parallel inputs to parallel outputs, simultaneously.

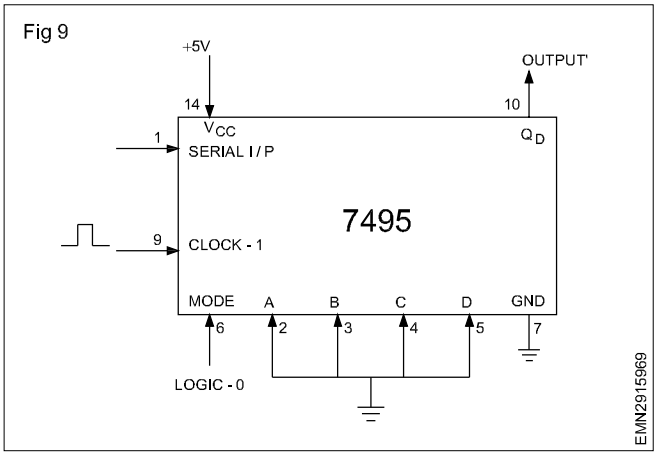
This type of register requires very less time (i.e one clock



pulse) for transfer 1 set of parallel data information.

Serial In Serial Out (SISO)

The Fig 9 shows the pins to be used for SISO operation in IC 7495. When the mode control input is at logic-0 condition inverter 1 (refer functional diagram of 7495 for inter blocks) output will be at logic-1 and that enables AND

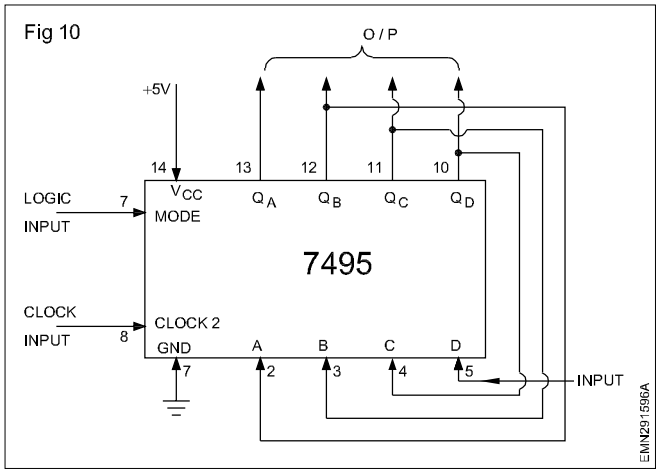


gates 3,5,7,9 and 1. AND gate-1 selects clock-1 status for triggering flip-flops through OR gate. AND gates 3,5,7,9 selects serial input data. At the same time inverter-2 output will be at logic-0 that disables AND gates 4,6,8,10 thus disconnecting all parallel inputs A,B,C and D reaching flip-flop 4 clock pulses are required to transfer data from input to output of the shift register.

If the outputs are taken from all the outputs Q_A, Q_B, Q_C and Q_D, then this register works like serial in parallel out (shift right) register.

Serial In Parallel Out (shift left)

The Fig 10 shows external wiring diagram for serial in parallel out shift left register. For shift left operation mode control signal level should be logic-1.



Data input is applied to the parallel input-D remaining parallel inputs A, B and C receives signals from the outputs Q_B, Q_C and Q_D respectively as shown in Fig 10.

When mode control signal is at logic-1 AND gate 2 is enabled and AND gate 1 is disabled. Hence all the flip-flops get triggering pulse from clock 2. At the same time AND gates 3,5,7 and 9 are disabled and AND gates 4,6,8 and 10 are enabled, therefore parallel inputs A,B,C and D routed to the flip-flops inputs, and serial input is disabled from the flip-flops. The data input given at the D input is shifted left as the clock pulse progress. To move data from Q_D to Q_A, 4 clock pulses are required.

Analog-to-Digital Converter

Objectives: At the end of this lesson you shall be able to
- **explain the function of A to D converter and its types**
- **explain successive-approximation method of A/D converter**
- **state the characteristic of ADC0809 IC.**
- **list the application of ADC**

In electronics there are several circuit designed according to requirements. An analog-to-digital converter is a circuit that converts an analog signal from a microphone or a digital camera, into a digital signal.The schematic representation of ADC is shown in Fig 1

Fig 1

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This electronic circuit directly converts the continuous form of signal to discrete form is also expressed as A/D or A-to-D or ADC .

Analog to digital conversion is necessary when measured quantities must be in digital form for processing in a computer for display or storage. This A/D converter is a linkage between the analog (linear) world of transducers measuring parameter like temperature, pressure, vibration etc into equivalent digital signals for discrete world of processing the signal and handling the data.

The major factors that determine the quality performance of A/D converter are resolution, sampling rate, speed and linearity. The resolution is the smallest change in voltage that can be detected by the system and that can produce a change in the digital code.

The speed of a A/D converter is determined by the time it takes to perform the conversion process. Analog signal can be converted to digital codes by many methods of which successive approximation and flash A/D conversion methods are most common

Types of Analog to Digital Converter

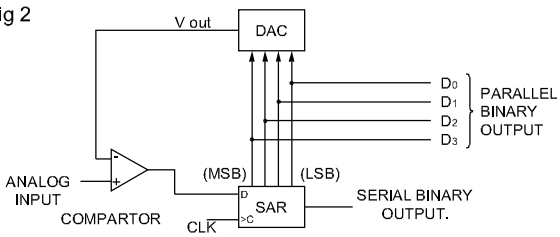
- Successive Approximation ADC: This converter compares the input signal with the output of an internal DAC at each successive step. It is the most expensive type.
- Dual Slope ADC: It has high accuracy but very slow in operation.
- Pipeline ADC: It is same as that of two step Flash ADC.
- Delta-Sigma ADC: It has high resolution but slow due to over sampling.
- Flash ADC: It is the fastest ADC but very expensive.
- Other: Staircase ramp, Voltage-to-Frequency, Switched capacitor, tracking, Charge balancing, and resolver.

Successive-approximation A/D converter

Successive approximation is perhaps the most widely used method of A/D conversion. It has a much shorter conversion time, it also has fixed conversion time that is the same for any value of the analog input.

The Fig 2 shows basic block diagram of a 4 bit successive approximation ADC. It consists of a DAC, a successive-approximation register (SAR), and a comparator.

Fig 2



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The basic operation is as follows:

The input bits of the DAC are enabled (made equal to logic-1) one at a time, starting with MSB, as each bit is enabled, the comparator produces an output that indicates whether the analog input voltage is greater or less than the output of the DAC for the corresponding I/p. If the DAC output is greater than the analog input, the comparator's output is low, causing the bit in the register to RESET. If

Fig 3

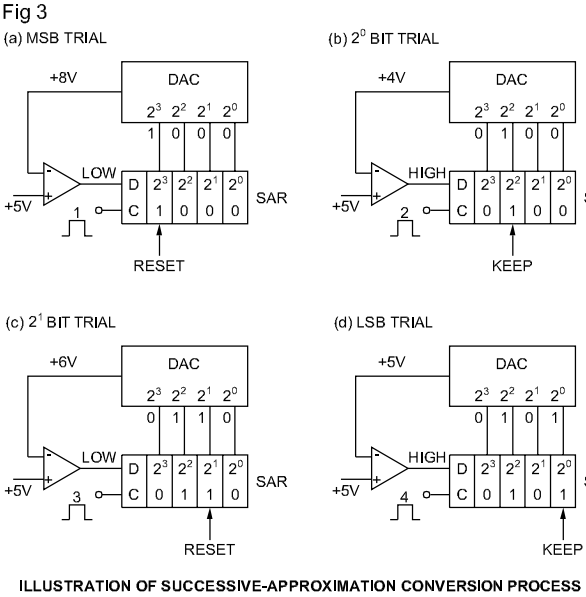

ILLUSTRATION OF SUCCESSIVE-APPROXIMATION CONVERSION PROCESS

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the DAC output is less than the analog input the '1' bit is retained in the SAR register. The system does this with the MSB first, then the next most significant bit, then the next and so on. After all the bits of the DAC have been tried, the conversion cycle is complete.

Fig 3 illustrates the step-by-step conversion of a constant analog input voltage (5V in this case). Let us assume that the DAC has the following output characteristic: V_{out} = 8V for the 2^3 bit (MSB), V_{out} = 4V for the 2^2 bit, V_{out} = 2V for the 2^1 bit and V_{out} = 1V for the 2^0 bit (LSB).

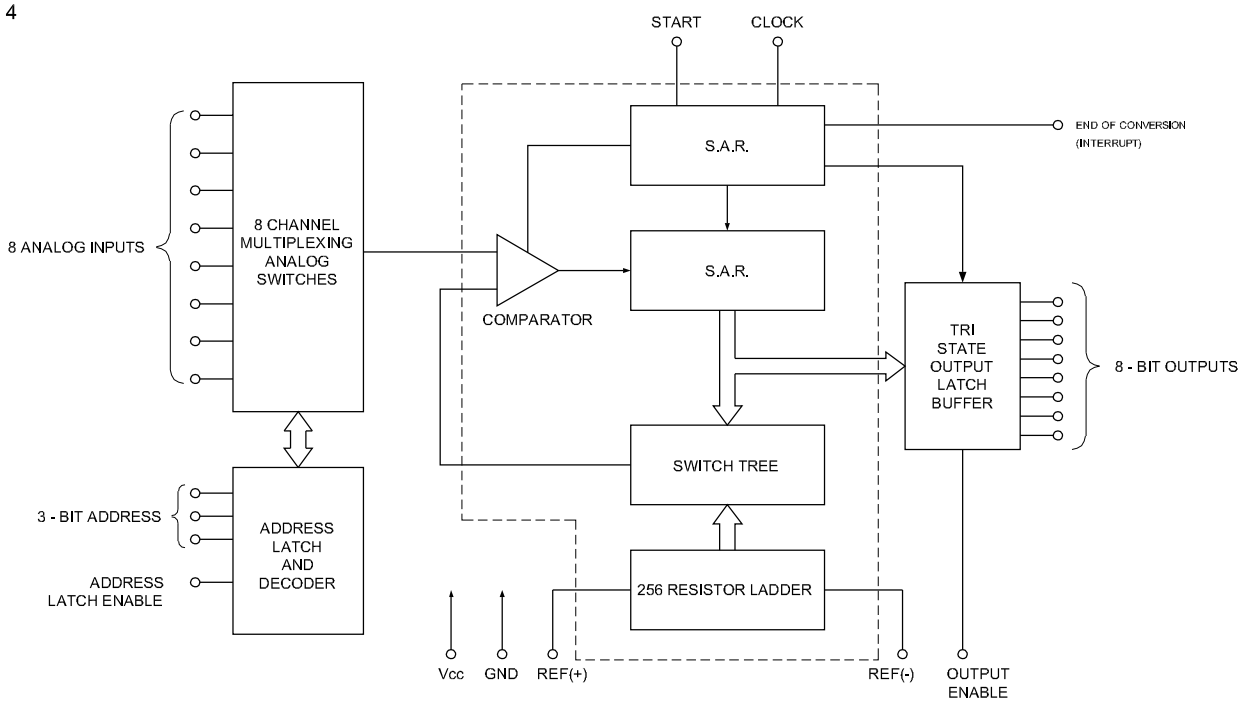
Fig 3a shows the first step in the conversion cycle with the MSB=1, the output of the DAC=8V. Since this is greater than the analog input of 5V, the output of the DAC is 8V. Since this is greater than the analog input of 5V, the output of the comparator is low, causing the MSB in the SAR to be reset to a logic-0.

Fig 3b shows the second step in the conversion cycle with the 2^2 bit equal to a logic-1. The output of the DAC is 4V, since this is less than the analog input of 5V, the output of the comparator switches to a HIGH, causing this bit to be retained in the SAR.

Fig 3c shows the third step in the conversion cycle with the 2^1 bit equal to a logic-1. The output of the DAC is 6 volts because there is a logic-1 on the 2^2 bit input and on the 2^1 bit input 4V+2V=6V, since this is greater than the analog input of 5V, the output of the comparator. Switches to a LOW, causing this bit to be RESET to a logic-0.

Fig 3d shows the fourth and final step in the conversion cycle with the 2^0 bit equal to a logic-1. The output of the DAC is 5V because there is a logic-1 on the 2^2 bit input and on the 2^0 bit input 4V+1V=5V.

Fig 4



BLOCK DIAGRAM OF 8 - BIT MICROPROCESSOR COMPATIBLE ANALOG TO DIGITAL CONVERTERS

The four bits have all been tried, thus completing the conversion cycle. At this point the binary code in the register is 0101, which is the binary value of the analog input of 5V. Another conversion cycle now begins and the basic process is repeated. The SAR is cleared at the beginning of each cycle.

Analogue to digital converter ADC0808/0809 8 bit microprocessor compatible A/D converter

The ADC0808/0809 data acquisition device implement on a single chip most the elements of the standard data acquisition system. They contain an 8-bit A/D converter, 8 channel multiplexer with an address input latch and associated control logic. These device provide most of the logic to interface to a variety of microprocessors with the addition of a minimum number of parts.

Functional description

The ADC0808/0809 shown in the above Fig 4 can be functionally divided into 2 basic sub circuits. These two sub circuits are an analog multiplexer and an A/D converter. The multiplexer uses 8-standard CMOS analog switches to provide for upto 8 analog inputs, the switches are selectively turned on, depending on the data latched into 3-bit multiplexer address register.

The second function block, the successive approximation A/D converter transforms the analog output of the multiplexer to an 8 bit digital word, the output of the multiplexer goes to one of two comparator inputs. The other input is derived from a 256R resistor ladder, which is tapped by a MOSFET transistor switch tree. The converter control logic controls the switch tree, funneling a particular tap voltage to the comparator, based on the result of this comparison, the control logic and the successive approximation register (SAR) will decide whether the next tap to be selected should be higher or lower than the present tap on the resistor ladder, this algorithm is executed 8 times per conversion, once every 8 clock periods, yielding a total conversion time 64 clock period.

When the conversion cycle is complete the resulting data is loaded into the tri-state output latch can then be read by the host system any time before the end of the next conversion. The try state capability of the latch allows easy interface to bus oriented systems.

Application of ADC

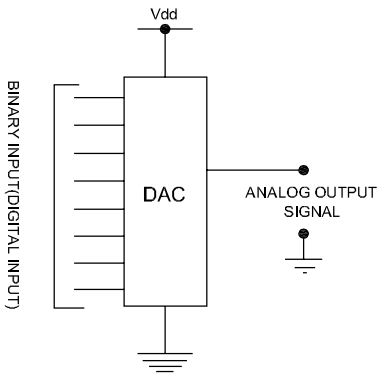
- Used together with the transducer.
- Used in computer to convert the analog signal to digital signal.
- Used in cell phones.
- Used in microcontrollers.
- Used in digital signal processing.
- Used in digital storage oscilloscopes.
- Used in scientific instruments.
- Used in music reproduction technology etc.

Digital -to- Analog converter

Objectives: At the end of this lesson you shall be able to
- **explain the function of digital to analog converter**

Digital to Analog Converter (DAC) is a device that transforms digital data into an analog signal. A DAC can reconstruct sampled data into an analog signal with precision. The digital data may be produced from a microprocessor, Application Specific Integrated Circuit (ASIC), or Field Programmable Gate Array (FPGA), but ultimately the data requires the conversion to an analog signal in order to interact with the real world. The block diagram of Basic Digital to Analog Converter is shown in Fig1.

Fig 1



BLOCK DIAGRAM OF DAC

D/A Converter Architectures: There are two methods commonly used for digital to analog conversion: Weighted Resistors method and the other one is using the R-2R ladder network method.

DAC 0808 Digital to Analog converter

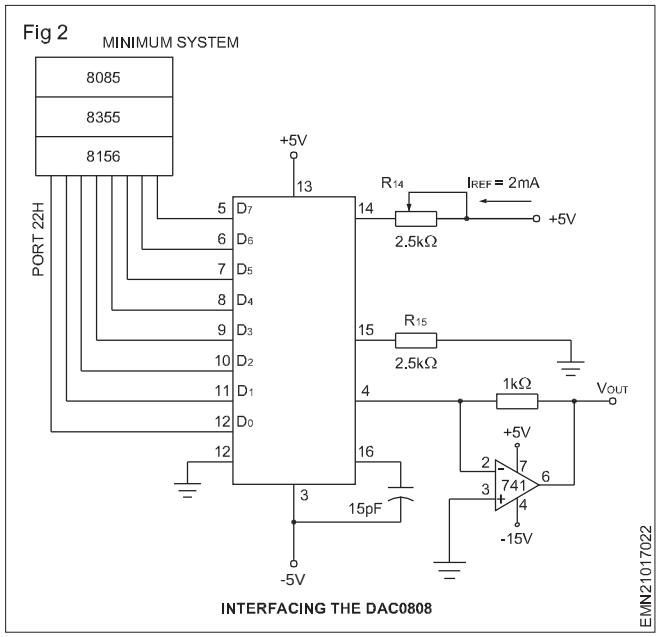
The DAC 0808 series is an 8 bit monolithic digital-to-analog converter (DAC) featuring a full scale output current setting time of 150ns while dissipating only 33mw with ±5V supplies. No reference current (I_{ref}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{ref}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity, while zero level output current of less than 4μA provides 8-bit zero accuracy for I_{ref} = 2mA, the power supply currents of the DAC 0808 series are independent of bit codes and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC 0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408.

The Fig 1 shows the data bits of a DAC0808 connected to port 22H of minimum system. Pin 2 of the DAC0808 is grounded, and a 15pF compensating capacitor is between pins 16 and 3, +5V supply sets up a reference current for the R-2R ladder, pin 14 is connected to a positive supply through a resistor (trimmer) R_{14} allows you to adjust this to 2mA and pin 15 is grounded through a resistor R_{15} is the same size as R_{14}; this compensates for drift in the input stage of the converter. Notice that I_{out} drives the inverting input of an op-amp; therefore the final output ranges from 0 to +2V. Pin 1 is unused, pin 2 is chip ground, pin 3 (V_{EE}) is -5V, pin 4 is the ground return for the current out of the ladder; this pin usually connects to an op-amp, pin 5 to 12 are for the 8 bits of input data, Pin 13(V_{CC}) is +5V. Finally a capacitor between pin 16 and pin 3 frequency-compensates the device.

Grounding and bypassing

Fig 2



INTERFACING THE DAC0808

D/A and A/D converter IC(s) require correct grounding and capacitive bypassing in order to operate according to performance specifications. The digital signals can

severely impair analog signals to contact the electromagnetic interference caused by the digital signals, the analog and digital grounds should be kept separate and should have only one common point on the circuit board. Bypass capacitors are required at the power connections to the IC, the reference signal inputs and the analog inputs to minimize noise that is induced by the digital signals. Manufacturer specifies the recommended bypass capacitor locations and values in the data sheet.

The typical DAC 0808 Digital to Analog converter is shown in Fig 2 and its working is explained below:

Applications of Digital to Analog Converter

DACs are used in many digital signal processing applications and many more applications. Some of the important applications are discussed below.

- **Audio Amplifier** DACs are used to produce DC voltage gain with Microcontroller commands. Often, the DAC will be incorporated into an entire audio codec which includes signal processing features.
- **Video Encoder** the video encoder system will process a video signal and send digital signals to a variety of DACs to produce analog video signals of various formats, along with optimizing of output levels. As with audio codecs, these ICs may have integrated DACs.
- **Display Electronics** the graphic controller will typically use a lookup table to generate data signals sent to a video DAC for analog outputs such as Red, Green, Blue (RGB) signals to drive a display.
- **Data Acquisition Systems** data to be measured is digitized by an Analog-to-Digital Converter (ADC) and then sent to a processor. The data acquisition will also include a process control end, in which the processor sends feedback data to a DAC for converting to analog signals.
- **Calibration** the DAC provides dynamic calibration for gain and voltage offset for accuracy in test and measurement systems.
- **Motor Control** many motor controls require **voltage control signals,** and a DAC is ideal for this application which may be driven by a processor or controller.
- **Digital Potentiometer** almost all digital potentiometers are based on the string DAC architecture. With some reorganization of the resistor/switch array, and the addition of an I2C compatible interface, a fully digital potentiometer can be implemented.

Interfacing the digital and analog signals

Objectives: At the end of this lesson you shall be able to
- **differentiate between analog and digital system**
- **appreciate digital system over analog system**
- **state different methods used in D to A conversion**
- **explain performance characteristic of D to A converter**
- **explain characteristics of DAC 0808IC.**

Analog quantities are sometimes called real-word quantities because most physical quantities are analog in nature. Many applications of computers and other digital systems require the input of real-world quantities, such as temperature, speed, position, pressure and force. Real-world quantities can even include graphic images, also digital systems often must produce outputs to control real world quantities.

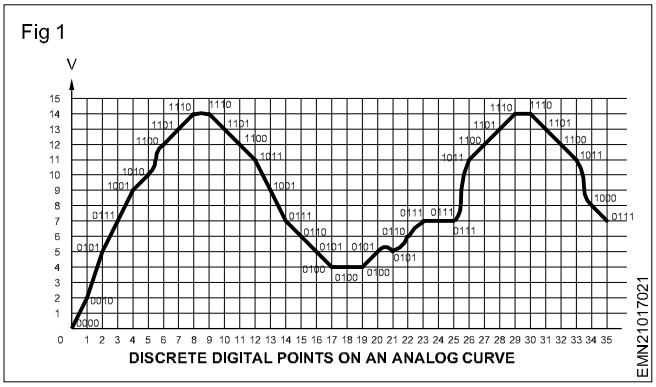
Digital and analog signals

An analog quantity is one that has continuous values over a given range, as contrasted with a discrete set of values for the digital case.

For Example: A voltage that varies over a range from +0 volts to +15 volts. The analog representation of this quantity takes in all values between 0 and 15V which are infinite in number.

In the case of a digital representation of the voltage using a 4-bit binary code, only sixteen values can be defined. More values between 0 and +15 can be represented by using more bits in the digital code. So an analog quantity can be represented to some degree of accuracy with a digital code that specifices discrete values with in the range. This concept is illustrated in Fig 1.

Fig 1

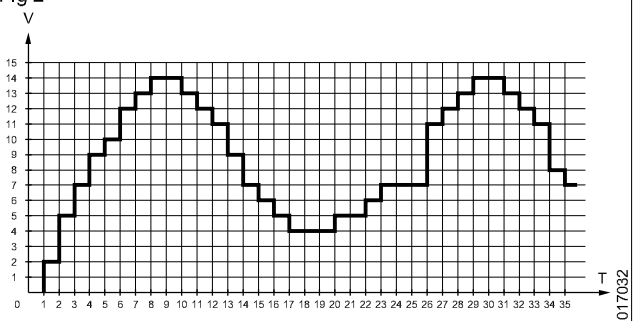


In the Fig 1 the voltage on the analog curve is measured, or sampled, at each of thirty five equal intervals. The voltage at each of these intervals is represented by a 4-bit code as indicated. At this point, we have a series of binary numbers representing various values along the analog curve. (This is the basic idea of A/D conversion)

An approximation of the analog function can be reconstructed from the sequence of digital numbers that

has been generated, obviously, there will be some error in the reconstruction because only certain values are represented, Thirty six shown in the Fig 2 and not the continuous set of values.

Fig 2



ROUGH DIGITAL REPRODUCTION OF THE ANALOG CURVE

If the digital values at all of the thirty six points are graphed as shown in Fig. 2 the graph only approximates the original curve.

Accuracy can be increased by sampling the curve more often and by increasing the number of bits used to represent each sampled value.

To interface between the digital and analog systems, two basic processes are required. They are analogue to digital converter and digital to analogue converter.

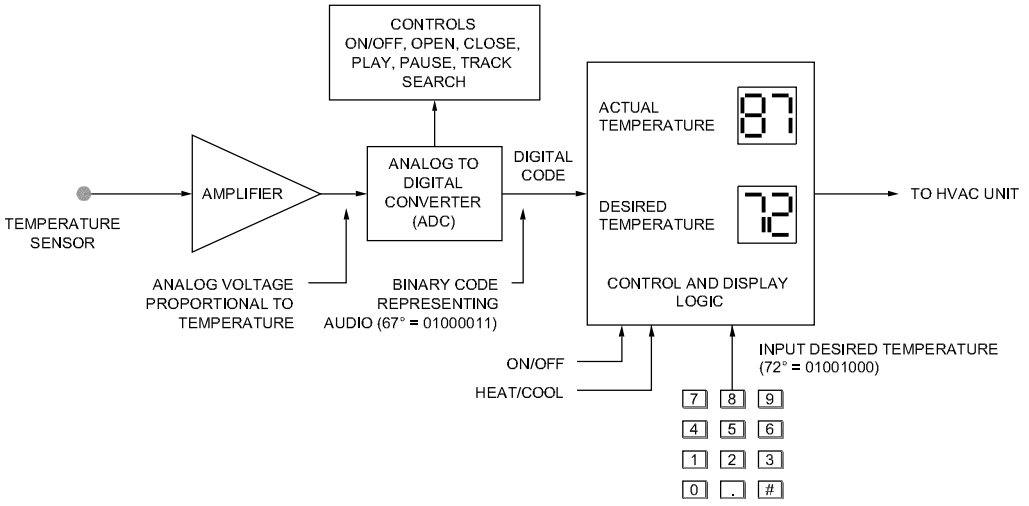
The following examples illustrate applications of these conversion processes.

Electronic thermostat

The Fig.3 shows the simplified block diagram of an electronic thermostat, the room temperature sensor produces and analog voltage that is proportional to the temperatue. This voltage is increased by the linear amplifier and applied to the analog - to-digital converter (ADC) where it is converted to a digital code and periodically sampled by the control logic.

For Example: The room temperature is 67°F. A specific voltage value corresponding to this temperature appears on the ADC input and is converted to an 8-bit binary number 01000011. The control logic compares this binary number with a binary number representing the desired temperature (say 01001000 for 72°F). This desired value has been previously entered from the key pad and stored in a register. The comparison shows that the actual room temperature is less than the desired temperature. As a result, the control logic instructs the control unit circuit to turn the furnace on. As the furnace runs, the control logic continues to monitor the actual temperature through the ADC. When the actual temperature equals or exceeds the desired temperature, the control logic turns the furnace off, both the actual temperature and the desired temperature are displayed.

Fig 3



BASIC BLOCK DIAGRAM OF AN ELECTRONIC THERMOSTAT

CD player

The compact-disk (CD) player is an example of a system that uses a digital to analog converter (DAC). The block diagram is shown in Fig 4, an audio signal is digitally recorded on the CD in the form of pits that are sensed by the laser pick up and amplified. The amplified digital signal is converted to a sequence of binary codes that represent the originally recorded audio signal, the binary representation of the audio is converted to analogue form by the DAC, amplified, and sent to the speakers.

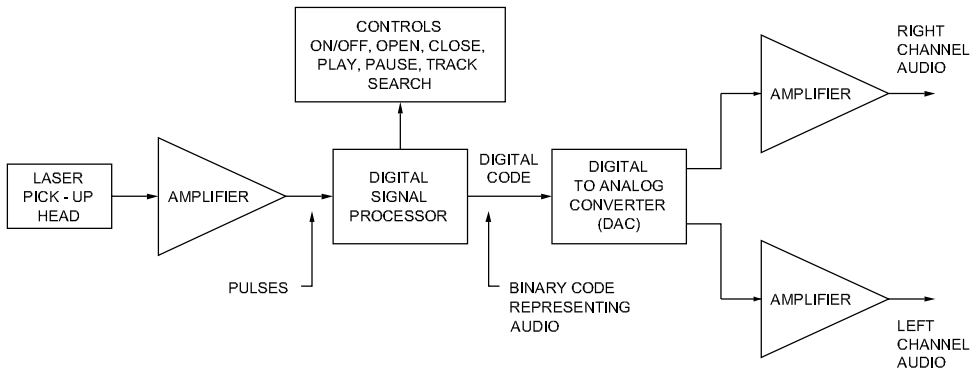
Digital-to-analog converter

Digital to analog converter is an important section in any digital system as indicated in the above two examples. OP-AMP is the most common element used in the D to A converter.

The basic problem in converting a digital signal into an equivalent analog signal is to change the 'n' digital voltage levels into one equivalent analog voltage. This can be most easily accomplished by designing a resistive network as shown in Fig 5, that will change each digital level into an equivalent binary weighted voltage or current.

The values of the input resistors network is chosen to be inversely proportional to the binary weights of the corresponding input bits, the lowest-value resistor(R)

Fig 4



BASIC BLOCK DIAGRAM OF A CD PLAYER

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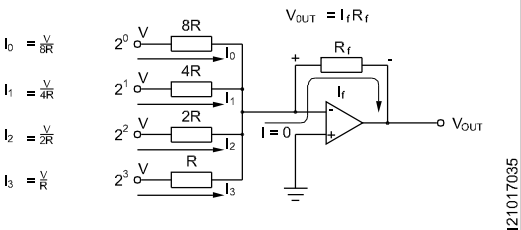
corresponds to the highest binary weighted input (2^n). The other resistors are multiples of R(2R, 4R and 8R) and correspond to the binary weights, 2^{n-1}, 2^{n-2}, 2^{n-3}.....2^{n-n} respectively.

The I/P currents are also proportional to the binary weights, thus the o/p voltage is proportional to the sum of the binary weights because the sum of the input current is through R_f.

The Fig 5 shows a 4 bit DAC, each of the input resistors will either have current or have no current, depending on the input voltage level. If the input voltage is zero (binary 0), the current is also zero. If the input voltage is HIGH (binary 1), the amount of current depends on the input resistor value and is different for each input resistor.

Since there is practically no current into the op-amp inverting input, all of the input currents SUM together and go through R_f, since the inverting input is at 0V (Virtual ground), the drop across R_f is equal to the o/p voltage, so $V_{out}=I_fR_f$.

Fig 5



FOUR BIT DIGITAL-TO-ANALOG CONVERTOR

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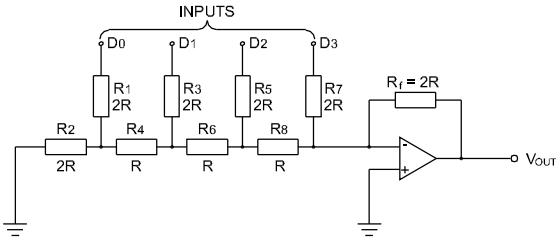
The main disadvantage of this type of DAC is the number of different resistor values. For example, An 8 bit converter requires eight resistors, ranging from some value of R to 128R in binary-weighted steps. This range of resistors requires tolerances of one part in 255 (less than 0.5%) to accurately convert the input, making this type of DAC very difficult to mass-produce.

R/2R ladder digital-to-analog converter

The Fig 6 shows another method of DA conversion using R/2R ladder resistor network, for four bits. It overcomes one of the problems in the binary-weighted input DAC. In this type DAC only two values of resistors are required R and 2R.

Assuming that the D_3 input is HIGH (+5V) and the others

Fig 6



R/R2 LADDER DIGITAL-TO-ANALOG CONVERTER

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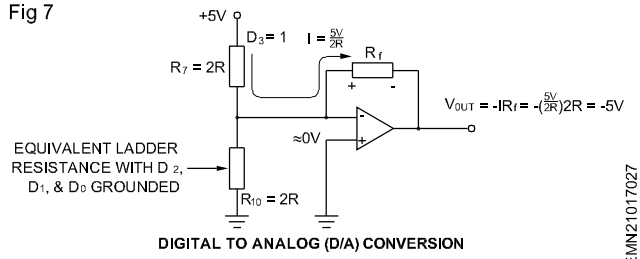
are LOW (ground 0V). This condition represents the binary 1000. A circuit analysis will show that this reduces to the equivalent form shown in Fig 7. Essentially no current goes through the 2R equivalent resistance because the inverting input is at virtual ground.

Thus all of the current (I=5V/2R) through R_7 also goes through R_f, and the output voltage is -5V. The operational amplifier keeps the inverting (-) input near zero volts (˜0V) because of -ve feedback. Therefore all current goes through R_f rather than into the inverting input.

When the D_2 input is at +5V and the others are at ground. This condition represents 0100. Thevanize the R2/2R ladder network looking from R_8, results in a current through R_f of I=2.5V/2R, which gives an output voltage of-2.5V. Keep in mind that there is no current into the Op-Amp inverting input and that there is no current through the equivalent resistance to ground because it has zero volts across it, due to the virtual ground.

Fig 7



DIGITAL TO ANALOG (D/A) CONVERSION

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When the input is 0010

When D_1 input is at +5V and the others are at ground, this condition represents 0010, again thevanizing the R_2/2R ladder network looking from R_8, results in a current through R_f of I=1.25V/2R, which gives an output voltage of -1.25 volts.

When the input is 0001

When D_0 input is at +5V and the others are at ground, this condition represents 0001, again thevanizing the R/2R ladder network looking from R_8, results in a current through R_f of I=0.625V/2R, which gives an output voltage of -0.625V.

Notice that each successively lower weighted input produces an o/p voltage that is halved, so that the output voltage is proportional to the binary weight of the input bits.

In equation form the o/p voltage is given by

$$V_{out} = \frac{D_0 2^0 + D_1 2^1 + D_2 2^2 + D_3 2^3 + ...D_{n-1} 2^{n-1}}{2^n}$$

where D_0, D_1, D_2, D_3.....D_{n-1} are the digital input levels.

Performance characteristics of digital-to-analog converter

Resolution

The resolution of a DAC is the reciprocal of the number of discrete steps in the output. This of course, is dependent on the number of input bits.

For example: A 4-bit DAC has a resolution of one part in 2^4-1 (one part in fifteen) expressed as a percentage, this is (1/15)x 100 = 6.67%. The total number of discrete steps equals 2^n-1, where n is the number of bits. Resolution can also be expressed as the number of bits that are converted.

Accuracy

Accuracy is a comparison of the actual output of a DAC with the expected output. It is expressed as a percentage of a full-scale, or maximum output voltage.

Example: If a converter has a full-scale output of 10V and the accuracy is ±0.1%, then the maximum error for any output voltage is (10V) (0.001)=10mV, ideally, the accuracy should be, at most ±1/2 of an LSB. For an 8-bit converter, 1 LSB is 1/256 = 0.0039 (0.39% of full scale), the accuracy should be approximately ±0.2%.

Linearity

A linear error is a deviation from the ideal straight-line output of a DAC. A special case is an offset error, which is the amount of output voltage when the input bits are all zeros.

Monotonicity

A DAC is monotonic if it doesn't take any reverse steps when it is sequenced over its entire range of input bits.

Settling time

Settling time is normally defined as the time it takes a DAC to settle within ±1/2 LSB of its final value when a change occurs in the input code.

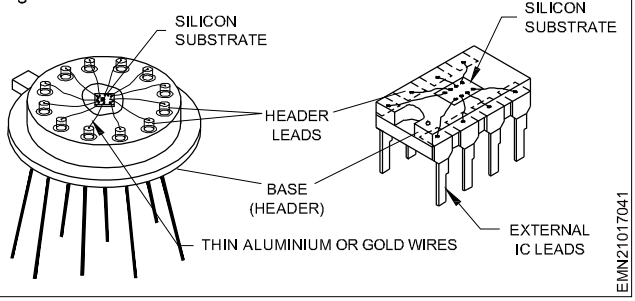
Operational amplifiers and their applications

Objectives : At the end of this lesson you shall be able to
- **state the base material used in making ICs**
- **state the most important considerations in designing ICs**
- **state the meaning of operational amplifier**
- **state the two basic modes of operation of Op- Amps**
- **list ideal and typical characteristics of Op-Amps**
- **explain a simple summing and differential amplifier**
- **state the meaning of slew rate and its importance.**

Integrated circuits

An integrated circuit (IC), as its name implies, is an integrated (put together) form of several components of a circuit on a single chip or wafer of a semiconductor material, generally silicon. ICs may have hundreds of active components (transistors, diodes) and passive components (resistors, capacitors etc.,).

Fig 1



The active and passive components are deposited or diffused on this minute sized silicon substrate. The substrate is then mounted on a ceramic or a insulated metal base called header as shown in Fig. 1. Aluminum or gold wires of about one-third thickness of a human hair are bonded between the IC contacts called pads and the header leads.

ICs are made by a complex photographic process on a very small sized surface. This process is known as micro photolithographic process

The base material of ICs is a highly refined silicon chip (also known as substrate) as shown in Fig 1. Generally the size of the silicon substrate is of the size of a pin head.

The number of pins each IC has depends on the complexity of the circuit built into the IC. However, any IC will have minuimum of 3 pins as in any voltage regulator ICs, to more than 64 pins in computer ICs.

In IC, fabrication of active components such as transistors and diodes take much less space on the chip than resistors and capacitors.

Direct coupling between transistor stages are used in ICs. Also transistors are used as resistors instead of fabricating resistors themselves. Components like chokes, coils and transformers cannot be fabricated in ICs because of its physical bulkiness. Therefore, wherever inductors are necessary for a circuit leads are brought out of the ICs such that, inductors can be connected external to the IC. Most ICs are designed to be used for more than one application by making small changes in external circuitry. For example, an IC may be used as an amplifier or as an oscillator and so on.

The commonly used OP-AMP ICs are μA741-single op-amp and LM 324 - having four op-amp. They come in DIP and having larger input voltage range no latch up, high gain short circuit protection, no frequency compensation required.

Input voltage range from -15v to +15v while common mode input is from -12v to +12v supply current is 1.7mA power consumption is 50 mV.

The leading IC manufactures are signetics, texas instruments, fair child and national semi conductors limited.

Advantages of integrated circuits

- Although the circuit inside an IC is complex consisting of a large number of components, the overall physical size of the IC is extremely small resulting in miniaturization of the electronic gadgets size.
- Drastic decrease in the overall weight of the gadget due to miniaturised size of the circuit.
- Low power requirement.
- Increased reliability due to less number of solder connections.
- Greater flexibility in use of the same IC for different circuit configurations.
- Better functioning under wide range of temperatures.
- Low cost per IC due to large scale production of ICs.

Limitation of integrated circuits

- Large value capacitors and resistors cannot be fabricated.
- Chokes, inductors and transformers cannot be fabricated.
- If any one stage inside the IC circuit becomes defective, the complete IC has to be discarded.
- Handling is very delicate.

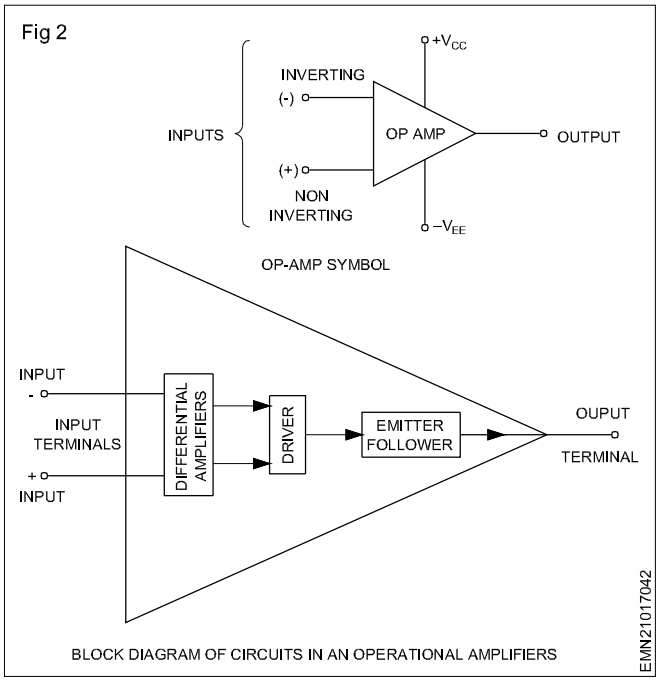
Basic linear integrated circuit-'Operational Amplifiers' (Op- Amps)

An operational amplifier, often referred as op-Amp, is a high gain, direct coupled differential amplifier, designed to amplify both DC and AC signals.

The term operational is used with these amplifiers because, in early days these amplifiers were used in analog computers to perform mathematical operations such as addition, multiplication etc.,

Symbol used to represent an Op-Amp and the functional blocks inside it are shown in Fig 2.

Fig 2

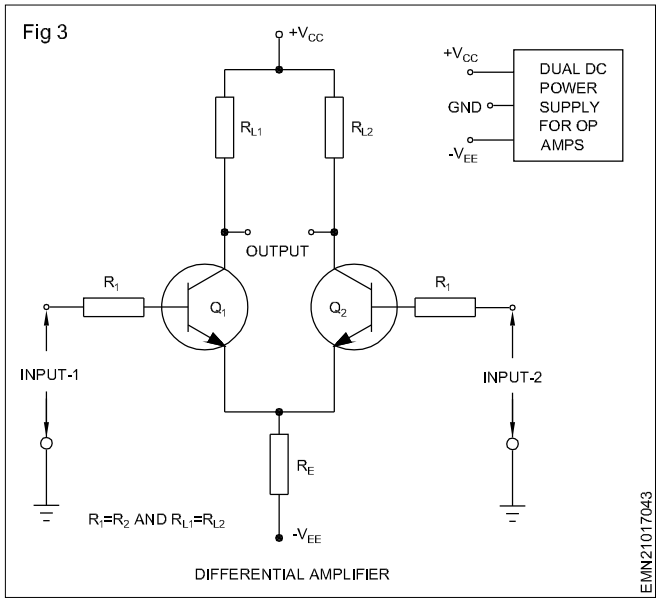


BLOCK DIAGRAM OF CIRCUITS IN AN OPERATIONAL AMPLIFIERS

As can be seen from Fig 3, operational amplifiers will have two inputs and one output. The reason for having two input points is that Op Amps have a special type of amplifier configuration known as Differential amplifier as its first stage.

A typical differential amplifier stage is shown in Fig 3. A differential amplifier stage consists of two transistors with an input to each transistor. The output is taken between the collectors of the transistors as shown in Fig. The most

Fig 3



DIFFERENTIAL AMPLIFIER

important point to note is, both the transistors have identical characteristics, load resistors, input resistors and a single emitter resistor. Dual power supply(+ve,-ve and Gnd) is required for differential amplifiers (single supply can also be used with a few extra components). If a dual supply is used and if the amplifier is properly balanced (symmetrical values), the output voltage across the collectors will be equal to the difference of the two input voltages. Hence, this amplifier is called differential amplifier.

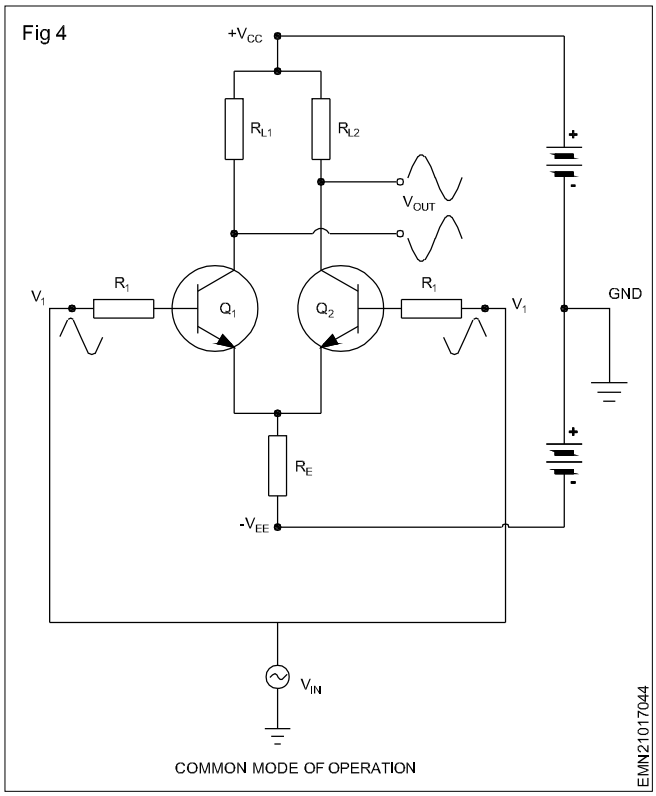
Modes of operation of differential amplifiers

Any operational amplifier can be operated in two modes. They are,

- Common-mode operation
- Differential-mode operation.

Common-mode operation

In Fig 4, since both sides of the differential amplifier circuit are identical, if an identical signal (same level and phase)



COMMON MODE OF OPERATION

is applied to both the inputs(transistors), the same output signal results from both collectors. If a meter is connected across the outputs the voltage difference will be zero. Thus, the output is equal to the gain times the difference between the input voltages. Mathematically, this is expressed as,

$V_{out\ (com)} = A(V_1\ V_2)$

Where,

A is the grain of each transistor

V_1 and V_2 are the base input voltages measured to ground.

This mode of operation is called Common-mode operation.

In common-mode operation, a differential amplifier theoretically rejects the common mode signals (signal that is identical at each input) and hence the output will be zero as shown below,

If both the magnitude and phase of V_1 and V_2 are the same, then,

$V_{out} = A(V_1\ V_2) = A\ (V_1 - V_1) = A\ (0)$

In practice, since the two halves of the circuit cannot be perfectly identical, instead of zero output there will be a very small output. For example, a differential amplifier with a 0.5 V common-mode input signal may give an output of 0.025 V instead of zero. This 0.025V is because of the slight mismatch between the two half of the differential amplifier circuit.

Differential-mode operation

Fig 5 shows the differential-mode operation. When the two input signals are out of phase by 180°, the amplifier amplifies the difference of the input signals. Since the input signals are of equal in amplitude, but out of phase by 1 80° the output signal is equal to, twice the gain times the input signal. This can be mathematically written as,If magnitude of $V_1 = V_2$ then,

$V_{out\ (Dif)} = A\ [\ V_1 - (\ -\ V_2\ )] = A\ [\ (2V_1)] = ..2A\ (V_1)$

Common-mode rejection ratio

The common-mode rejection ratio (CMRR) of a differential amplifier (or other device) is the rejection by the device of unwanted input signals common to both input leads, relative to the wanted difference signal. An ideal differential amplifier would have infinite CMRR; this is not achievable in practice. A high CMRR is required when a differential signal must be amplified in the presence of a possibly large common-mode input. An example is audio transmission over balanced lines.

Ideally, a differential amplifier takes the voltages, V_+ and V_- on its two inputs and produces an output voltage $V=A_d(V_+-V_-)$ where A_d is the differential gain. However, the output of a real differential amplifier is better described as

$V_o = A_d(V_+-V_-)+1/2A_{cm}(V_+-V_-)$,

Where is the common-mode gain, which is typically much smaller than the differential gain.

The CMRR is defined as the ratio of the powers of the differential gain over the common-mode gain, measured in positive decibels (thus using the 20 log rule):

As differential gain should exceed common-mode gain, this will be a positive number, and the higher the better.

The CMRR is a very important specification, as it indicates how much of the common-mode signal will appear in your measurement. The value of the CMRR often depends on signal frequency as well, and must be specified as a function thereof.

It is often important in reducing noise on transmission lines. For example, when measuring the resistance of a thermocouple in a noisy environment, the noise from the environment appears as an offset on both input leads,

making it a common-mode voltage signal. The CMRR of the measurement instrument determines the attenuation applied to the offset or noise.

Methods of giving input and taking output in differential amplifiers

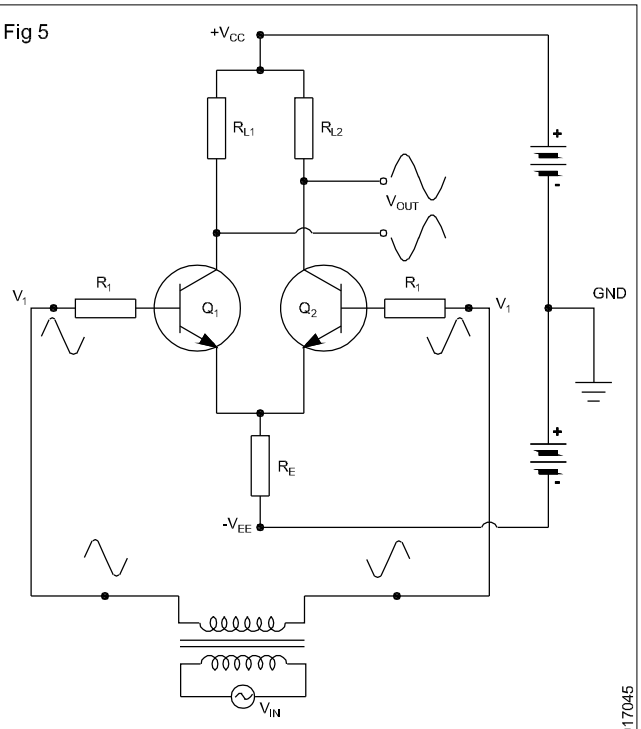
A differential amplifier is normally used with a double ended input and double ended output. But this is not a compulsion. A differential amplifier can also be used as single ended input and with single ended output.

Single-ended input: The input signal is applied to only one input and the other input is grounded as shown in Fig.6a.

Single-ended output:

The output can be taken from the collector of Q1 to Gnd or Q2 to Gnd or from both collectors to ground as shown in Fig 6b. when the output is taken from both collectors to Gnd the two signals provide a push-pull output as shown in Fig 6b.

Fig 5



DIFFERENTIAL-MODE OF OPERATION

Recall that the two transistors of a push-pull amplifiers need signal of some amplitude but out-of-phase by 180°.

Differential input:

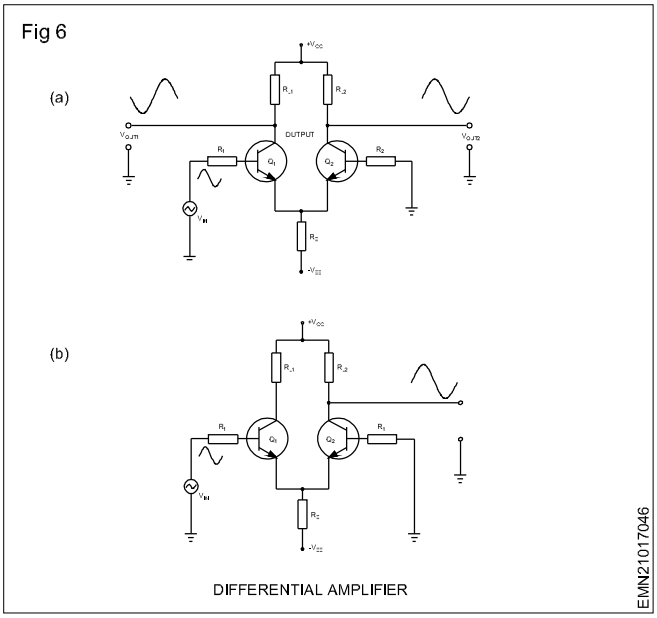
The two inputs given are signals having opposite polarity(180° out of phase). The input is similar to input to a push-pull amplifier.

Differential output: The output is taken across the two collectors which is nothing but the difference between the two collector voltages. The difference will be zero when the input voltages are equal and are of the same polarity. The input signals add up if they have opposite polarities.

Practical Op-Amps and applications

Most of the commercially available Op-Amp ICs will

Fig 6



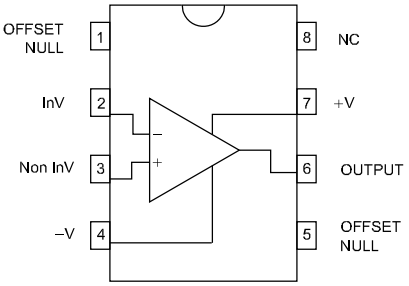
DIFFERENTIAL AMPLIFIER

usually have two input terminals and only one output terminal as shown in Fig 7. The two inputs of the Op-Amp are called, INVERTING(-) and NON-IN-VERTING(+) inputs. This is because, a signal applied to the inverting (-) input, produces output which will be 180° out of phase with the input. Whereas a signal applied, to the NON-INVERTING (+) input produces an output which will be in-phase with the input.

Gain of Op-Amps

The gain and other characteristics of the operational amplifier depends upon the external components connected externally to the Op-Amp.

Fig 7

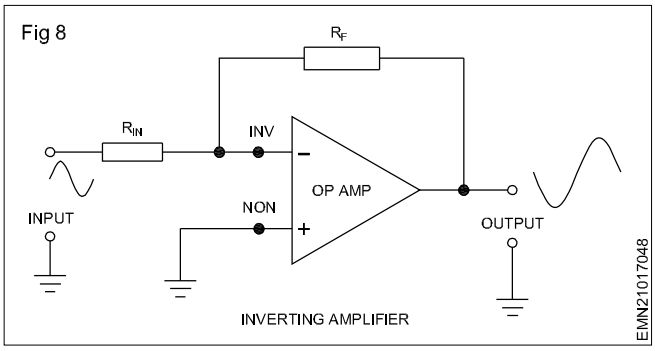


The theoretical gain of Op-Amps is very high, of the order of 100,000 or more. In practical amplifiers using Op-Amp, a resistor is used to provide an external negative feed back to the Op-Amp. The negative feedback resistor is generally connected between the output terminal to either of the input terminals as shown in Fig 8. Although the negative feed back reduces the gain of the amplifier drastically (10 to 1000), the negative feed back makes the amplifier stable, prevents it from going into oscillations and increases the frequency response range of the amplifiers.

The gain of Op-Amp without negative feedback is referred to as OPEN LOOP GAIN whereas, the gain of Op-Amp with feed back is referred to as CLOSED LOOP GAIN.

Op - AMP as inverting amplifier

Fig 8 shows a typical inverting amplifier using an Op-AMP. In this inverting amplifier, the input signal is applied to the INVERTING (INV)terminal. The NON-INVERTING (NON) terminal which is grounded the input signal is applied at the INV terminal, the output of the amplifier will be an amplified signal of opposite polarity. The resistor R_F between the output and input provides necessary negative feedback. The amount of negative feedback provided depends on the values of resistors R_F and R_{In}.



$$\text{Inverting Amplifier Gian } \left(A_{inv}\right) = -\frac{R_F}{R_1}$$

Negative sign indicates inverting of output signal generally, amplifier gain can also be written as

$$A = \frac{Vo}{V_{in}}$$

As an example, let us calculate the closed-loop voltage gain, for the inverting amplifier at Fig 8. Assume values of R_F = 470 KΩ and R_{in} = 47 KΩ. Assume an input signal voltage of 0.5V.

The closed-loop gain of an inverting amplifier is given by,

$$A_{inv} = \frac{R_F}{R_{in}}$$

$$A_{inv} = \frac{-470K}{47K} = -10$$

Since $R_F/R_{in} = A_{(inv)}$, equation can also be written as,

The out put voltage of the non – inverting amplifier is given by,

$V_{out(inv)} = A_{(inv)} \cdot V_{in}$

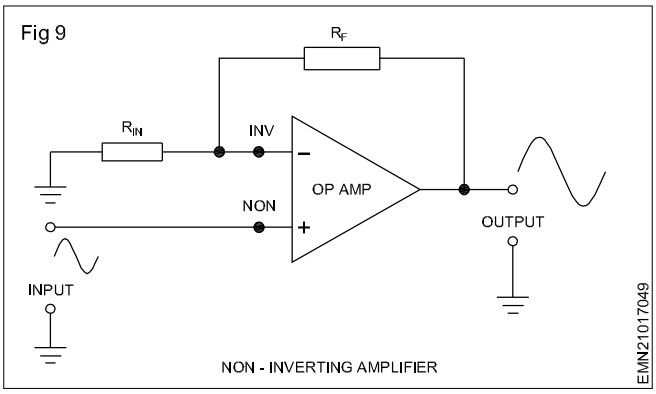
in the given example,

$V_{OUT\ (NON)}$ = 10x0.5 v

= 5.0 Volts

OP Amp non inverting amplifier

In the Fig. 9 shows a typical amplifier using OP-Amp. In this non-inverting amplifier, the input signal is applied to the non-inverting (NON) terminal. The output signal of



amplifier is same polarity (inphase) of applied input signal. The resistor R_F between output and input providing necessary feedback. The amount of feedback provided by amplifier depends on value of R_F and R_{in}.

$$\text{For gain } A_{(NON)} = \frac{V_{out}}{V_{in}} = \frac{R_{in} + R_F}{R_{in}} = 1 + \frac{R_F}{R_{in}}$$

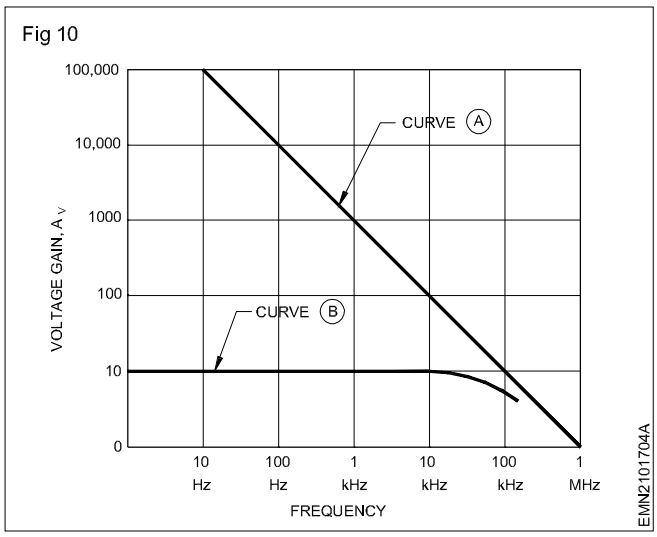
Gain-bandwidth product(GBP)

Typical frequency response of an Op-Amp is from direct current, or 0 Hz, to more than 1 MHz. However, because of internal shunt capacitances, the amplifier gain drops off sharply as the frequency is increased Therefore to specify the gain of an Op-Amp at different frequencies, a term called as Gain-Bandwidth-Product(GBP) is specified. For example, if the GBP of an Op-Amp is given as 1MHz, it means that the gain of the Op-Amp becomes unity at an input signal of 1 MHz. It is always useful to know the gain-bandwidth product (GBP), of the Op-Amp being used.

Example: The GBP of an Op-AMP is specified as 1 MHz. What is the maximum gain that can be obtained using this Op- Amp at 1 kHz GBP of 1 MHz means, gain = 1 at 1 MHz. Therefore, at 1 kHz more gain will be,

$$\text{Gain at 1kHz} = \frac{GEP}{1kHz} = \frac{1MHz}{1kHz} = 1000$$

This means, at 1 kHz an OpAmp with GPB of 1 MHz provides a maximum gain of 1000. This is shown in curve A of Fig 10.



Curve A of Fig 10 shows the open loop frequency response of an Op-Amp with a constant GBP of 1 MHz. As can be seen from curve A, for the same Op-Amp, the gain is 100 at 10 kHz, 10 at 100 kHz and becomes unity at 1 MHz.: This huge variation in open loop gain $A_{(OPEN)}$, can be made almost constant using negative feedback.

As shown in curve B of Fig 10, using suitable value of resistor R_F and R_{in}, if the closed loop gain $A_{(CIOSED)}$ of the Op-Amp is set at say 10, then the frequency response of the Op-Amp becomes almost flat upto 100kMz. This is one of the major advantages of negative feed back in Op-Amps.

TIP: The lower you set the gain of the amplifier, the higher will be the bandwidth of the amplifier.

Characteristics of Op-Amps

An ideal operational amplifier will have the following characteristics:

Voltage gain $A_V = \infty$

Bandwidth BW = ∞

Input resistance $R_{in} = \infty$

Output resistance $R_0 = 0$.

In practice such ideal characteristics cannot be achieved. However, in many practical situations, Op-Amps come close to these characteristics. Typical specifications of an Op-Amp is given below:

Voltage gain, $A_V \leq 100, 000$

Bandwidth, BW $\approx$ 1 MHz (unity gain)

Input resistance, R_{in} 2 MΩ

Output resistance $R_0 \leq 50\ \Omega$

Typical Op-Amp applications

Application of Op-Amps are innumerable. This is because, of the flexibility that is built into the internal circuit of the Op-Amp. In addition to its basic function of amplification, Op-Amp are used as comparators, adders, subtracters, differentiator, integrators and so on.

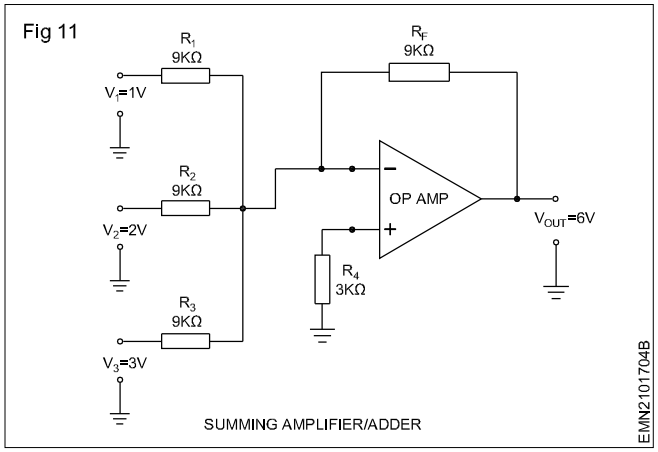
Application of Op-Amp as a summing amplifier

Fig 11 is the circuit of a Op-Amp summing amplifier or in simple terms an adder. Here, the Op-Amp is used as an inverting amplifier to do the summing operation. In Fig 11, three input signals are applied to the INV terminal of the Op-Amp through resistors R_1 R_2 and R_3. The amount of negative feedback given to the Op-Amp is dependent on the value of R_F divided by each resistor in the feedback path. As a result, the output voltage of the Op-Amp is given by,

$$V_{out} = \left[\left(\frac{R_f}{R_1} x V_1\right)\right] + \left(\frac{R_f}{R_1} x V_2\right) + \left(\frac{R_f}{R_1} x V_3\right)$$

If, $R_1 = R_2 = R_3 = R_F$, then R_F/R becomes 1 in each signal path.

Fig 11



Then, the output is given by,

$V_{out} = V_1 + V_2 + V_3$

$V_{out} = (1x1V) + (1x2V) + (1x3V)$

$V_{out} = 1V + 2V + 3V = 6$Volts

The output of 6V is equal to the sum of the three input voltages. Note that the value of resistor R_4 (3K) at the NON terminal of Op-Amp is made equal to the parallel combination of three 9 K resistors at the INV terminal. This resistor is required to balance the inputs of the differential amplifier in the Op-Amp.

Slew rate in Op-Amps

Slew rate is an important characteristic of Op-Amps. The term slew refers to the rate of change of the output voltage. As an example, a slew rate of 1 volt per microsecond (V/μS) means, the amplitude of output voltage can change by a maximum of 1 V in 1μS. Fast slew rate or high slew rate is desirable for high frequency amplifiers, especially those with non-sinusoidal input signal wave shapes.

DC supply voltage for Op–Amps

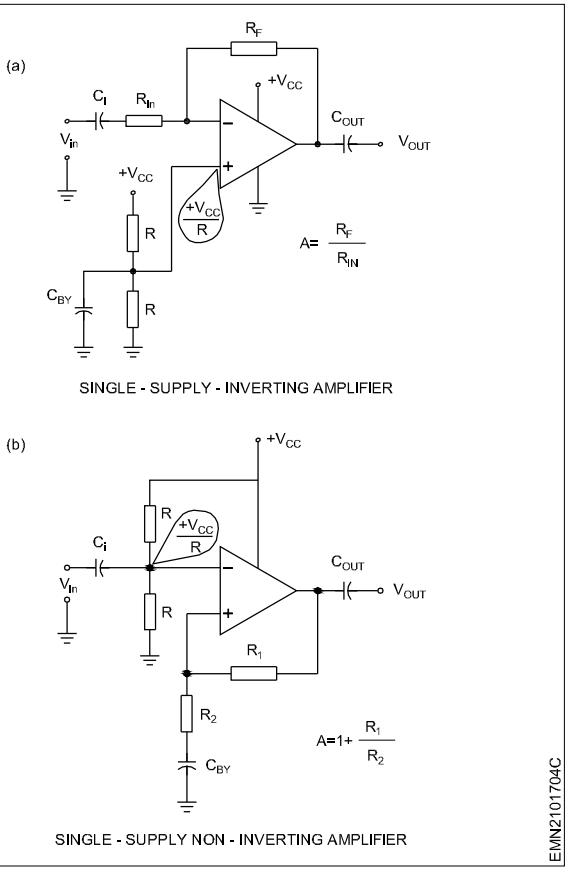
Op-Amps generally need dual (+ Ve, com,-Ve) DC supply. Typical values of DC supply voltages are $\pm$ 9 V $\pm$ 15 V and $\pm$ 12V. Note that both positive and negative voltages of same amplitude is required for Op-Amps. The V+ is used as the collector voltage, and the V- is used as the emitter supply voltage of the first differential amplifier stage of the Op Amp as shown in Fig.4

The DC load current drawn from the power supply for an Op-Amp is generally less than a few milliamps. Typical power rating of Op-Amps is around 500 mW.

Commercial Op-Amp ICs

The earliest and most popular commercial Op-Amp is the 741 IC. This Op-Amp IC is manufactured by several manufacturers, and hence, carries along with it tags such as uA 741(Fairchild), LM 741 (National semiconductor) and so on. Commercially several other types of Op-Amp ICs having different type numbers are available in the market. Some IC packages may consist of more than one Op-Amp built-in a single package. For instance, LM324 (National semiconductors) is a quad-operational amplifier. The term quad means it has four Op-Amp in one package.

Fig 12



Some of the popular Op-Amps and its specifications manufactured by National Semiconductors)

Single supply operation of Op-Amps

Most Op-Amp circuits are designed to work using dual (±) DC power supply. Due to some inconvenience of dual supplies, many Op-Amp circuits are made to work using single supply. The method of making Op-Amps to work with single-supply is shown in Figs 12a and 12b.

Noise in operational amplifiers

Undesired electrical signals present in the output of an amplifier is referred to as *noise.* Noise in the output of a circuit may be due to the noise generated in the circuit (internal) or noise getting into the circuit from external sources. External noise can be minimised by adopting proper construction techniques. A few tips to reduce external noise is listed below;

1) Shorten the interconnecting wire lengths. Mount components as close to the Op-Amp as possible. Keep the output circuit components away from the input components (this avoids unwanted feedback).
2) Bypass the Op-Amp $+V_{CC}$ supply pins using 0.01 to 0.1 uF disc capacitors.

Even if there is no significantly visible/audible noise at the output, there will be some noise in the output of Op-Amp due to internal noise. This internal noise can be minimised by avoiding large values of R_{in} and R_F. This internally generated noise due to resistors can be reduced to a large extent by connecting a small capacitor in the range of 3 to 56 pF across feedback resistor R_F. This will reduce internal noise, specially the high frequency noise.

Op-Amp applications - comparators, differentiator

Objectives : At the end of this lesson you shall be able to
- **explain the zero crossing detector circuit using Op Amp IC uA 741**
- **describe op-amp as comparator, differentiator.**

Applications of op-amp:

Op-amp is a building block of linear or analog systems. It has countless applications.

(i) It is used in non linear analog systems- the non linear applications are comparator, rectifer, clipper, clamper, log and antilog amplifier, multiplier etc.

(ii) It is used in linear circuits, the output varies with input signal in a linear manner.The linear applications are adder, subtractor, voltage to current converter, current to voltage converter,differentiator, integrator, differential amplifier, instrumentation amplifier and etc.

Comparator :

An operational amplifier in the open loop configuration operates in a non linear manner. Comparator, detector, limiters and converters work in this mode.

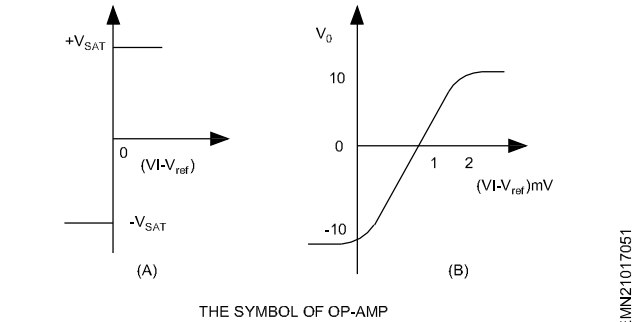
A comparator is a circuit which compares a signal voltage at one input of an op-amp with the known reference voltage at the other input. There are two types of comparator

(i) non - inverting comparator

(ii) inverting comparator

The output of an op-amp is + V_{sat}= ($+V_{cc}$) and $-V_{sat}$ ($-V_{cc}$) in the ideal transfer characteristics and commercial transfer characteristics is shown in Fig1.

Fig 1

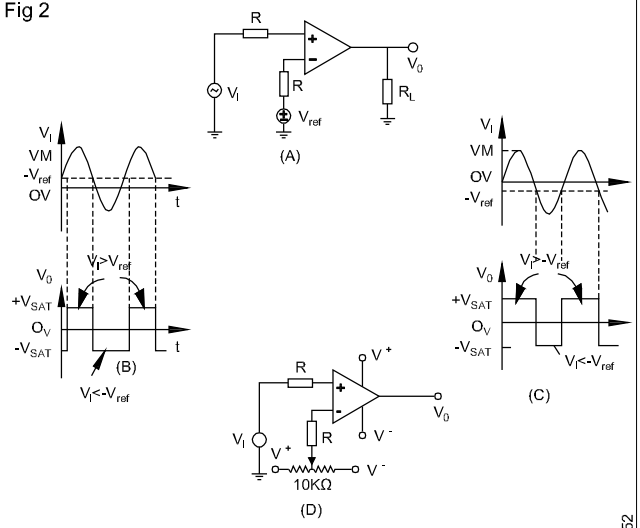


Non -inverting comparator :

If the fixed reference voltage is applied to the (-) input, and the time varying signal voltage V_{in} is applied to the (+) input, then the arrangement is called non inverting amplifier.

The output voltage is at $-V_{sat}$ for the applied input voltage less than the reference voltage ($V_i < V_{ref}$). And goes to $+V_{sat}$ for ($V_i > V_{ref}$) the input voltage greater than the reference voltage. The circuit diagram,input and output waveforms are shown in Fig 2.

Fig 2



A. NON INVERTING COMPARATOR INPUT AND OUTPUT WAVEFORM FOR
B. VREF POSITIVE
C. VERF NEGATIVE
D. PRACTICAL NON INVERTING COMPARATOR

EMN21017052

Differentiator :

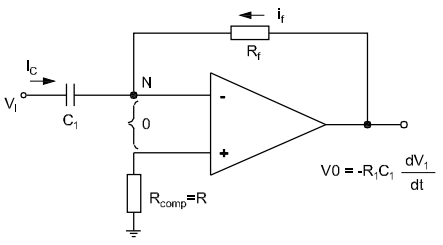
One of the simplest of the op-amp circuit that contain capacitor is the differentiator. It performs mathematical operation of differentiation, that is the output waveform is the derivative of input waveform. It produces an output signal proportional to the rate of change of its input signal.

Analysis :

The node N is at virtual ground potential (i.e) $V_N = 0$. The current through the feedback resistor is V_0/R_f and there is no current through the op-amp. Therefore the nodal equation at node N is

$C_1 dV_1/dt + Vo/R_f = 0$ (or) $Vo = -R_f C\, dVi/dt$.

Fig 3



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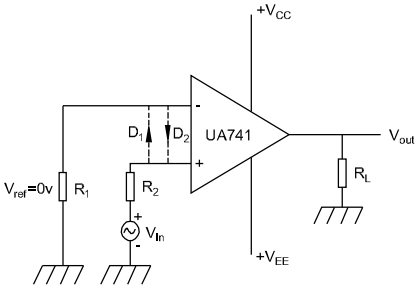
Thus the output voltage V_o is a constant ($-R_fC_1$) times the derivative of the input voltage V_1 and circuit is known as differentiator which is shown in Fig 3. The minus sign indicates a 180 phase shift of the output waveform Vo with respect to the input signal. The output is the time derivative of the input signal, if V_i = sin wt.So the output of the op-amp varies with frequency and will vary high at high frequency. Hence it is also known as “High Pass filter circuit’.

Adding the input resistor R_{in} inseries to the capacitor will increase the gain by R_F/R_{in} and it will act as a differenctiator at low frequencies.

Zero Crossing Detector using 741 IC is shown in Fig 4.The zero crossing detector circuit is an important application of the **Op-Amp comparator circuit**. It can also be called as the sine to square wave converter. Anyone of the inverting or non-inverting comparators can be used as a zero-crossing detector. The only change to be brought in is the reference voltage with which the input voltage is to be compared, must be made zero (Vref = 0V). An input sine wave is given as Vin. These are shown in the circuit diagram and input and output waveforms of an inverting comparator with a 0V reference voltage.

Fig 4



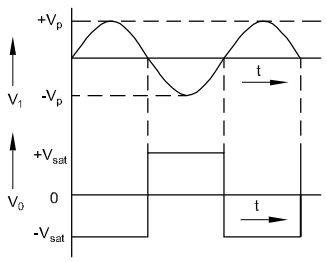
Zero Crossing Detector Using UA 741 op-amp IC

EMN21017054

Zero-Crossing Detector Using UA741 op-amp IC

As shown in Fig 5 the waveform, for a reference voltage of 0V, when the input sine wave passes through zero and goes in positive direction, the output voltage Vout is driven into negative saturation. Similarly, when the input voltage passes through zero and goes in the negative direction, the output voltage is driven to positive saturation. The diodes D1 and D2 are also called clamp diodes. They are used to protect the op-amp from damage due to increase in input voltage. They clamp the differential input voltages to either +0.7V or -0.7V.

Fig 5



Zero Crossing Detector Using 741IC Waveform

EMN21017055

In certain applications, the input voltage may be a low frequency waveform. This means that the waveform only changes slowly. This causes a delay in time for the input voltage to cross the zero-level. This causes further delay for the output voltage to switch between the upper and lower saturation levels. At the same time, the input noises in the op-amp may cause the output voltage to switch between the saturation levels. Thus zero crossing are detected for noise voltages in addition to the input voltage. These difficulties can be removed by using a **regenerative feedback circuit with a positive feedback** that causes the output voltage to change faster thereby eliminating the possibility of any false zero crossing due to noise voltages at the op-amp input.

Integrator Using Operational Amplifier

Objectives : At the end of this lesson you shall be able to
- **explain the performance of circuit using Op-Amp integrator**
- **how to reduce the output offset voltage in Op-integrator.**

An integrator is a circuit that performs the mathematical operation of integration since it produces an output voltage that is proportional to the integral of the input. With an Op-amp, we can build an integrator, a circuit that produces a well defined ramp output for a rectangular constant input.

The Fig 1 shown is an Op-Amp integrator. The typical input to an integrator is a rectangular pulse. As shown in Fig 1b, the V_{in} represents a constant voltage during pulse time T and it is applied to the left end of R. Because of virtual ground, the input current is constant and equals. $I_{in} = V_{in} / R$. Approximately all this current goes to the capacitor. The basic capacitor law says that

$C = Q/V$ or $V = Q/C$ ..... (1)

The change Q increases linearly since a constant current is flowing into the capacitor. This means that the capacitor voltage increases linearly with the polarity. The output voltage is a negative ramp because of the phase reversal of the Op-Amp as shown in Fig 1C. At the end of the pulse period, the input voltage returns to zero, and the charging current stops. Since the capacitor hold its charge, the different voltage remains constant at a negative level.

For output voltage divide eq.(1) by T

$$V/T = \frac{Q/T}{C}$$

Since the charging is constant, we can write

$V/T = I/C$

or $V = IT/C$ ..... (2)

Where V = capacitor voltage

I = charging current, Vin / R

T = charging time

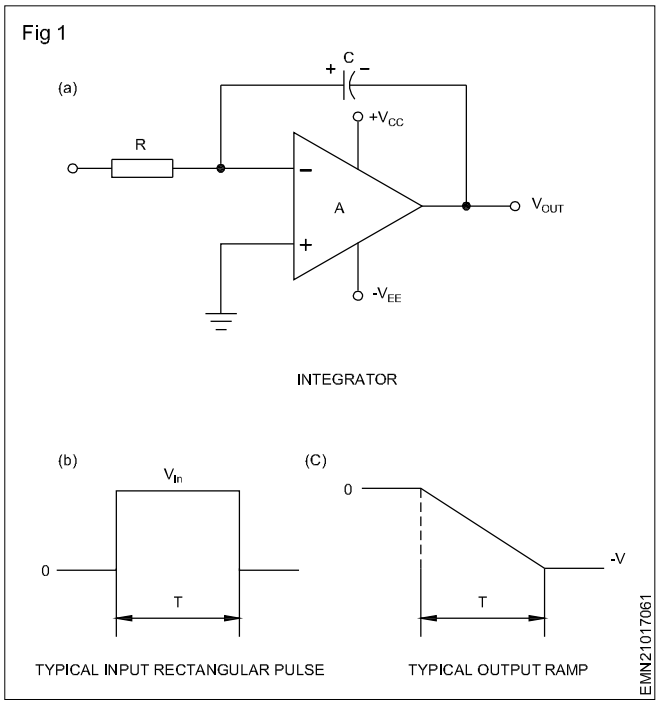
C = capacitance.

This is the voltage across the capacitors. Because of the phase reversal, $V_{out} = - V$.

For Example: If I = 4mA, T = 2msec and C = 1 F, then the capacitor voltage at the end of the charging period is (4mA) (2ms)/1uF = 8V because of the phase reversal, the output voltage is -2V after 2ms.

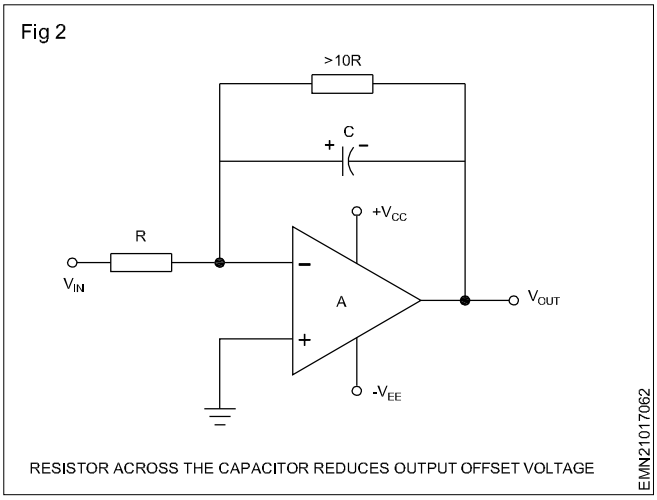
In Fig 1, since the capacitor acts like an open to DC signals, the closed-loop voltage gain equals to the open-loop voltage gain at zero frequency. This will produce too much output offset voltage without negative feed back at zero frequency, the circuit will treat the input offsets as a valid input signal. The input offsets will eventually charge the capacitor and drive the output into positive or negative saturation.

Fig 1



By inserting a resistor in parallel with capacitor as shown in Fig 2, we can reduce the effect of input offsets. This resistor should be atleast 10 times larger than the input resistor i.e., if the added resistance equals 10R, the closed loop voltage gain is -10 and the output offset voltage is greatly reduced.

Fig 2



Op-Amp Applications - Differential & Instrumentation Amplifiers

Objectives : At the end of this lesson you shall be able to
- **describe the working of differential amplifier**
- **describe the operation of Instrumentation amplifier.**

Differential amplifier :

The easiest way to construct fully-differential circuit is to think of the inverting op-amp feedback topology. In fully-differential op-amp circuits, there are two inverting feedback paths:

1 Inverting input to noninverting output

2 Noninverting input to inverting output

Both feedback paths must be closed for the fully - differential op-amp to operate properly.

The differential amplifier has a unique feature that many circuits don't have - two inputs. This circuit amplifies the difference between its input terminals. Other circuits with one input actually have another input – the ground potential. But, in cases where a signal source (like a sensor) has both of its terminals biased at several volts above ground, you need to amplify the difference between the terminals. What about noise that adds an unwanted voltage equally to both terminals of a sensor? The differential amplifier reject the noise and rescue the signal.

A new pin :

Fully-differential op-amps have an extra input pin (V_{COM}). The purpose of this pin is to provide a place to input a potentially noisy signal that will appear simultaneously on both inputs – i.e. common mode noise. The fully-differential op-amp can then reject the common mode noise.

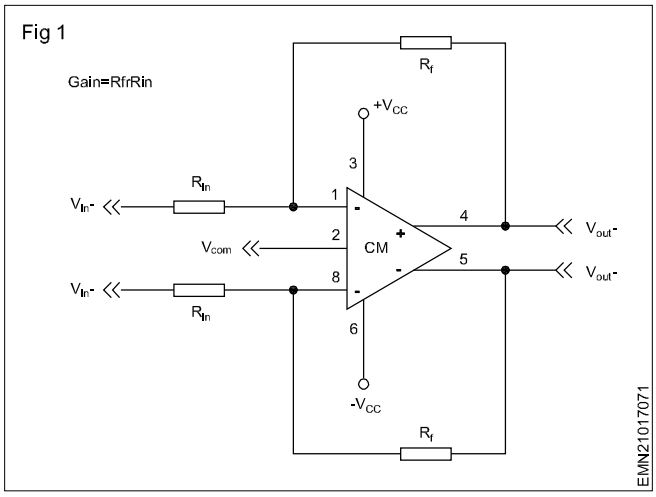
The V_{COM} pin can be connected to a data converter reference voltage pin to achieve tight tracking between the op-amp common mode voltage and the data converter common mode voltage. In this application, the data converter also provides a free dc level conversion for single supply circuits. The common mode voltage of the data converter is also the dc operating point of the single-supply circuit. The designer should take care, however, that the dc operating point of the circuit is within the common mode range of the op-amp + and – inputs. This can most easily be achieved by summing a dc level into the inputs equal or close to the common mode voltage.

Gain

A gain stage is a basic op-amp circuit. Nothing has really changed from the single-ended design, except that two feedback pathways have been closed. The differential gain is still Rf /Rin a familier concept to analog designers. fig 1 shows the differential amplifier circuit.

This circuit can be converted to a single-ended input by connecting either of the signal inputs to ground. The gain equation remains unchanged, because the gain is the differential gain.

Fig 1



Instrumentation amplifier:

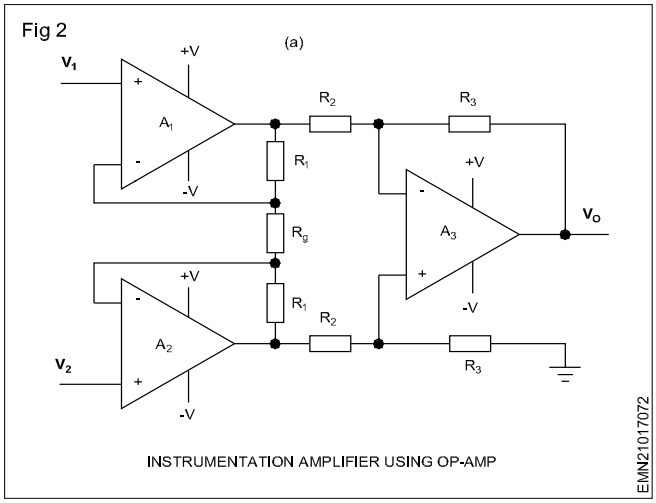
An instrumentation system is used to measure the output singal produced by a transducer. The input stage is composed of a transducer, depending on the physical quantity to be measured.

The output stage may use devices such as meters, oscilloscopes and display circuits. The signal source of instrumentation amplifier is the output of the transducer. To amplify the low level output signal of the transducer, instrumentation amplifier is used in the middle.

Instrumentation amplifier is a kind of differential amplifier with additional input buffer stages. The addition of input buffer stages makes it easy to match impedance with the preceding amplifier stage. Instrumentation amplifier is commonly used in industrial test and measurement applications. They are generally used in situations where high sensitivity, accuracy and stability are required.The instrumentation amplifier also has some useful features like low offset voltage, high CMRR (Common mode rejection ratio), high input resistance, high gain etc.

The circuit diagram of a typical instrumentation amplifier using three op-amps is shown in Fig 2.

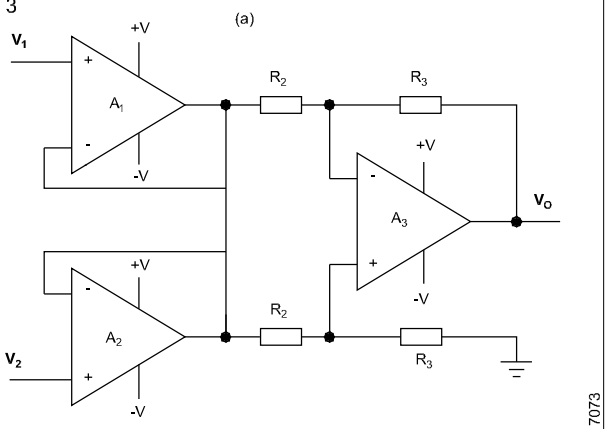
Fig 2



A circuit providing an output based on the difference between two inputs is given in the above circuit. In the circuit diagram, op-amps labelled A1 and A2 are the input buffers. The gain of these buffer stages are not unity because of the presence of R1 and Rg. Op amp labelled A3 is wired as a standard differential amplifier. R3 connected from the output of A3 to its non-inverting input is the feedback resistor. R2 is the input resistor.

The voltage gain of the instrumentation amplifier can be expressed by using the equation below:Voltage gain (Av)= Vo/(V2-V1) = (1 + 2R1/Rg) x R3/R2. For varying the gain, replace Rg with a suitable potentiometer. A simplified instrumentation amplifier design isshown in Fig 3.

Fig 3



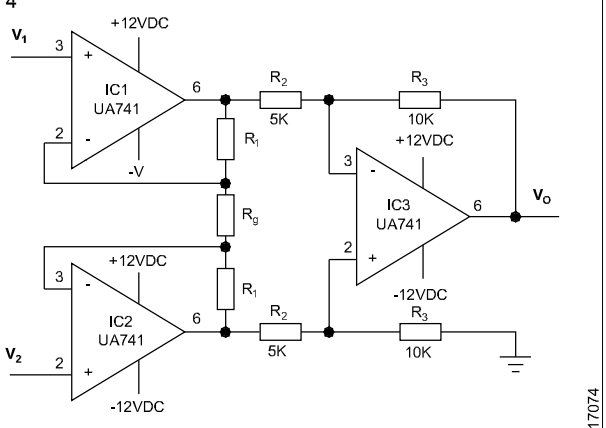
SIMPLIFIED INSTRUMENTATION AMPLIFIER

Here the resistances labelled R1 are shorted and Rg is removed. This results in a full series negative feedback path and the gain of A1 and A2 will be unity. The removal of R1 and Rg simplifies the equation to Av = R3/R2.The output impedance is also low, being in the range of milliohms. The input bias current of the instrumentation amplifier is determined by the op-amps A1 and A2.

Practical instrumentation amplifier using op-amp.

A practical instrumentation amplifier circuit designed using uA741 op amp is shown in Fig 4. The amplifier operates from +/-12V DC and has a gain 10. If you need a variable gain, then replace Rg with a 5K POT. Instead of using uA741 you can use any op-amp but the power supply voltage must be changed according to the op amp. A single LM324 op amp IC is a good choice. Out of the four op-amps inside the LM324, three can be used for IC1, IC2, IC3 and the remaining one can be left alone. This reduces the PCB size a lot and makesthe circuit compact. Supply voltage for LM324 can be up to +/-15V DC.

Fig 4



PRACTICAL INSTRUMENTATION AMPLIFIER USING OP-AMP

A high gain accuracy can be achieved by using precision metal film resistors for all the resistances. Because of large negative feedback employed, the amplifier has good linearity, typically about 0.01% for a gain less than 10.

Once the circuit is built, set the function generator to a 500mVp-p Sine wave at 1 kHz and input it to V1, as shown in figure 3 andground the other input terminal (V2).

In order to test the gain of the instrumentation amplifier, place the oscilloscope probe of Channel-1 on the function generator and another probe on the output of instrumentation amplifier. With the power supplied to the circuit and a proper waveform as an input, one should see an output similar to Fig 5.

Fig 5

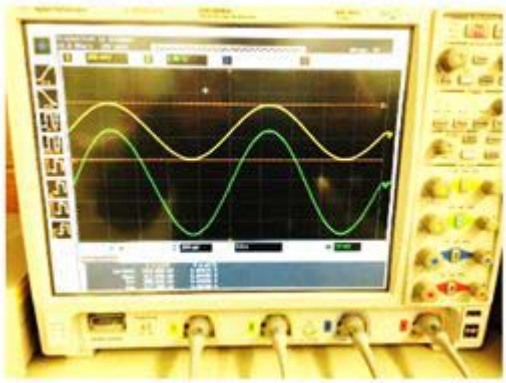


Fig 5 displays the input and the output on the same time scale, but different voltage scales. To ensure the gain is about 10, take the output voltage and divide it by the input voltage. This example has Vout/Vin = 5.046 V/513.66 mV = 9.82.

Instrumentation amplifiers are easy to design and can be used in many applications.The simplicity of the design depends on the selection of the resistor values. Ifchosen correctly, the gain can be calculated and changed only with one resistor value.

Timer IC and its applications

Objectives : At the end of this lesson you shall be able to
- **list the features that make 555 a popular integrated circuit**
- **name the functional blocks of a IC555**
- **describe the principle of operation of a IC555**
- **list different types of packaging of IC555**
- **explain the schematic of an astable multi-vibrator using IC 555**
- **find the ON-time and OFF-time of a given astable multi-vibrator using 555**
- **explain the term PRF**
- **list a few applications of astable multi-vibrator**
- **describe the working of VCO using IC 555.**

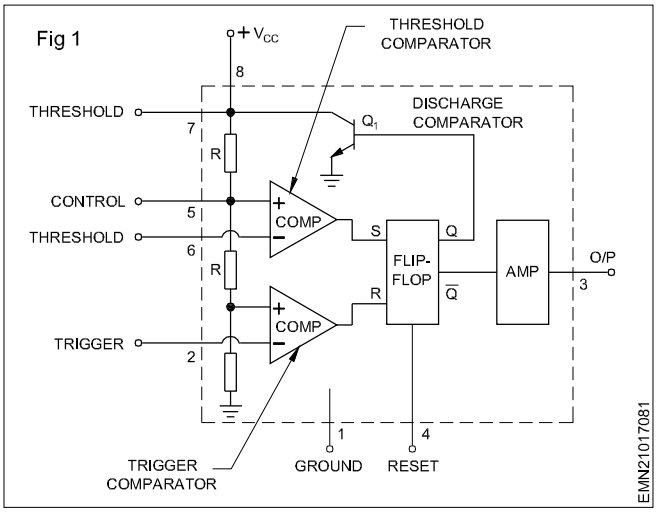
Timer

Applications such as square wave, ramp, pulse generators, and one-shot multi-vibrators etc. require a circuit essentially capable of producing timing intervals. Due to the circuit components count and the delicacy in using transistors, integrated circuits(ICs) are preferred. One such most suitable and popular IC for producing timing intervals is the 555. This IC is popularly known as **555 timer**. Similar to operational amplifiers, 555 IC is reliable, easy to use in a variety of applications, and at low cost. The 555 IC can operate from a wide range of supply voltages of + 5 V to +18 V. This makes 555 compatible with standard digital circuits whose voltage levels(0-state = 0V, 1-state = 5 V) are known as TTL (transistor-transistor logic) levels.

The 555 timer

The functional blocks in 555 timer is shown in Fig 1.

Fig 1



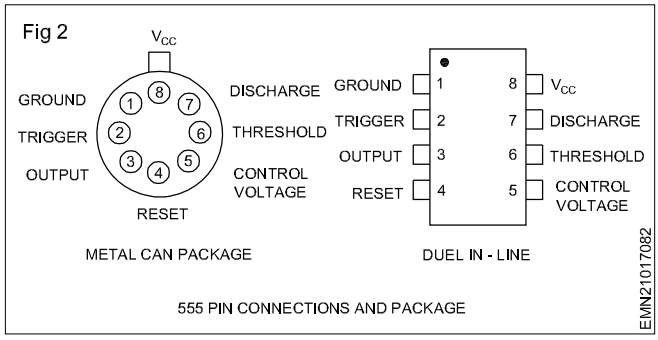
As can be seen from Fig 1, the 555 IC contains two comparators, one transistor, three equal value resistors, a flip-flop, and an output stage. Timer find application in precision timing, pulse generator, sequential timing, time delay circuits, pulse width modulation, pulse position modulation and linear ramp generator circuits, time period is adjustable from micro seconds to hours. Output source or sink current 200 mA, output and supply TTL compatible temperature stability each better than 0.005% per degree centigrate. Normally ON and normally OFF output they are available in 8 and 16 pin package.

A comparator is a circuit having two inputs and a single output. It compares the signal voltage given at one input with a reference voltage on the other input as shown in Fig 2. Comparators are essentially made using Op-Amps.

Types of 555 timer IC packages

The 555 timer IC is available in two package styles metal can (TO) and DIP as shown in Fig 2.

Fig 2



Source and Sink current capacity

The internal circuitry of 555 requires about 0.7mA per supply volt (7 mA for V_{CC} = +10V) to set up internal bias currents. Maximum power a 555 IC can dissipate is around 600 mW.

The maximum current that can be drawn from the output terminal(pin No.3) of 555(called source current) or the maximum current that can be forced through the output terminal(called sink current) is around 40 mA.

Modes of operation

The 555 IC timer has two modes of operation:

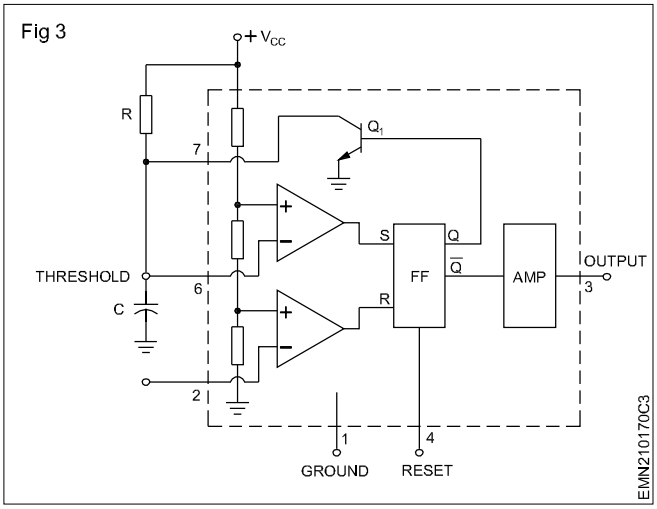
– as an astable(free-running) multi-vibrator
– as a mono-stable (one-shot) multi-vibrator.

Principle of 555 operation

Referring to the block diagram of IC 555 in Fig 1, at the input there are two comparators connected to an internal resistive voltage divider. Both comparators have a reference input tied to the voltage divider. The **threshold comparator** is referenced to as 2(V_{CC}/3), and the **trigger comparator** is referenced to as V_{CC}/3. Comparator outputs are connected to a **set-reset flip-flop**. If the trigger voltage input falls below V_{CC}/3, its associated comparator resets the flip-flop output low.

For using the 555 IC, certain external components are required to be connected as shown in Fig 3.

Fig 3



The threshold input is usually connected to an external RC timing circuit. If the capacitor charge(threshold input) exceeds the 2/3 V_{CC} reference on the threshold comparator, the comparator is triggered and the flip-flop is set. When the flip-flop is set, the discharge transistor is turned-on and the capacitor discharges.

IC 555 as an astable multi-vibrator

Fig 5 shows 555 connected for astable operation.

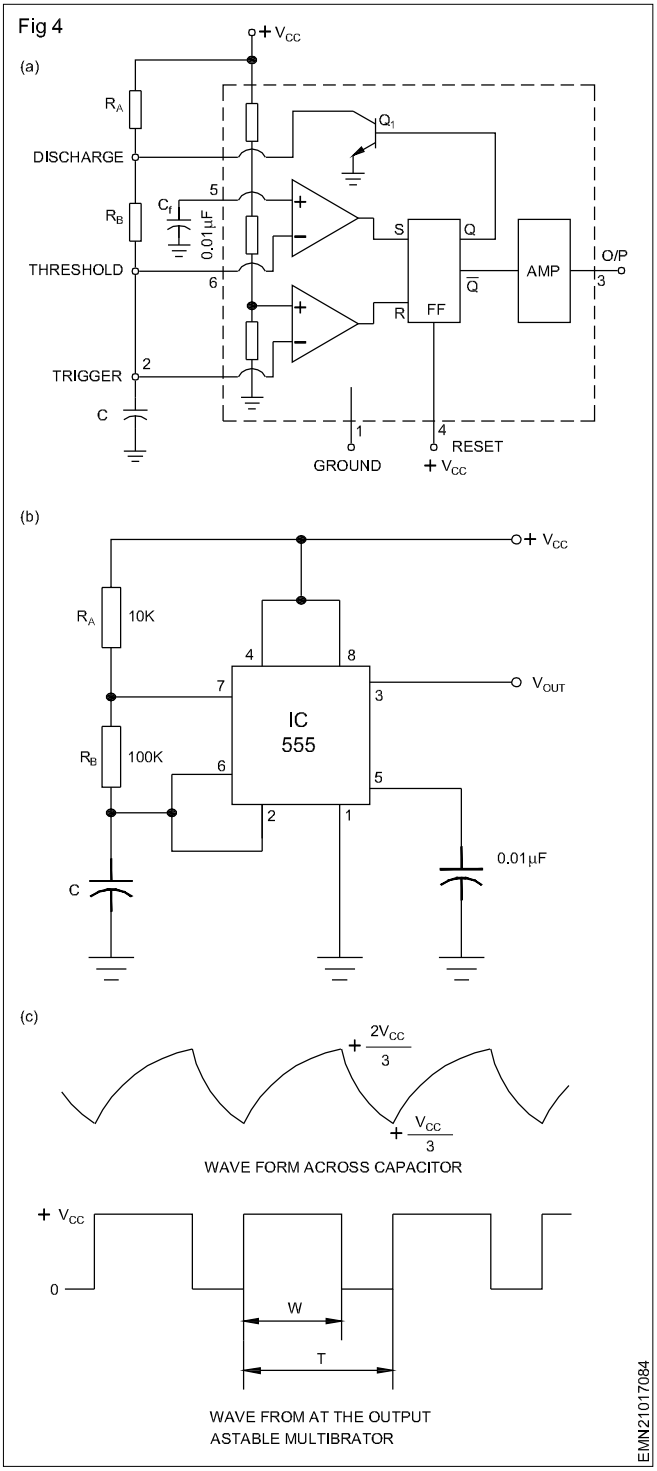
- The reset input is connected to V_{CC}. If it were connected to ground, 555 will get disabled.
- C_f provides noise filtering for the control voltage input.
- When the discharge transistor is off, capacitor C is charging through R_A and R_B. Thus the circuit time constant is given by,

  $t = (R_A + R_B)C$
- As capacitor C charges, the threshold input voltage will soon reach $2V_{CC}/3$. At this point the flip-flop changes states, causing the discharge transistor Q_1 to turn on. Transistor Q_1 saturates and discharges C through resistor R_B and Q_1. The discharge time constant is therefore given by,

  $t = R_B C$
- Since the threshold and trigger inputs are tied together, as C discharges, at some point it falls to a value below 1/3 V_{cc} and activates the trigger comparator. This resets the RS flip-flop, turning OFF Q_1 and allowing C to start charging again. So, 555 operates as an astable multi-vibrator by causing C to continuously charge and discharge between 1/3 V_{cc} and $2/3V_{cc}$. Wave-forms at the capacitor(trigger input) and at the output 555 are shown in Fig 4c.

It is important to note that, because the charging path for C is through $R_A + R_B$ and the discharge path is through only R_B, the output is not symmetrical. In other words, the ON-time and the OFF-time of the output pulses are not equal. The ratio of the ON-time of the pulse to the OFF-time of the pulse is known as **duty cycle**. The duty cycle of 555 astable circuit range from near 50% to near 100%. The duty cycle can be calculated as follows:

Fig 4



$$\text{Duty cycle(D)} = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

From the above equation,

- if R_B is made much greater than R_A, the duty cycle will approach 50 %.
- for higher duty cycle, R_A should be made greater than R_B.

Pulse Repetition Frequency(PRF)

The term frequency is generally used with repetitive wave-forms which are symmetrical such as sine wave form. For repetitive wave-forms which are non-symmetrical such as the output of an astable multi-vibrator, instead of the term frequency the term **Pulse Repetition**

Frequency(PRF) is used. PRF can be calculated as follows:

If t_{ON} is the ON-time of the pulse
and, if t_{OFF} is the OFF-time of the pulse,
then, Time period, $T = t_{ON} + t_{OFF}$

Hence, $PRF = \frac{1}{T}$

Application of astable multi-vibrators

Application of astable multi-vibrators are almost innumerable: some general applications are listed below;

– In electronic pianos : different frequencies are generated by astable with different RC values.
– Signal injectors : used as a testing instrument by service technicians.
– Flashing light : if lamps or LEDs are connected at the output of the astable, the lamp/LED flashes at the rate set by the values of RC.
– As Voltage Controlled Oscillator(VCO): The oscillator frequency is controlled by the input control voltage. A VCO circuit is shown in Fig 6.

IC 555 Timer as VCO

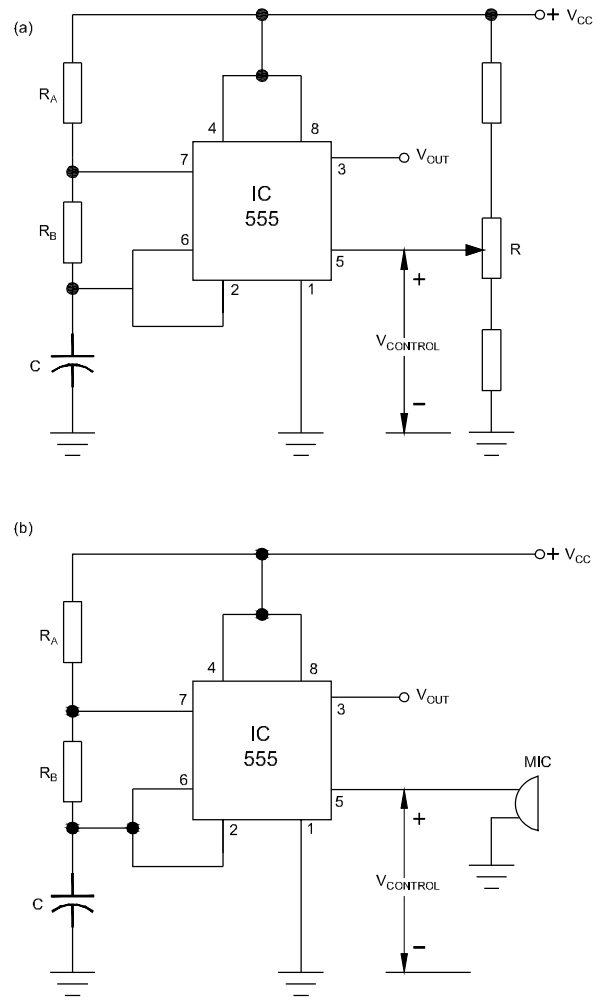
A Voltage-Controlled Oscillator (VCO) changes its output frequency in relation to the input voltage at the control input of the threshold comparator(pin No.5). The voltage at pin 5 is normally $2/3V_{cc}$ owing to the internal resistive voltage divider. However, by connecting an external component or voltage source as shown in Fig 6a, the voltage at pin 5 can be changed. If the voltage on pin 5 is raised, the capacitor must charge to a higher value, which decreases the output frequency. With pin 5 elevated in voltage, a greater time is required for C to discharge to $1/3V_{CC}$ as well.

Voltage controlled oscillator circuit can be used in digital circuits where, data are converted to tones for recording or transmission on telephone lines. Such a circuit may produce a tone of 2400 Hz when a low is applied to pin 5 and a tone of 1200 Hz when a high is applied. Fig 5b shows a typical VCO whose output frequency is in relationship to the voice input amplitude.

Working ofMonostable Mutlivibrator with 555 Timer Circuit

- The output of the monotablemultivibrator using 555 timer remains in its stable until it gets a trigger.
- In monostaable 555 multivibrator, when both the transistor and capacitor are shorted then this state is called as a stable state.
- When the voltage goes below at the second pin of the 555 IC, the o/p becomes high. This high state is called quasi stable state. when the circuit activates then the transistion from a stable to quasi stable state.
- Then the discharge transistor is cut off and capacitor starts charging to VCC. Charging of the capacitor is done via the resistor R1 with a time constant R1C1
- Hence, the voltage of the capacitor increases and finally exceeds 2/3 V_{CC}, it will chane the internal control flip flop, thereby turning off the 555 timer IC
- Thus the o/p goes back to its stable state from an unstable state.

Fig 5



VOLTAGE CONTROLLED OSCILLATOR CIRCUIRTS

Finally we can conclude that,in themonostablemultivibrator using 555 timer, the output stays in a low state until it gets a trigger input. This type of operation is used in push to operte systems. When the input is triggered, then the will go to high state and comes back to its original state.

555 timer Example

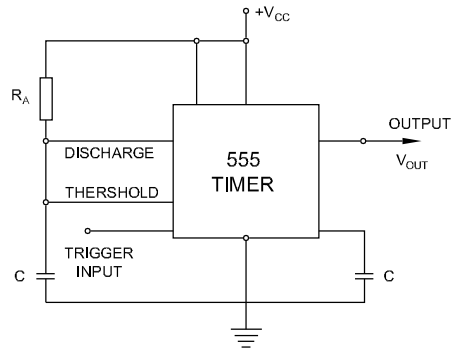
A 555 Timer IC in a Monostablemultivibrator in needed to produce a time delap in a circuit. If a 10 mF timing capacitor is used, then calculate the value of the resistor required to poduce a minimum output time delay of 500ms.

R=t/1.1C

Where,t=0.5,C=10mF

Insert these values in the above formula

Fig 6



$R=0.5/1.1x10x10^{-6}$

=45.5kilo Ohms

Applications of 555 timer in Monostable Mode

The applications of the 555 timer circuits mainly involve in various 555 timer based projects in monostable mode.

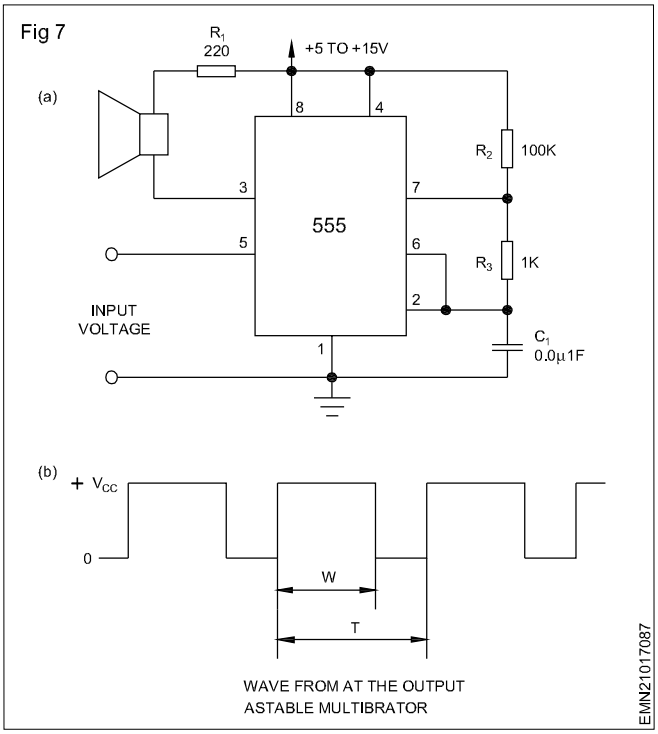
Voltage Controlled Oscillator (VCO)

Voltage-Controlled Oscillator (VCO) circuit using the 555 timer IC as the main component as shown in Fig 7(a). As expected, the 555 timer is configured as an astable multi vibrator to be able to serve as an oscillator. An astable multi vibrator is just a timing circuit whose output oscillates between 'low' and 'high' continuously, in effect generating a train of pulses, as shown in the Fig 7(b) of the circuit.

1) The difference of this circuit with the basic 555 astable circuit is that its 555's pin 5 is tied to an external voltage source.

2) Pin 5 is the 555's control voltage pin, which allows the user to directly adjust the threshold voltages to which the pin 2/pin 6 input voltages are compared by the 555's internal comparators. Since the outputs of these comparators control the internal flip-flop that toggles the output of the 555, adjusting the pin 5 control voltage also adjusts the frequency at which the 555 toggles its output.

Fig 7



3) Increasing the input voltage at pin 5 decreases the output oscillation frequency while decreasing the input voltage increases the output oscillation frequency.

Application of VCO

- Phase locked loop.
- Function generator.
- Frequency synthesizers, used in communication circuits.
- Production of electronic music/different types of noise.
- Electronic jamming equipment.

Monostable multivibrator

Objectives : On completion of this lesson you shalll be able to

- **monostable multivibrator circuit using timer IC 555**
- **find values of R and C for a required output pulse width**
- **name the most popular application of mono-shot**
- **explain pulse width modulator using timer IC 555**

IC 555 as a Monostable multivibrator

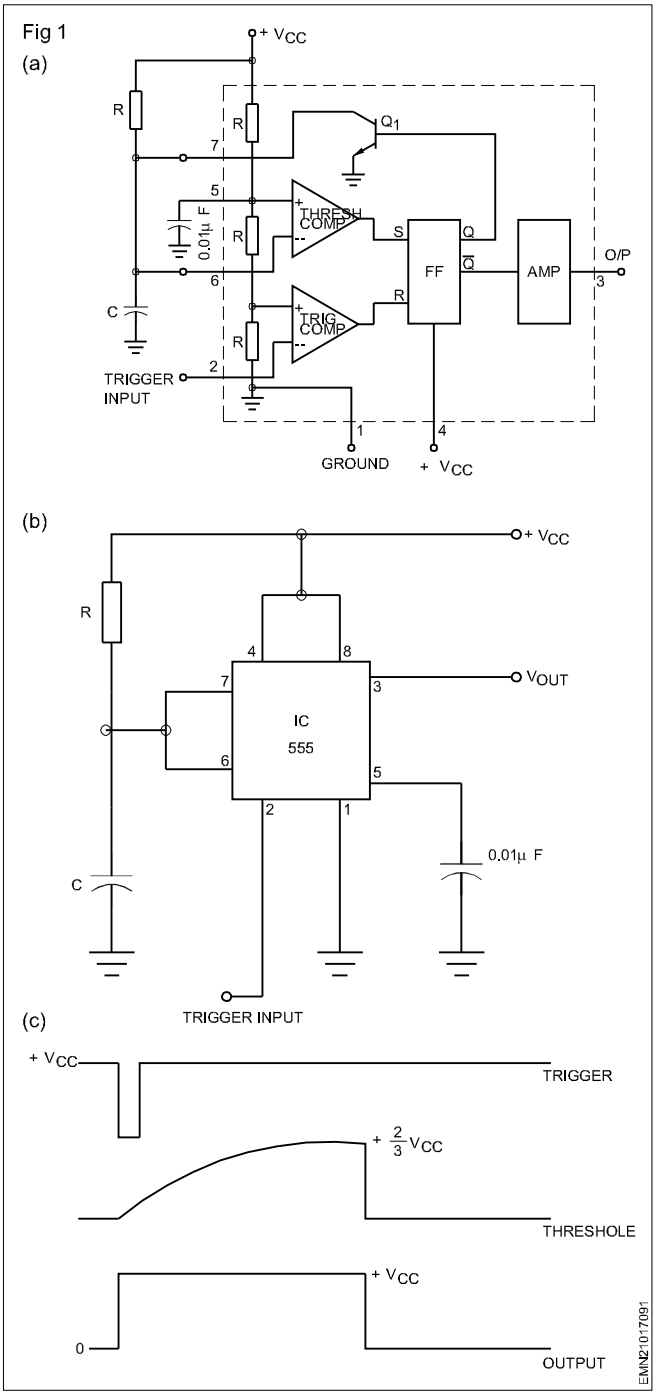
Fig 1, shows the circuit connections of a monostable multivibrator using 555 timer IC. It is also called as mono shot multi.

In Fig 1, unlike in an astable multi-vibrator, the trigger input is held at voltage near $V_{CC.}$ When the monosatable timer is to be made to change to its state, the trigger input must be made to fall to less than $1/3V_{CC}$.

When a trigger input is given i.e when the level at the trigger input is brought below $1/3V_{CC,}$ the flip-flop is reset, therefore Q_1 goes to cut-off, and C begins to charge.

When the charge on C increases to $2/3\ V_{CC,}$ the flip-flop is made to set by the threshold comparator. Thus Q1 is turned ON and C is discharged. The timer stays in this stable state, and nothing happens tills the trigger input is brought to less than $1/3V_{CC}$.

The time during which the output stays in the high state is determined by the RC time constant. The larger Ror C is, the wider the output pulse. The formula for pulse width is given by,



Pulse width (W) = 1.1RC

For exmple, if R= 10K and C=0.01F, the mono-stable output pulse width will be,

$$W=1.1 \times 10 \times 10^{3} \times 0.01 \times 10^{-6}$$

$$= 0.11 \text{ m sec.}$$

If the value of R is increased to R =100K and C =0.01F, the mono-stable output pulse width will be,

$$W=1.1 \times 100 \times 10^{3} \times 0.01 \times 10^{-6}$$

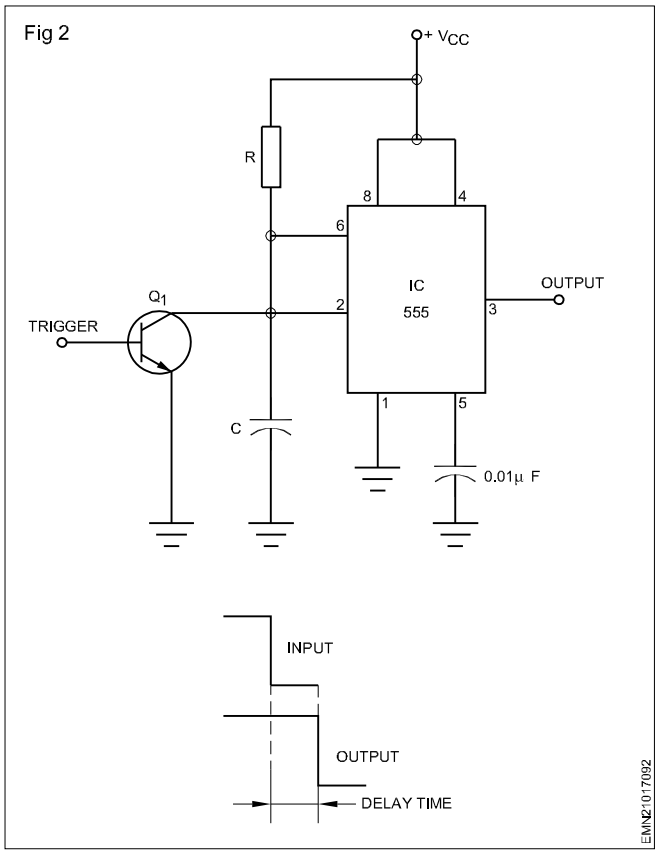
$$= 1.1 \text{ m sec.}$$

In Fig 1,notice that pin 5 is bypassed to ground by a small-value capacitor. The value of this capacitor is typically about 0.01F, an dits purpose is to provide noise filtering for the contorl voltage.Pin 4 is alos tied high (+ V_{CC}) agin. Recall that, if pin 4 is tied low, the 555 will not operate and will be in the reset state.

Applications of 555 Mono-shot

Applications of 555 timer as mono- shot are as numerous or even more than that of astable multivibnrator. Amongst the applications of 555 as mono- shot, the most popular uses are in the time delay or timer circuits. Fig 2 shows a 555 used as a time-delay device.

In the circuit at Fig 2, the output changes states after a delay period once the input trigger pulse is received.The duration of delay in the output is decided by the values of the circuit components R and C.



In the circuit at Fig 2, assume that the transistor is ON and hence pin 2 of 555 is at ground. Because of this, capacitor C is unable to charge.

When negative trigger input pluse is applied to the base of transistor Q1,Q1 is turned off. On cut-off of Q1, capacitor C begins to charge until it reaches 2(VCC/ 3).Once the charge on C goes slightly above 2(VCC/3), the 555 output is made to change state.

The delay in the change of state at output is due to th eRC time constant.Simple time delay circuit shown in Fig 2 is used where a short time delay is required.One application of such a delay circuit is in disk drives in computers.Computer users should not keep floppy disks in the drives when the computer is turned on. This is beacause, the power surge can damge the written information on the disk and make it non-readable. If the user happens to have kept the floppy disk unknowingly, then, using a time delay circuit if the disk electronics are turned on a fraction of a second after the power has been

turned on, the surge would not exist, and therefore, there is no danger of the information on the disk getting corrupted (damaged).

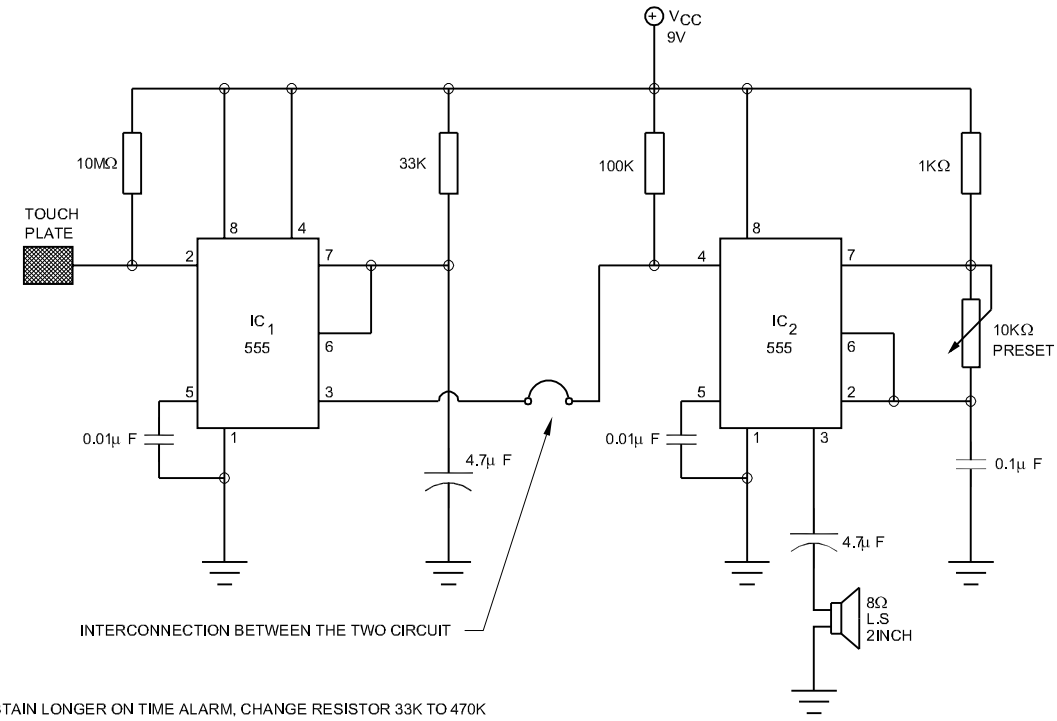
Security alarm circuit using Mono-shot and Astable

Fig 3 shows a security alarm circuit, which gives and audible alarm when an intruder happens to toch the trigger touch plate.

The circuit consists of a mono-shot coupled to a astable multivibrator.When the touch plate is touched by hand the monoshot makes its output go high for some duration (set by RC).This high level is coupled, to the reset pin (pin4) of the astable. Recall that the output of the astable will be present only when the reset pin is help high. Therefore, as long as the reset pin of astable is high, astable gives a repetitive output pulses(PRF set by RC values) which makes the speakergive an audible alarm calling the attention of the security.

The circuit at Fig 3 can be modified to suit several other applications such as,

Fig 3



- water level indicator
- smoke detector
- fire detector and so on.

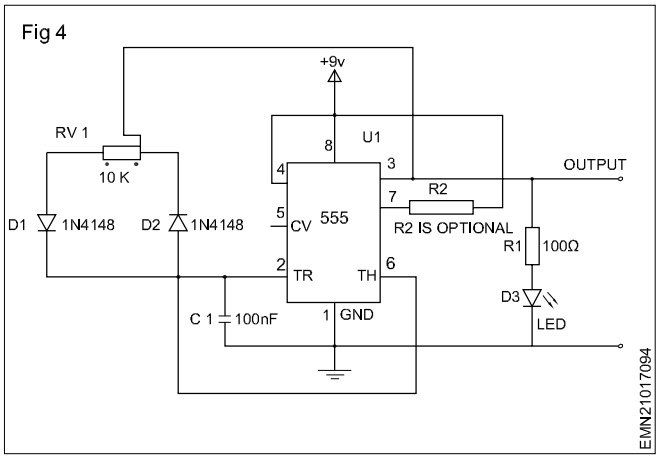
For further reading on 555 applications refer reference bools listed at the end of this book.

Pulse Width Modulation

PWM (Pulse Width Modulation) is one of the circuits for controlling many electronics devices. PWM is a digital signal which is most commonly used in control circuitry. PWM is widely used for motor controlling, lighting controlling etc. Sometime we do not use microcontroller in our applications and if we need to generate PWM without microcontroller then we prefer some general purpose ICs like op-amp, timers, pulse generators etc. 555 Timer IC is a very useful and general purpose IC which can be used as Pulse Width Modulator.The circuit using a 555 timer IC for generating PWM is shown in Fig 4.

In this circuit,the output frequency of PWM signal is controlled by selecting resistor RV1 and capacitor C1. A variable resistor is usedin place of fixed resistor for changing duty cycle of the output signal. Capacitor

Fig 4



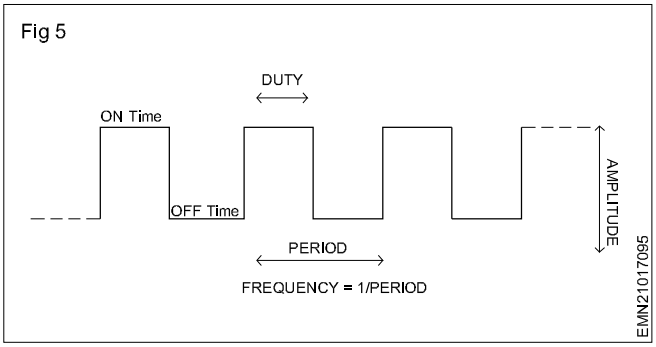
Charging through D1 diode and Discharge through D2 diode generates PWM signal at 555 timer's output pin. The frequency of PWM signal is calculated using the formula:

$$F = 0.693*RV1*C1$$

This signal is set high (5v) and low (0v) in a predefined time and speed. The time during which the signal stays high is called the "on time" and the time during which the signal stays low is called the "off time". There are two important parameters for a PWM as discussed below:

1. **Frequency of a PWM:** The frequency of a PWM signal determines how fast a PWM completes one period. One Period is complete ON and OFF of a PWM signal as shown in Fig 5.

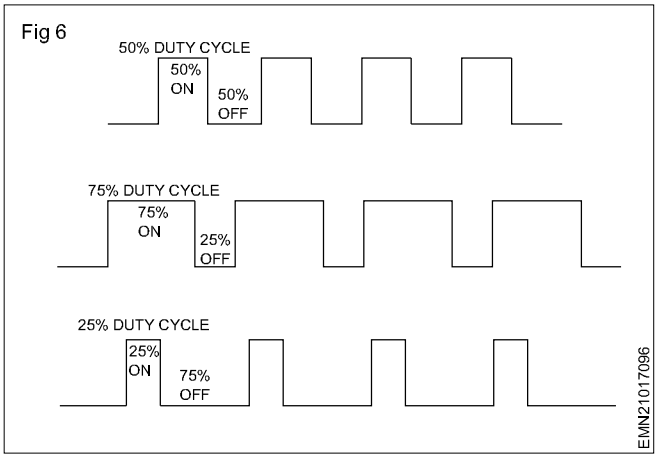
Fig 5



2. **Duty cycle of the PWM:** The percentage of time in which the PWM signal remains HIGH (on time) is called as duty cycle. If the signal is always ON it is in 100% duty cycle and if it is always off it is 0% duty cycle. Duty Cycle =Turn ON time / (Turn ON time + Turn OFF time).

Different duty cycle of PWM waveforms are shown in Fig 6.

Fig 6



3. Pulse Width Modulation, or PWM, is a technique for getting analog results with digital means. Digital control is used to create a square wave, a signal switched between ON and OFF.